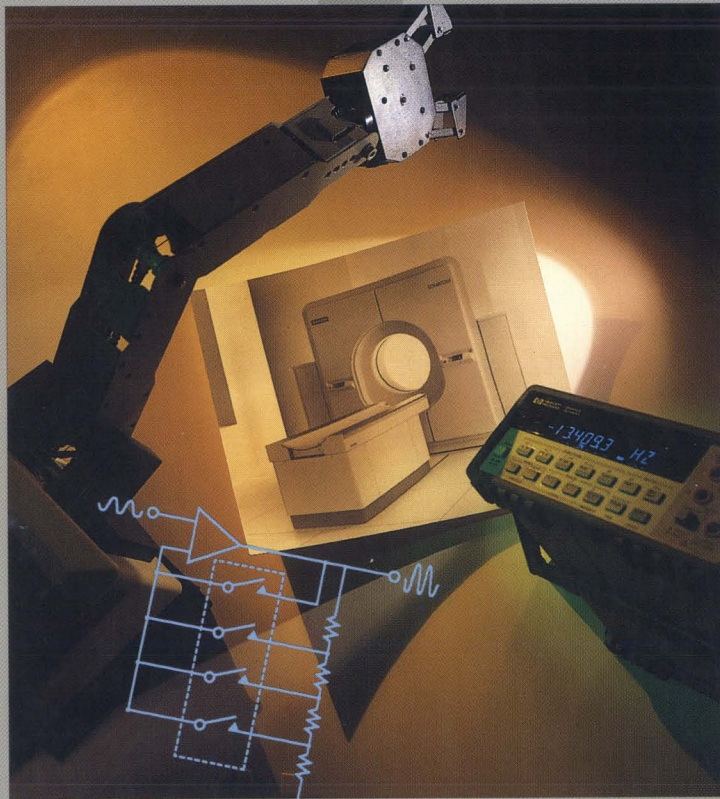


# Analog Integrated Circuits

1994



**Siliconix**  
A Member of the **TEMIC** Group



# **Analog Integrated Circuits Data Book**

**1994**

**Siliconix**  
A Member of the TEMIC Group

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Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## About Siliconix

Siliconix is a leading manufacturer of semiconductor products for the computer, communications, automotive, industrial, and hi-rel markets. The company's products bridge the interface gap between real-world analog signals and the digitally operated microprocessor, providing both discrete and integrated solutions to

- sense, convert, and control signals at a system's input
- regulate and manage the system's power supplies
- provide useful signals and power at the output.

As a member of TEMIC, the microelectronics enterprise of Daimler-Benz, Siliconix has expanded its worldwide presence and is further equipped to serve its customers on an international scale by sharing the technologies and applications expertise of its sister companies and by taking advantage of a combined international sales network.

In keeping with this global perspective, the company has aggressively pursued world-class standards of cycle time, yields, and average outgoing quality in its manufacturing facilities in the United States and Asia. Siliconix' continuous improvement efforts have resulted in dramatic improvements for each of these areas and in numerous quality awards from its customers. The company has pursued international quality certifications as well, and received ISO 9001 certification for its Santa Clara facilities in November 1993. Our booklet "Making Continuous Improvement A Way of Business" tells more about our commitment to quality. You can request a copy by calling (800) 554-5565.

The Company's manufacturing operations include wafer fabrication, assembly, and product testing. All wafer fabrication is done in Santa Clara, where the facilities include a four-inch wafer fab and a Class 1, six-inch wafer fab. High-volume assembly and product testing for plastic- and ceramic-packaged products are handled in the Company's facilities in Taiwan, the Philippines, and China.



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## About This Data Book

The products detailed in this data book include analog switches and multiplexers, wideband video switches, multiplexers, crosspoints, buffers, amplifiers, and voltage converters. These products are designed for applications in the industrial, instrumentation, computer peripherals, communications, automotive, and military markets. Siliconix serves these markets with products of unequalled performance, quality and reliability through the use of its leading design, processing, packaging, and testing technologies.

The product specifications listed in this data book are arranged in a simplified format. The electrical tables and performance curves contain detailed information, simplifying the tasks of design and component engineers. Each of the data sheets is controlled by the Siliconix Quality Assurance organization, which guarantees all stated limits.

### For More Information

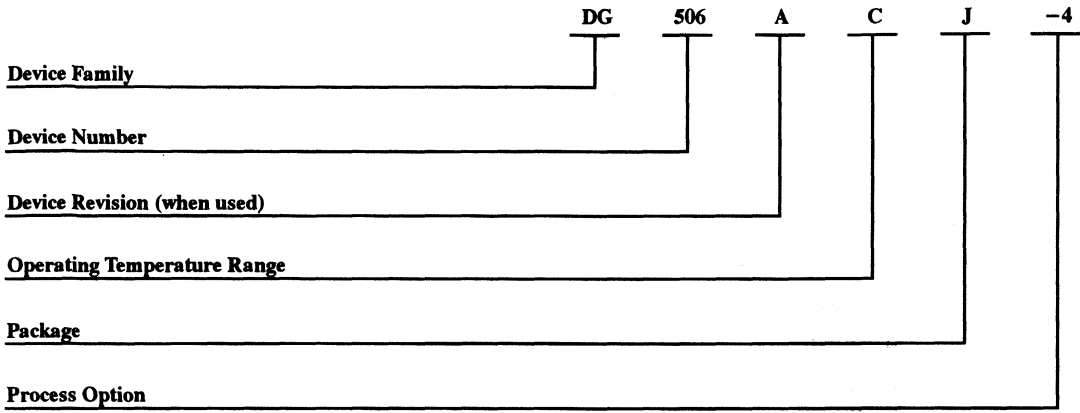
To request additional literature please call 1-800-554-5565. Literature and samples can also be requested from our sales representatives. See the sales office listings in Section 6.

Customer service representatives are available during normal West Coast business hours to provide information on orders placed with the factory.

### For Technical Support

In addition to the individual data sheets, which provide Application Hints, Siliconix offers a number of Applications Notes and Technical Articles to help you with your designs. Please refer to the Application Note listing in Section 5, and use our FaxBack system 408-970-5600 to obtain copies.

## Integrated Circuits Nomenclature



### Device Family

(1 or 2 Letters)

- DG — Analog Switches and Analog Multiplexers
- Si — Siliconix Integrated Circuits

### Device Number

(3- or 4-Digit Numbers)

### Operating Temperature Range

(1 Letter)

- A — -55 to 125°C
- B — -25 to 85°C
- C — 0 to 70°C
- D — -40 to 85°C
- E — -40 to 105°C

### Package

(1 Letter)

- A — Metal Can
- J — Dual-In-Line Package — Plastic DIP
- K — Dual-In-Line Package — Ceramic DIP
- L — Flat Package
- M — CerQuad J-Leaded Chip Carrier
- N — Plastic J-Leaded Chip Carrier — PLCC
- P — Dual-In-Line Package — Sidebrazed
- R — Dual-In-Line Package — Sidebrazed
- W — Wide-Body Small-Outline Package (SOIC)
- Y — Narrow-Body Small-Outline Package (SOIC)
- Z — Leadless Chip Carrier — LCC

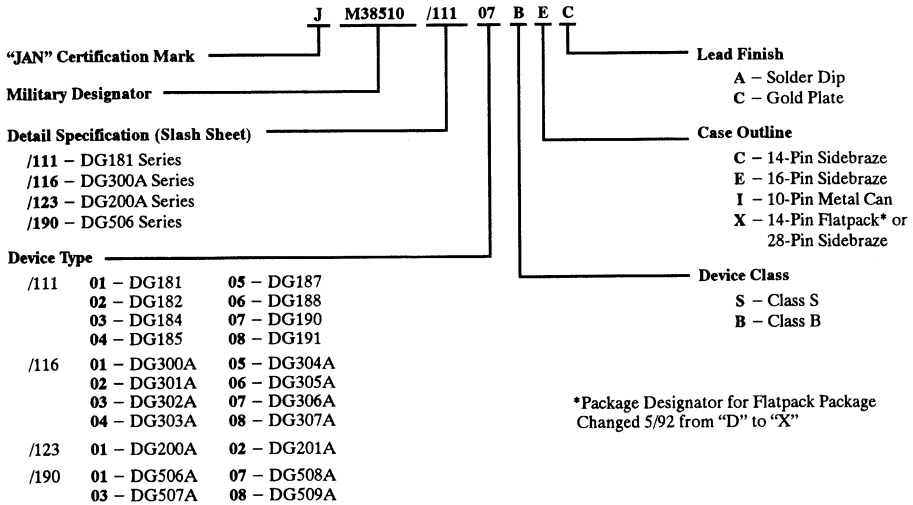
### Process Option

- /883 — Processing to the current revision of MIL-STD-883, Level B. Compliant Non-JAN
- 4 — Ruggedized Plastic Flow

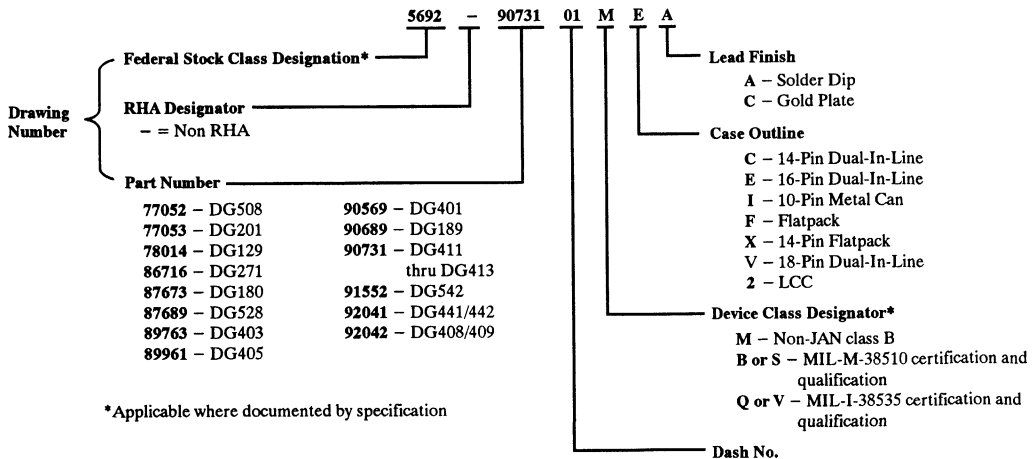
All possible combinations of device types, temperature ranges, package types and MIL-883 process options are not necessarily available. Consult individual data book pages or sales office for complete information.

## Military Nomenclature

### MIL-M-38510



### Standard Military Drawing



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# About Analog Switches

Siliconix is the world's leading supplier of high-performance, precision solid-state analog switches. For more than twenty years, we've combined new technologies with our experience and expertise to produce new families of leading-edge products.

Our DG4XX and DG6XX families of analog switches and multiplexers are one way Siliconix maintains its high reputation for innovation. These new devices can be used to upgrade existing products or to open new doors to high-performance analog switching. The DG4XX family includes all the most popular functions—SPST, SPDT, and DPST—in single and dual switch configurations, along with several SPST quads. Packaging options include both plastic and ceramic DIP, mini DIP, PLCC, and plastic SOIC packages for surface-mount assembly. These are available in both industrial ( $-40$  to  $86^{\circ}\text{C}$ ) and military ( $-55$  to  $125^{\circ}\text{C}$ ) temperature ranges. The growing DG6XX series goes even further, giving you the fastest switching times and lowest on-resistance available. The DG641/DG642, for example, are the industry's first analog switches with on-resistance below  $10\ \Omega$ , while the DG611/612/613 achieve switching speeds of 15 ns.

The DG2XX, DG3XX, and DG5XX families provide adequate performance for many applications. Siliconix also offers its popular JFET (DG18X) family of switches. Single-supply operation, charge injection optimization, and a wide range of packaging options, including small outline and PLCC, are additional benefits.

## CMOS

Since CMOS analog switches are parallel combinations of p- and n-channel MOSFETs, the effective on-resistance is a combination of the PMOS and NMOS resistance curves (Figure 2). This gives a fairly constant on-resistance over the entire analog voltage range. New CMOS switches also have the advantage of very low quiescent supply current because, other than for channel leakage, no current flows in the driver except when a control input transition occurs.

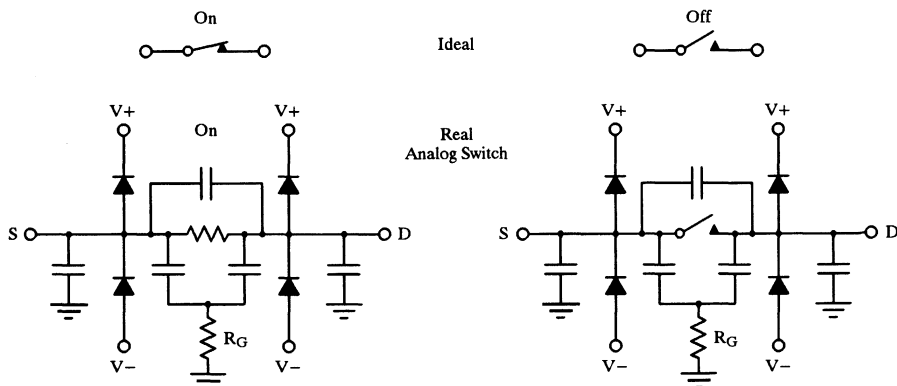


Figure 1. Comparison of the "Ideal" Switch to a Solid-State Analog Switch



## Metal-Gate and Silicon-Gate CMOS

Both metal- and silicon-gate technologies are incorporated into our CMOS processes, but each is used with separate product lines. The mature metal-gate process is used for our DG2XX, DG3XX, and DG5XX families. Our newer silicon-gate process (DG4XX family) is recommended for applications needing state-of-the-art performance and versatility.

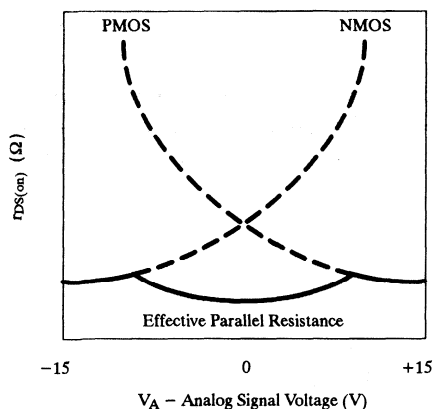
Figure 3 gives a comparison of on-resistance curves for a JFET (DG180), a D/CMOS (DG642), a metal-gate CMOS (DG201A), and a silicon-gate CMOS (DG400) analog switch.

## D/CMOS “T” Switches

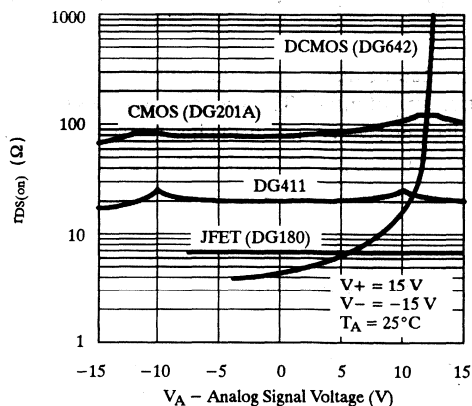
Siliconix manufactures analog switches and multiplexers for wideband/video applications using double-diffused MOS (DMOS) technology. DMOS FETs are n-channel enhancement-mode MOSFETs which exhibit very low capacitance and on-resistance compared to conventional CMOS devices. The result is wide bandwidth switches which feature crosstalk and off-isolation performance as high as 100 dB at 5 MHz and 3 dB bandwidths in excess of 500 MHz. These devices are ideal for broadcast video, digital data routing, high-end workstation networks and imaging applications from medical to military. The DG54x family of wideband/video “T” switches includes the DG540, DG541 and DG542 devices. The DG61X family of high-speed non-T switches boast 15-ns switching times. The DG64X family offers very low on-resistance.

## Important Switch Parameters

Each switch family in the Siliconix product line has a set of optimized characteristics that make it suitable for certain types of applications. Several major specifications should be compared and prioritized before selecting an analog switch for a particular circuit.



**Figure 2.** Graph of CMOS Switch Resistance vs. Analog Signal



**Figure 3.** On-Resistance for Several Analog Switch Technologies

## **On-Resistance ( $r_{DS(on)}$ )**

This specification is the dc resistance of the channel when the analog switch is in the on state. The on-resistance of an analog switch depends upon the device type and the analog signal magnitude. Although the resistance may vary across the entire analog signal range, the worst case is normally specified on the data sheet.

## **Switching Speed**

Switching speed is the elapsed time from the application of the control signal on the input pin to the appearance (or disappearance) of the analog signal at the output. Switching speed can be affected by the load on the analog switch. Each data sheet shows a switching time test circuit with a standard load for comparison purposes.

## **Switch Current**

The amount of current that can be fed through the switch channel is sometimes important. For example, the DG411 can handle up to 100 mA of pulsed current or 30 mA of continuous current, while the DG180 can handle up to 200 mA of continuous current.

## **Break-Before-Make vs. Make-Before-Break**

For most analog switch applications, break-before-make switching is desired. Because it is often necessary to disconnect one signal source before connecting another to avoid source crosstalk. However, make-before-break switching is critical in some control circuits, such as the feedback resistor gain selector for programmable gain op amps, to avoid opening the loop.

## **Electrostatic Discharge Sensitivity (ESDS)**

Electrostatic discharge is the transfer of charge that occurs when an object makes contact with a device at a different potential. The standard MIL-883C, method 3015, classifies three levels of voltage protection that a device must withstand on all pins. Class 1 devices are protected to 1999 V, Class 2 from 2000 to 3999 V, and Class 3 protection is greater than 4000 V. Beginning with DG411 series, most of our new devices have Class 2 ratings and are marked accordingly.

## **Charge Injection**

Charge injection is the transfer of charge to a load from the driver to the FET channels during switching. In a sample-and-hold circuit, charge injection is critical as the charge added or subtracted from the holding capacitor is seen as an offset error. The lower the charge injection the better. The DG4XX family, especially the DG441 and DG411 series, are designed for balanced (linear and crossing near zero) charge injection. The DG601 and DG611 use internal compensation to minimize the charge injection seen by applications sensitive to this parameter.

## Power Supplies and Power Consumption

A bipolar supply means positive and negative voltages are used, while single supply means the negative supply is grounded. Most analog designs use bipolar supplies, but a growing number of designers are turning to single-supply operation to save board space and cost. Most of our devices work well with bipolar supplies, but not all function properly in the single supply mode. The DG4XX family for analog switches and multiplexers not only functions superbly in a single-supply mode, but it is fully characterized and specified with V+ at 12 V and V- at GND. The less the power consumed by a device within a system the better. Some members of the DG4XX family draw under 1  $\mu$ A of supply current compared to the milliamperes required by previous products.

## Interfacing



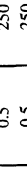
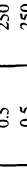
The two most common logic families are TTL and CMOS. The standard logic levels for both families are displayed in Table 1. Not all analog switches are compatible with both types of logic. Refer to the functional diagram section for each data sheet to determine the required logic levels.

Microprocessor compatibility is a growing concern when designing with analog switches. Standard analog switches require a constant control signal present on the input to hold the switch in the desired position (on or off). This could tie up a microprocessor control system unless external latches are added to control the switch. The DG42X series has incorporated these latches, complete with control logic, on board to minimize parts count and ease interface to microprocessor-based control systems.




Table 1. Logic Levels for TTL and CMOS Compatibility

Logic	TTL	CMOS
0	$\leq 0.8$ V	$\leq 1.5$ V
1	$\geq 2.4$ V	$\geq (V_{CC} - 1.5$ V)

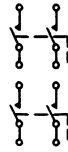
# Analog Switch Selector Guide

Functional Configuration	Part Number	Max $r_{DS(on)}$ ( $\Omega$ )	Max $I_{S(ON)}$ (mA)	Max $t_{ON}$ (ns)	Typ $Q_{int}$ (pC)	Max Supply Range (V)	On-Chip Logic Regulator	Max Power Consumption (mW)	Package	Comments	Page
1-Channel SPST 	DG417	35	0.25	175	60	44	-	0.035	J, K, Y	8-Pin Package	1-146
	DG418	35	0.25	175	60	44	-	0.035	J, K, Y	8-Pin Package	1-146
2-Channel SPST 	DG180	10	10	400	N/A	36	-	120	A, P, X	JFET	1-4
	DG181	30	1	150	N/A	36	-	120	A, P, X	JFET	1-4
	DG401	35	0.25	150	80	44	-	0.035	J, K, Z	-	1-127
	DG421	35	0.25	250	80	44	-	0.035	J, K	Latches	1-155
	DG300A	50	1	300	8	44	-	7.65	A, J, K, P	-	1-90
	DG304A	50	1	250	30	44	-	0.3	A, J, K, P	-	1-99
4-Channel SPST 	DG381A	50	1	300	10	44	-	7.65	J	-	1-119
	DG200A	70	2	1000	-10	44	Yes	60	A, J, K	-	1-32
	DG182	75	1	250	N/A	36	-	120	A, P, X	JFET	1-4
	DG641	15	10	70	-19	21	Yes	108	J, Y	Video	1-208
	DG411	35	0.25	175	5	44	-	0.035	J, K, Y, Z	-	1-137
	DG412	35	0.25	175	5	44	-	0.035	J, K, Y, Z	-	1-137
	DG413	35	0.25	175	5	44	-	0.035	J, K, Y, Z	-	1-137
	DG601	35	4	45	13	22	Yes	180	J, K, Y, Z	High Speed	1-189
	DG271	50	1	65	9	44	Yes	225	J, K, Y, Z	High Speed	1-85
	DG201HS	50	1	50	5	44	Yes	240	J, K, Y, Z	High Speed	1-52
	DG540	60	10	70	-25	21	Yes	108	J, N, P	Video	1-179
	DG541	60	10	70	-25	21	Yes	108	J, P, Y	Video	1-179
4-Channel SPST 	DG611	60	0.25	35	1	21	-	0.018	J, K, Y, Z	Glitchless, High Speed	1-200
	DG612	60	0.25	35	1	21	-	0.018	J, K, Y, Z	Glitchless, High Speed	1-200
	DG613	60	0.25	35	1	21	-	0.018	J, K, Y, Z	Glitchless, High Speed	1-163
	DG201B	85	0.5	300	1	44	Yes	0.765	J, K, Y	-	1-44
	DG202B	85	0.5	300	1	44	Yes	0.765	J, K, Y	-	1-44
	DG211B	85	0.5	300	1	44	-	0.35	J, Y	General Purpose	1-68
	DG212B	85	0.5	300	1	44	-	0.35	J, Y	General Purpose	1-68
	DG308B	85	0.5	200	1	44	-	0.03	J, K, Y	General Purpose	1-200
	DG309B	85	0.5	200	1	44	-	0.03	J, K, Y	General Purpose	1-200
	DG441	85	0.5	250	1	44	Yes	1.5	J, K, Y	-	1-163
	DG442	85	0.5	250	1	44	Yes	1.5	J, K, Y	-	1-163
	DG444	85	0.5	250	1	44	-	0.035	J, Y	-	1-171
DG445	85	0.5	250	1	44	-	0.035	J, Y	-	1-171	

# Analog Switch Selector Guide (Cont'd)

Functional Configuration	Part Number	Max $r_{DS(on)}$ ( $\Omega$ )	Max $I_{S(off)}$ (mA)	Max $t_{ON}$ (ns)	Typ $Q_{ch}$ (pC)	Max Supply Range (V)	On-Chip Logic Regulator	Max Power Consumption (mW)	Package	Comments	Page
4-Channel SPST 	DG221	90	1	550	20	44	Yes	37.5	J, K, Y	Latches	1-75
	DG308A	100	1	200	-10	44	-	0.3	J, K, Y	-	1-107
	DG309	100	1	200	-10	44	-	0.3	J, Y	-	1-107
	DG201A	175	1	600	20	44	Yes	60	J, K, Y, Z	-	1-37
	DG202	175	1	600	20	44	Yes	60	J, K	-	1-37
	DG211	175	5	1000	3	44	-	20.4	J, Y	-	1-60
DG212	175	5	1000	3	44	-	20.4	J, Y	-	1-60	
1-Channel SPDT 	DG642	8	10	100	-40	21	Yes	108	J, Y	Video	1-208
	DG186	10	10	400	N/A	38	-	73	A, P	JFET	1-18
	DG301A	50	1	300	8	44	-	0.3	A, J, K, Z	-	1-90
	DG187	30	1	150	N/A	38	-	73	A, P, X	JFET	1-18
	DG419	35	0.25	175	60	44	-	0.035	J, K, Y	8-Pin Package	1-146
	DG305A	50	1	250	30	44	-	0.3	A, K, P	-	1-99
	DG387A	50	1	300	10	44	-	7.65	A, J, K	-	1-119
	DG188	75	1	250	N/A	38	-	73	A, P, X	JFET	1-18
	DG189	10	10	400	N/A	36	-	120	P	JFET	1-25
	DG643	15	10	70	-19	21	-	108	J, Y	Video	1-208
2-Channel SPDT 	DG190	30	1	150	N/A	36	-	120	P, X	JFET	1-25
	DG403	35	0.25	150	60	44	-	0.035	J, K, Y, Z	-	1-127
	DG423	35	0.25	250	60	44	-	0.035	J, K, N	Latches	1-155
	DG243	50	1	500	60	44	-	0.45	J, N	Latches	1-81
	DG303A	50	1	300	8	44	-	7.65	J, K, P, Z	-	1-90
	DG307A	50	1	250	30	44	-	0.3	J, K, P, Z	-	1-99
	DG390A	50	1	300	10	44	-	7.65	J, K	-	1-119
	DG5043	50	1	1200	30	44	-	9	J	-	1-218
	DG5143	50	0.5	200	60	44	-	0.035	J, K	-	1-221
	DG542	60	10	100	-25	21	Yes	108	J, P, Y	Video	1-179
DG191	75	1	250	N/A	36	-	120	P, X	JFET	1-25	

# Analog Switch Selector Guide (Cont'd)

Functional Configuration	Part Number	Max $r_{DS(on)}$ (Ω)	Max $I_S(off)$ (mA)	Max $t_{ON}$ (ns)	Typ $Q_{int}$ (pC)	Max Supply Range (V)	On-Chip Logic Regulator	Max Power Consumption (mW)	Package	Comments	Page
2-Channel DPST 	DG183	10	10	400	N/A	36	-	120	P	JFET	1-11
	DG184	30	1	150	N/A	36	-	120	P, X	JFET	1-11
	DG405	35	0.25	150	60	44	-	0.035	J, K, Y, Z	-	1-127
	DG425	35	0.25	250	60	44	-	0.035	J	Latches	1-155
	DG302A	50	1	300	8	44	-	7.65	J, K, P	-	1-90
	DG306A	50	1	250	30	44	-	0.3	J, K, P	-	1-99
	DG384A	50	1	300	10	44	-	7.65	J, K	-	1-119
	DG185	75	1	250	N/A	36	-	120	P, X	JFET	1-11

A = Metal Case  
P = Sidebreak

K = CerDIP  
Y = SOIC

N = PLCC  
Z = LCC

# Analog Switch—Switching Speed vs. $r_{DS(on)}$

$r_{DS(on)}$ (Max Ω)	$t_{ON}$ (Max) or $t_{OFF}$ (Max), Whichever is Greater										
	20/35 ns	60/75 ns	125/150 ns	200 ns	250 ns	300 ns	500/600 ns	1 μs			
175							DG201A	DG202	DG211	DG212	
100			DG441 DG442	DG444 DG445	DG308A DG309A	DG485 DG894	DG221				
85					DG308B	DG309B		DG201B DG202B	DG211B DG212B	DG200A	
60	DG611 DG612	DG540 DG541									
50		DG271	DG201HS		DG5143	DG304A DG305A	DG306A DG307A	DG300A DG301A DG302A DG303A	DG381A DG384A DG387A DG390A	DG243	DG5043
35 to 25		DG601	DG181 DG184 DG187 DG190 DG401 DG403	DG405 DG411 DG412 DG413 DG417 DG418							
15		DG641	DG643								
10		DG642						DG180 DG183 DG186 DG189	DG180 DG183 DG186 DG189		

# Analog Switch—Power Consumption vs. $r_{DS(on)}$

Maximum Power Consumption						
$r_{DS(on)}$ (Max. $\Omega$ )	0.018 mW	0.035 mW	0.1 to 1.5 mW	5 to 40 mW	60 to 140 mW	180 to 240 mW
175				DG211 DG212	DG201A DG202	
100		DG444 DG445	DG308A DG309A DG441	DG442 DG485	DG894 DG894	
85		DG308B DG309B	DG201B DG202B	DG211B DG212B	DG182 DG185 DG188	DG191 DG200A
60	DG611 DG612				DG540 DG541	DG542
50		DG5143	DG243 DG304A DG305A	DG306A DG307A	DG201HS	DG271
35 to 25		DG401 DG403 DG405 DG411 DG412 DG413		DG300A DG301A DG302A DG303A	DG381A DG384A DG387A DG5043	DG181 DG184 DG187 DG190
15					DG641	DG601
10					DG180 DG183 DG188	DG189 DG642 DG643





# Dual DPST JFET Analog Switch

## Features

- Standby Power: <1 mW
- Bipolar Drivers
- Constant  $r_{DS(on)}$  Over Signal Range
- Off Isolation: > 60 dB @ 1 MHz
- Make-Before-Break

## Benefits

- Minimizes Standby Power Requirements
- Better Radiation Tolerance
- Less Distortion
- Higher Frequency Switching
- Smooth Closed Loop Response

## Applications

- Battery Powered Systems
- Aerospace Control Systems
- Low Distortion Circuits
- High Frequency Switching Circuits

## Description

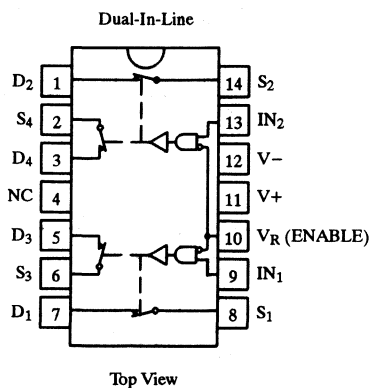
The DG129 is a dual double-pole single-throw analog switch for use in instrumentation, control, and audio communication systems. It is ideally suited for applications requiring a constant on-resistance over the entire analog range.

On-resistance for the DG129 is 20  $\Omega$  (typical), and on-leakage is < 2 nA. With all switches off, total power consumption is < 750  $\mu$ W. These switches have make-before-break action and due to the processing are relatively radiation tolerant. An

enable pin ( $V_R$ ) simplifies interfacing with microprocessor, or other logic.

Each device contains four junction field-effect transistors (JFETs) to achieve constant on-resistance. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the on-off state of each switch. With logic "0" at the driver input the switches will be off. With a logic "1" at the input the switches will be on. In the on-state each switch will conduct current in either direction, and in the off-state each switch will block voltages up to 20 V peak-to-peak.

## Functional Block Diagram and Pin Configuration



Four SPST Switches per Package

Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq$  0.8 V  
Logic "1"  $\geq$  2.5 V

Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
-55 to 125°C	14-Pin Sidebrazed	DG129AP/883
		781401CA

1

## Absolute Maximum Ratings

V+ to V-	36 V
V+ to V <sub>D</sub>	36 V
V <sub>D</sub> or V <sub>S</sub> to V-	36 V
V <sub>D</sub> to V <sub>S</sub>	±22 V
V+ to V <sub>R</sub>	25 V
V <sub>R</sub> to V-	25 V
V <sub>IN</sub> to V-	30 V
V+ to V <sub>IN</sub>	25 V

V <sub>IN</sub> to V <sub>R</sub>	±6 V
Current (any terminal)	30 mA
Storage Temperature	-65 to 150°C
Power Dissipation <sup>a</sup>	
14-Pin DIP <sup>b</sup>	825 mW

**Notes:**

- a. All leads welded or soldered to PC Board.
- b. Derate 11 mW/°C above 75°C

## Specifications<sup>a</sup>

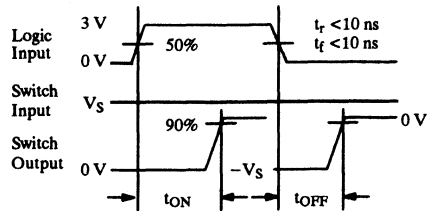
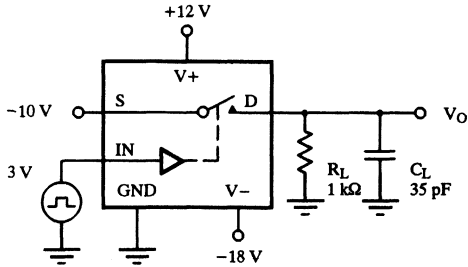
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V- = -18 V, V <sub>R</sub> = 0 V, V <sub>IN</sub> = 0.8 V or 2.5 V <sup>f</sup>	Temp <sup>b</sup>	A Suffix -55 to 125°C			Unit
				Min <sup>d</sup>	Typ <sup>c</sup>	Max <sup>d</sup>	
<b>Switch</b>							
Analog Signal Range	V <sub>ANALOG</sub>		Full	-10		10	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = 10 V	Room Full		20	30 60	Ω
Source-Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V	Room Full	-1 -100	0.03	1 100	nA
Drain-Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = ±10 V, V <sub>S</sub> = ∓10 V	Room Full	-1 -100	0.02	1 100	
Channel-On Leakage Current	I <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = -10 V	Room Full	-2 -100	-0.03		
<b>Input</b>							
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2.5 V	Room Full		15	60 120	μA
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0.8 V	Room Full		0.005	0.1 2	
<b>Dynamic</b>							
Turn-On Time	t <sub>ON</sub>	See Figure 1	Room		0.5	0.6	μs
Turn-Off Time	t <sub>OFF</sub>		Room		1.1	1.6	
Source-Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz V <sub>D</sub> , V <sub>S</sub> = 0	Room		2.4		pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room		2.4		
Channel-On Capacitance	C <sub>D(on)</sub>		Room		2.8		
Off-Isolation	OIRR	R <sub>L</sub> = 75 Ω, f = 1 MHz	Room		> 60		dB
<b>Supply</b>							
Positive Supply Current	I+	One Channel On V <sub>IN</sub> = 2.5 V	Room		2.5	3	mA
Negative Supply Current	I-		Room	-1.8	-1.6		
Reference Supply Current	I <sub>R</sub>		Room	-1.4	-1.1		
Positive Supply Current	I+	All Channel Off Both V <sub>IN</sub> = 0 V	Room		0.6	25	μA
Negative Supply Current	I-		Room	-25	-0.5		
Reference Supply Current	I <sub>R</sub>		Room	-25	-0.5		

**Notes:**

- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = -55 to 125°C.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. V<sub>IN</sub> = input voltage to perform proper function.

**Test Circuits**

Switch output waveform shown for  $V_S =$  constant with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Logic "1" = Switch On

**Figure 1. Switching Time**

**Application Hints**

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	VR Reference Voltage (V)	VIN Logic Input Voltage VINH(min)/VIL(max) (V)	VS or VD Analog Voltage Range (V)
12	-18	0	2.5/0.8	-10 to 10
15	-15	0	2.5/0.8	-7 to 13
7	-12	0	2.5/0.8	-5 to 5
5	-15	0	2.5/0.8	-7 to 3
5	-10	0	2.5/0.8	-2 to 3

## High-Speed Drivers with Dual SPST JFET Switches

### Features

- Constant On-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Rad Hardness

### Benefits

- Low Distortion
- Eliminates Large Signal Errors
- High Precision
- High Bandwidth Capability
- Fault Protection

### Applications

- Audio Switching
- Video Switching
- Sample/Hold
- Guidance and Control Systems
- Aerospace

### Description

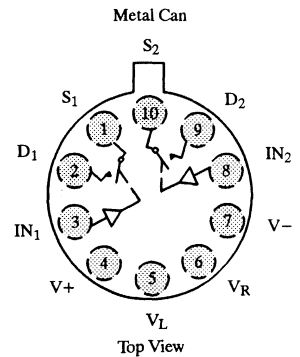
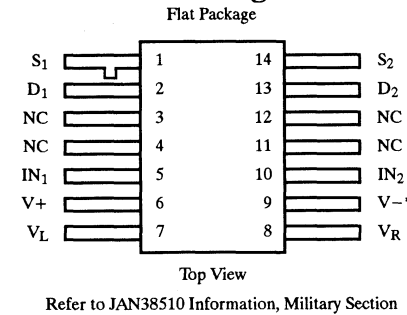
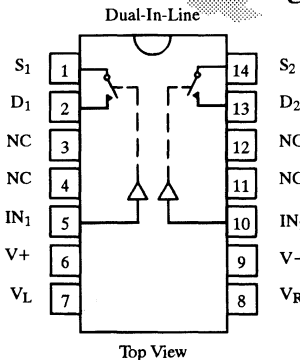
The DG180/181/182 are precision dual single-pole, single-throw (SPST) analog switches designed to provide accurate switching of video and audio signals. This series is ideally suited for applications requiring a constant on-resistance over the entire analog range.

The major difference in the devices is the on-resistance (DG180—10 Ω, DG181—30 Ω, DG182—75 Ω). Reduced errors are achieved through low leakage current ( $I_{p(on)} < 2$  nA). Applications which benefit from the flat JFET

on-resistance include audio switching, video switching, and data acquisition.

To achieve fast and accurate switch performance, each device comprises four n-channel JFET transistors and a TTL compatible bipolar driver. In the on state, each switch conducts current equally well in either direction. In the off condition, the switches will block up to 20 V peak-to-peak, with feedthrough of less than -60 dB at 10 MHz.

### Functional Block Diagram and Pin Configuration



#### Ordering Information – DG180/181/182

Temp Range	Package	Part Number
-25 to 85°C	10-Pin Metal Can	DG180BA
		DG181BA
		DG182BA
	14-Pin Sidebrazed	DG180BP
		DG181BP
		DG182BP
-55 to 125°C	10-Pin Metal Can	DG180AA/883, 5962-87673011A
		DG181AA/883, JM38510/11101B1A
		DG182AA/883, JM38510/11102B1A
	14-Pin Sidebrazed	DG180AP/883, 5962-8767301CA
		DG181AP/883, JM38510/11101B1CA
		DG182AP/883, JM38510/11102B1CA
	14-Pin Flat Pack	5962-8767301XA
		JM38510/11101B1XA
		JM38510/11102B1XA

\*Common to Substrate and Case

#### Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.0 V

Switches Shown for Logic "1" Input

## Absolute Maximum Ratings

V+ to V-	36 V
V+ to V <sub>D</sub>	33 V
V <sub>D</sub> to V-	33 V
V <sub>D</sub> to V <sub>D</sub>	±22 V
V <sub>L</sub> to V-	36 V
V <sub>L</sub> to V <sub>IN</sub>	8 V
V <sub>L</sub> to V <sub>R</sub>	8 V
V <sub>IN</sub> to V <sub>R</sub>	8 V
V <sub>R</sub> to V-	27 V
V <sub>R</sub> to V <sub>IN</sub>	2 V
Current (S or D) DG180	200 mA

Current (S or D) DG181, DG182	30 mA
Current (All Other Pins)	30 mA
Storage Temperature	-65 to 150°C
Power Dissipation <sup>a</sup>	
10-Pin Metal Can <sup>b</sup>	450 mW
14-Pin Sidebrazed <sup>c</sup>	825 mW
14-Pin Flat Pack <sup>d</sup>	900 mW

Notes:

- a. All leads welded or soldered to PC Board.
- b. Derate 6 mW/°C above 75°C
- c. Derate 11 mW/°C above 75°C
- d. Derate 10 mW/°C above 75°C

## Specifications<sup>a</sup> for DG180

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V, V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V, V <sub>IN</sub> = 2 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-7.5	15	-7.5	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = -7.5 V	Room Full	7.5		10 20		15 25	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		10 1000		15 300	nA
		V <sub>S</sub> = ±7.5 V, V <sub>D</sub> = ∓7.5 V	Room Hot	0.05		10 1000		15 300	
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		10 1000		15 300	nA
		V <sub>S</sub> = ±7.5 V, V <sub>D</sub> = ∓7.5 V	Room Hot	0.03		10 1000		15 300	
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = ±7.5 V	Room Hot	-0.1	-2 -200		-10 -200		nA
Saturation Drain Current	I <sub>DSS</sub>	2 ms Pulse Duration	Room	300					mA
<b>Digital Input</b>									
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	Room Hot	<0.01		10 20		10 20	μA
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Full	-30	-250		-250		μA
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>on</sub>	See Switching Time Test Circuit	Room	240		400		600	ns
Turn-Off Time	t <sub>off</sub>		Room	140		200		250	
Source-Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz	Room	21					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		V <sub>S</sub> = -5 V, I <sub>D</sub> = 0 V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	Room	17				
Channel-On Capacitance	C <sub>D(on)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	Room	17				
Off Isolation	OIRR	f = 1 MHz, R <sub>L</sub> = 75 Ω	Room	>55					dB
<b>Power Supplies</b>									
Positive Supply Current	I+	V <sub>IN</sub> = 0 V, or 5 V	Room	0.6		1.5		1.5	mA
Negative Supply Current	I-		Room	-2.7	-5		-5		
Logic Supply Current	I <sub>L</sub>		Room	3		4.5		4.5	
Reference Supply Current	I <sub>R</sub>		Room	-1	-2		-2		



## Specifications<sup>a</sup> for DG181

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, V_L = 5\text{ V}$ $V_R = 0\text{ V}, V_{IN} = 2\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-7.5	15	-7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = -7.5\text{ V}$	Room Full	18		30 60		50 75	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.05		1 100		5 100	nA
		$V_S = \pm 7.5\text{ V}, V_D = \mp 7.5\text{ V}$	Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.5		1 100		5 100	
		$V_S = \pm 7.5\text{ V}, V_D = \mp 7.5\text{ V}$	Room Hot	0.6		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 7.5\text{ V}$	Room Hot	-0.02	-2 -200		-10 -200		
<b>Digital Input</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Hot	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{on}$	See Switching Time Test Circuit	Room	85		150		180	ns
Turn-Off Time	$t_{off}$		Room	95		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		$V_S = -5\text{ V}, I_D = 0$	Room	6				
Channel-On Capacitance	$C_{D(on)}$		$V_D = -5\text{ V}, I_S = 0$	Room	14				
Off Isolation	OIRR	f = 1 MHz, $R_L = 75\ \Omega$	Room	>50					dB
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V}, \text{ or } 5\text{ V}$	Room	0.6		1.5		1.5	mA
Negative Supply Current	$I_-$		Room	-2.7	-5		-5		
Logic Supply Current	$I_L$		Room	3.1		4.5		4.5	
Reference Supply Current	$I_R$		Room	-1	-2		-2		

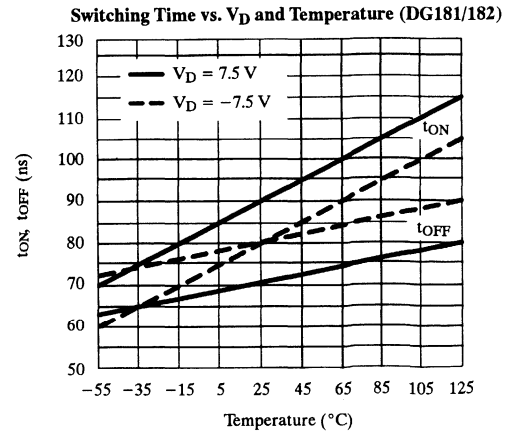
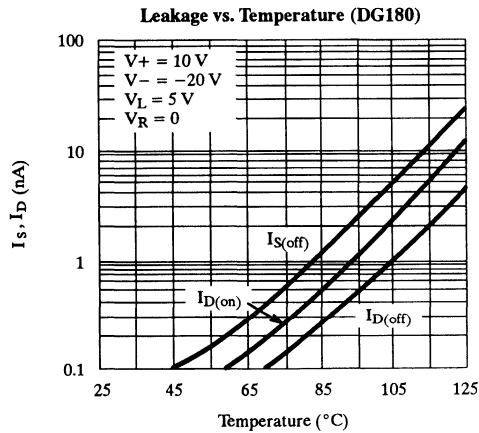
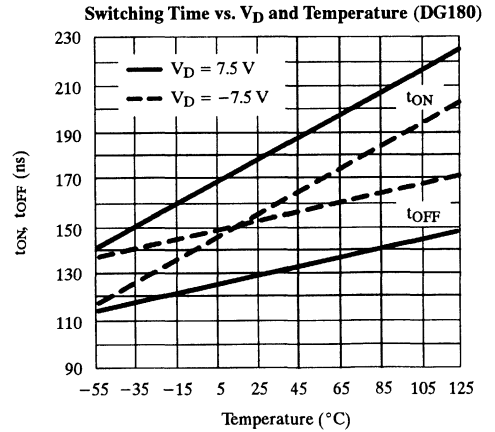
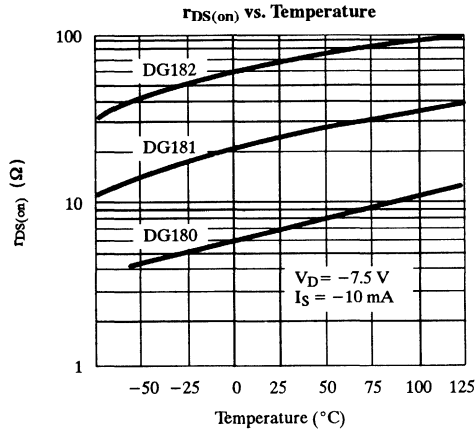
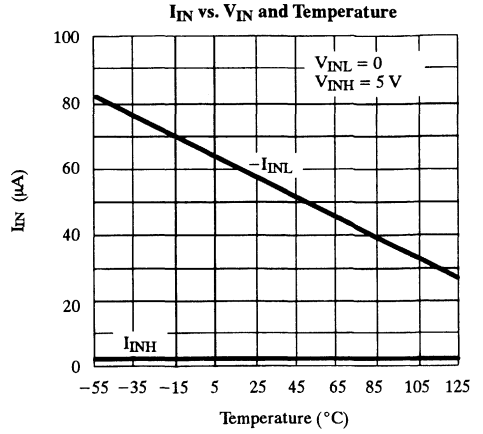
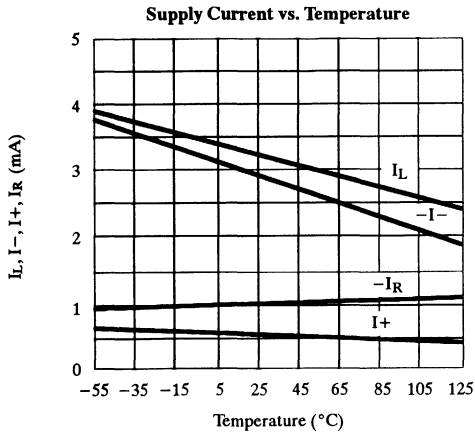
**Specifications<sup>a</sup> for DG182**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, V_L = 5\text{ V}$ $V_R = 0\text{ V}, V_{IN} = 2\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-10	15	-10	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = -7.5\text{ V}$	Room Full	35		75 150		100 150	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.05		1 100		5 100	nA
		$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$	Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.4		1 100		5 100	
		$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$	Room Hot	0.5		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 10\text{ V}$	Room Hot	-0.02	-2 -200		-10 -200		
<b>Digital Input</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Hot	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{on}$	See Switching Time Test Circuit	Room	120		250		300	ns
Turn-Off Time	$t_{off}$		Room	100		130		150	
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		$V_S = -5\text{ V}, I_D = 0$	Room	6				
Channel-On Capacitance	$C_{D(on)}$		$V_D = -5\text{ V}, I_S = 0$	Room	14				
Off Isolation	OIRR	$f = 1\text{ MHz}, R_L = 75\ \Omega$	Room	>50					dB
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V}, \text{ or } 5\text{ V}$	Room	0.6		1.5		1.5	mA
Negative Supply Current	$I_-$		Room	-2.7	-5		-5		
Logic Supply Current	$I_L$		Room	3.1		4.5		4.5	
Reference Supply Current	$I_R$		Room	-1	-2		-2		

**Notes:**

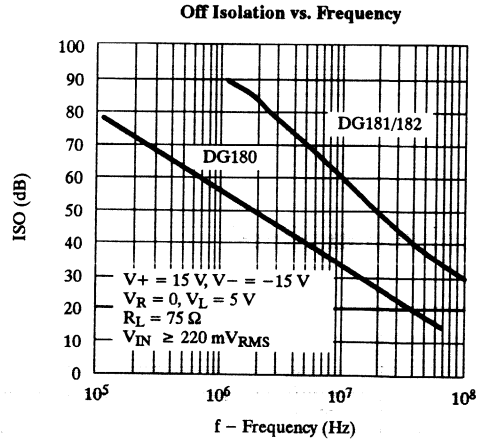
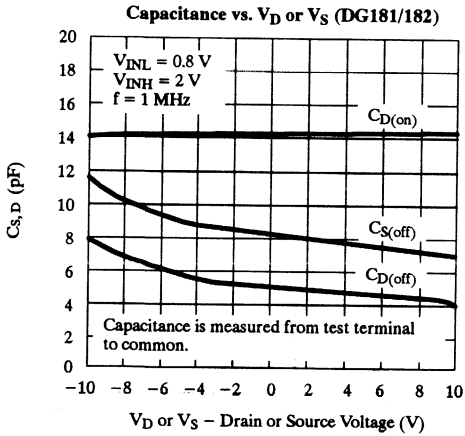
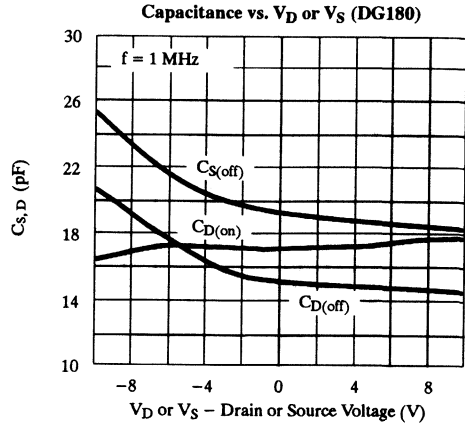
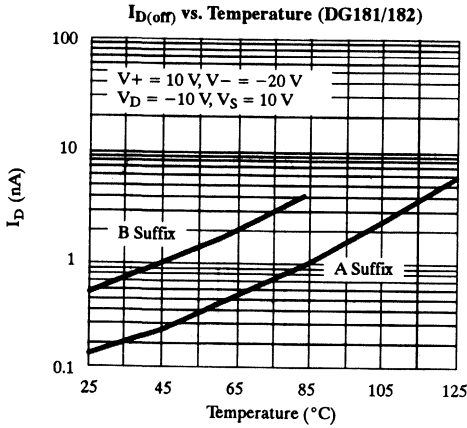
- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

## Typical Characteristics

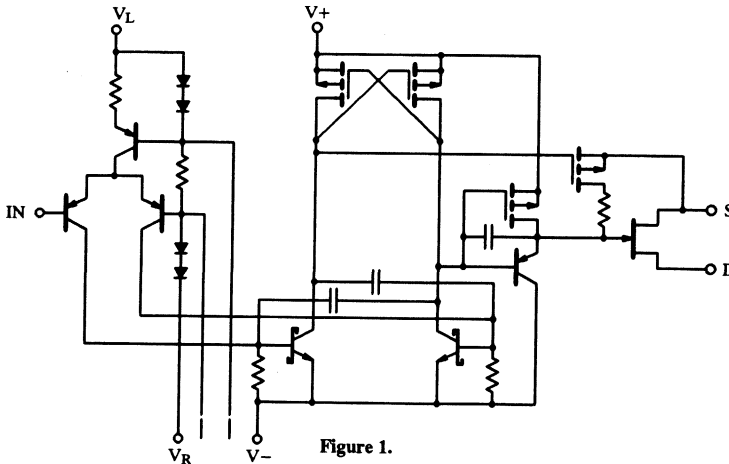




**Typical Characteristics (Cont'd)**



**Schematic Diagram (Typical Channel)**



## Test Circuits

Feedthrough due to charge injection may result in spikes at the leading and trailing edge of the output waveform.

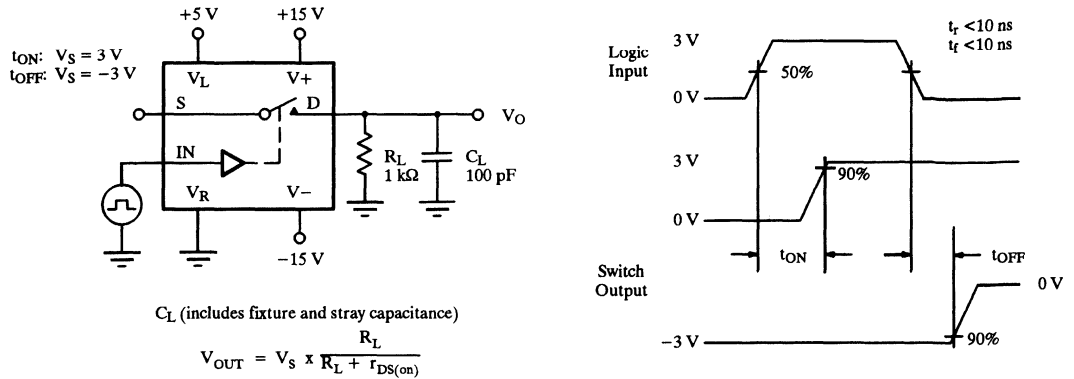


Figure 2. Switching Time

## Application Hints<sup>a</sup>

Switch	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>L</sub> Logic Supply Voltage (V)	V <sub>R</sub> Reference Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> / V <sub>INL(max)</sub> (V)	V <sub>S</sub> Analog Voltage Range (V)
DG180 DG181	15 <sup>b</sup>	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
DG182	15 <sup>b</sup>	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

**Notes:**

- a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- b. Electrical Parameter Chart based on V+ = 15 V, V<sub>L</sub> = 5 V, V<sub>R</sub> = GND

## High-Speed Drivers with Dual DPST JFET Switches

### Features

- Constant On-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Break-Before-Make Switching
- Rad Hardness

### Benefits

- Low Distortion
- Eliminates Large Signal Errors
- High Precision
- Improved Channel Isolation
- Eliminates Inadvertent Shorting Between Channels
- Fault Protection

### Applications

- Audio Switching
- Precision Switching
- Video Switching
- Video Routing
- Sample/Hold
- Aerospace

### Description

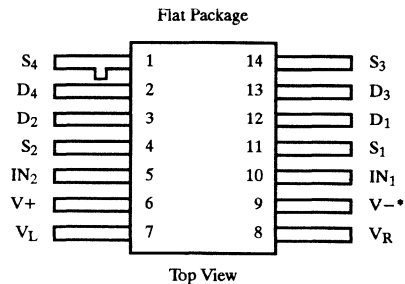
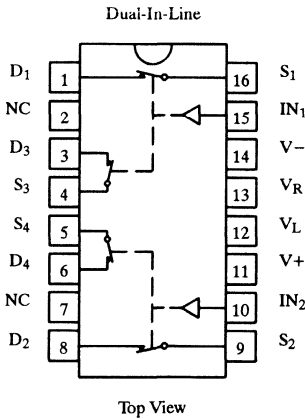
The DG183/184/185 are precision dual double-pole, single-throw (DPST) analog switches designed to provide accurate switching of video and audio signals. This series is ideally suited for applications requiring a constant on-resistance over the entire analog range.

The major difference in the devices is the on-resistance (DG183—10 Ω, DG184—30 Ω, DG185—75 Ω). Reduced errors are achieved through low leakage current ( $I_{D(on)} < 2 \text{ nA}$ ). Applications which benefit from the flat JFET

on-resistance include audio switching, video switching, and data acquisition.

To achieve fast and accurate switch performance, each device comprises four n-channel JFET transistors and a TTL compatible bipolar driver. In the on state, each switch conducts current equally well in either direction. In the off condition, the switches will block up to 20 V peak-to-peak, with feedthrough of less than -60 dB at 10 MHz.

### Functional Block Diagram and Pin Configuration



Refer to JAN38510 Information, Military Section

\*Common to Substrate and Case

#### Ordering Information – DG183/184/185

Temp Range	Package	Part Number
-25 to 85°C	16-Pin Sidebraze	DG183BP
		DG184BP
		DG185BP
-55 to 125°C	16-Pin Sidebraze	DG183AP/883
		DG184AP
		DG184AP/883, JM38510/11103BEA
		DG185AP/883, JM38510/11104BEA
	14-Pin Flat Pack	JM38510/11103BXA
		JM38510/11104BXA

#### Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.0 V

Switches Shown for Logic "1" Input

## Absolute Maximum Ratings

V+ to V-	36 V
V+ to V <sub>D</sub>	33 V
V <sub>D</sub> to V-	33 V
V <sub>D</sub> to V <sub>D</sub>	±22 V
V <sub>L</sub> to V-	36 V
V <sub>L</sub> to V <sub>IN</sub>	8 V
V <sub>L</sub> to V <sub>R</sub>	8 V
V <sub>IN</sub> to V <sub>R</sub>	8 V
V <sub>R</sub> to V-	27 V
V <sub>R</sub> to V <sub>IN</sub>	2 V

Current (S or D) DG183	200 mA
Current (S or D) DG184, DG185	30 mA
Current (All Other Pins)	30 mA
Storage Temperature	-65 to 150°C
Power Dissipation <sup>a</sup>	
16-Pin Sidebrazeb	900 mW
14-Pin Flat Packc	900 mW

**Notes:**

- a. All leads welded or soldered to PC Board.
- b. Derate 12 mW/°C above 75°C
- c. Derate 10 mW/°C above 75°C

## Specifications<sup>a</sup> for DG183

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V, V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V, V <sub>IN</sub> = 0.8 V or 2 V <sup>1</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-7.5	15	-7.5	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = -7.5 V	Room Full	7.5		10 20		15 25	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		10 1000		15 300	nA
		V <sub>S</sub> = ±7.5 V, V <sub>D</sub> = ∓7.5 V	Room Hot	0.05		10 1000		15 300	
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		10 1000		15 300	
		V <sub>S</sub> = ±7.5 V, V <sub>D</sub> = ∓7.5 V	Room Hot	0.03		10 1000		15 300	
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = ±7.5 V	Room Hot	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I <sub>DSS</sub>	2 ms Pulse Duration	Room	300					mA
<b>Digital Input</b>									
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	Room Hot	<0.01		10 20		10 20	μA
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>on</sub>	See Switching Time Test Circuit	Room	240		400		600	ns
Turn-Off Time	t <sub>off</sub>		Room	140		200		220	
Source-Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz	Room	21					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		V <sub>S</sub> = -5 V, I <sub>D</sub> = 0	Room	17				
Channel-On Capacitance	C <sub>D(on)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	Room	17				
Off Isolation	OIRR	f = 1 MHz, R <sub>L</sub> = 75 Ω	Room	>55					dB
<b>Power Supplies</b>									
Positive Supply Current	I+	V <sub>IN</sub> = 0 V, or 5 V	Room	0.6		1.5		1.5	mA
Negative Supply Current	I-		Room	-2.7	-5		-5		
Logic Supply Current	I <sub>L</sub>		Room	3.1		4.5		4.5	
Reference Supply Current	I <sub>R</sub>		Room	-1	-2		-2		

**Specifications<sup>a</sup> for DG184**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, V_L = 5\text{ V}$ $V_R = 0\text{ V}, V_{IN} = 0.8\text{ V or }2\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-7.5	15	-7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = -7.5\text{ V}$	Room Full	22		30 60		50 75	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.06		1 100		5 100	nA
		$V_S = \pm 7.5\text{ V}, V_D = \mp 7.5\text{ V}$	Room Hot	0.05		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.4		1 100		5 100	
		$V_S = \pm 7.5\text{ V}, V_D = \mp 7.5\text{ V}$	Room Hot	0.3		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 7.5\text{ V}$	Room Hot	-0.02	-2 -200		-10 -200		
<b>Digital Input</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Hot	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{on}$	See Switching Time Test Circuit	Room	85		150		180	ns
Turn-Off Time	$t_{off}$		Room	95		130		150	
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		$V_S = -5\text{ V}, I_D = 0$	Room	6				
Channel-On Capacitance	$C_{D(on)}$		$V_D = -5\text{ V}, I_S = 0$	Room	14				
Off Isolation	OIRR	$f = 1\text{ MHz}, R_L = 75\ \Omega$	Room	>50					dB
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V, or }5\text{ V}$	Room	0.6		3		3	mA
Negative Supply Current	$I_-$		Room	-2.7	-5.5		-5.5		
Logic Supply Current	$I_L$		Room	3.1		4.5		4.5	
Reference Supply Current	$I_R$		Room	-1	-2		-2		

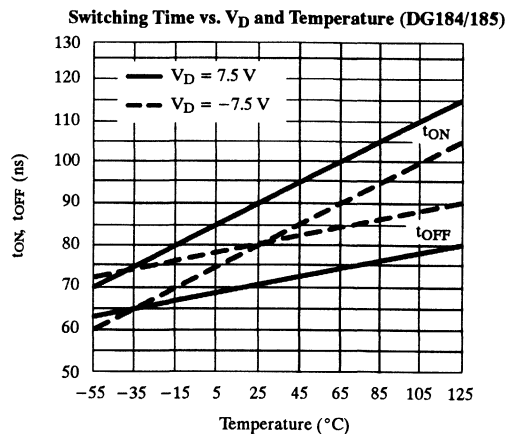
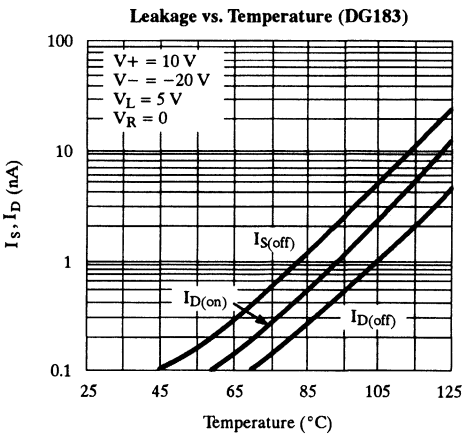
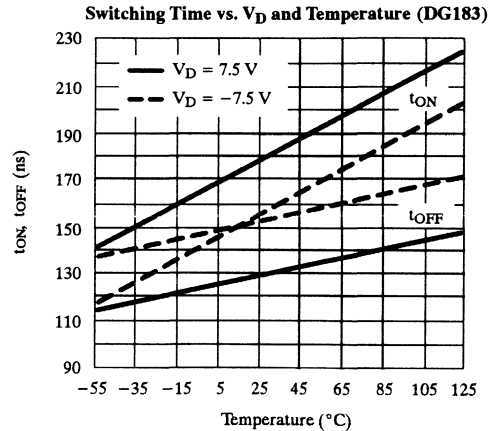
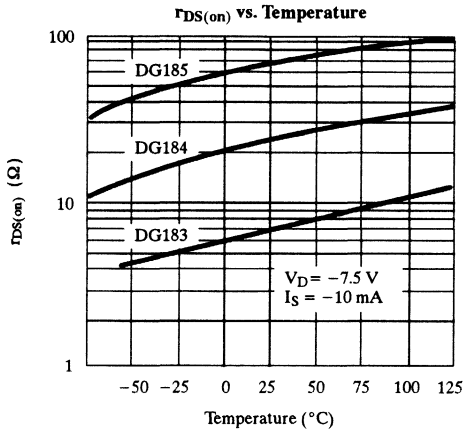
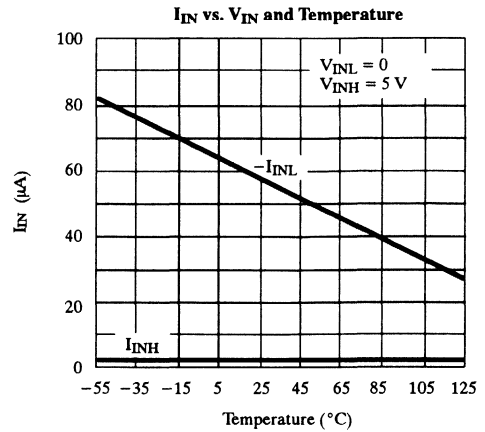
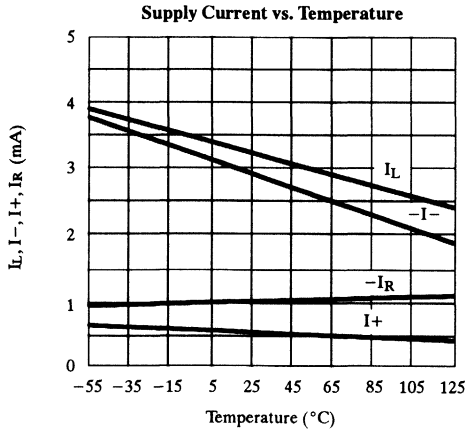
## Specifications<sup>a</sup> for DG185

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, V_L = 5\text{ V}$ $V_R = 0\text{ V}, V_{IN} = 0.8\text{ V or } 2\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-10	15	-10	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = -7.5\text{ V}$	Room Full	35		75 150		100 150	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.05		1 100		5 100	nA
		$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$	Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.4		1 100		5 100	
		$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$	Room Hot	0.3		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 10\text{ V}$	Room Hot	-0.03	-2 -200		-10 -200		
<b>Digital Input</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Hot	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{on}$	See Switching Time Test Circuit	Room	120		250		300	ns
Turn-Off Time	$t_{off}$		Room	100		130		150	
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		$V_S = -5\text{ V}, I_D = 0$	Room	6				
Channel-On Capacitance	$C_{D(on)}$		$V_D = -5\text{ V}, I_S = 0$	Room	14				
Off Isolation	OIRR	$f = 1\text{ MHz}, R_L = 75\text{ }\Omega$	Room	>50					dB
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V, or } 5\text{ V}$	Room	0.6		3		3	mA
Negative Supply Current	$I_-$		Room	-2.7	-5.5		-5.5		
Logic Supply Current	$I_L$		Room	3.1		4.5		4.5	
Reference Supply Current	$I_R$		Room	-1	-2		-2		

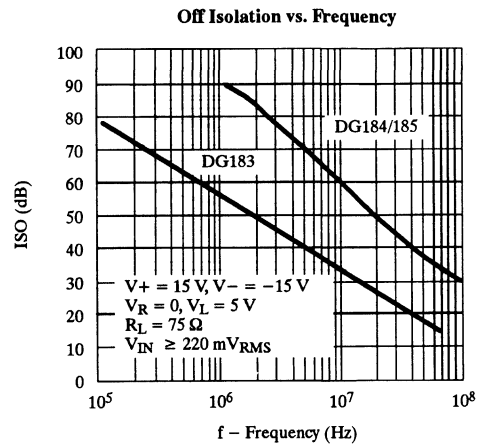
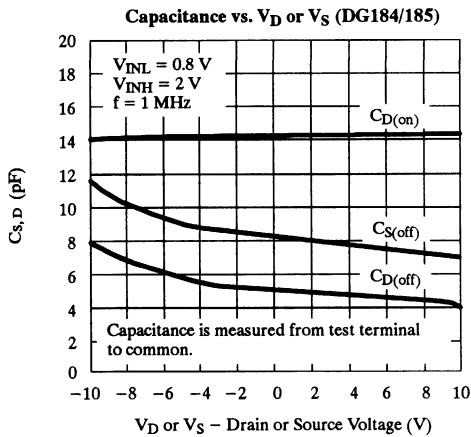
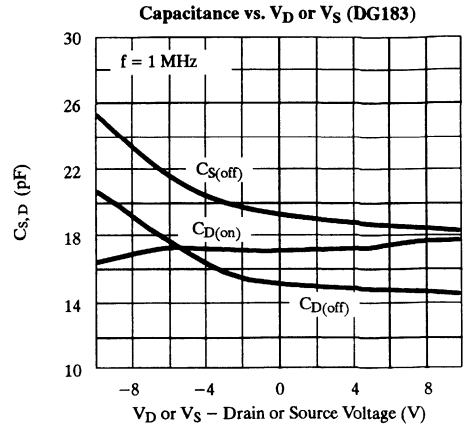
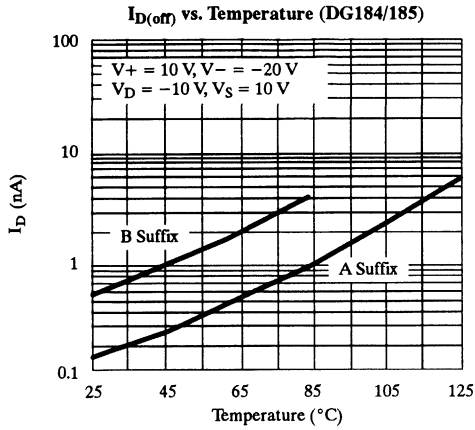
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

## Typical Characteristics



## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

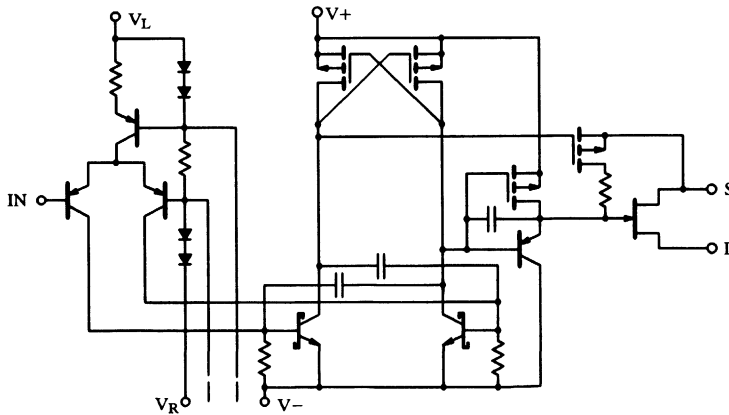
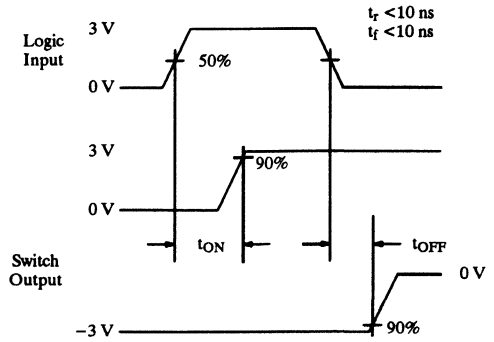
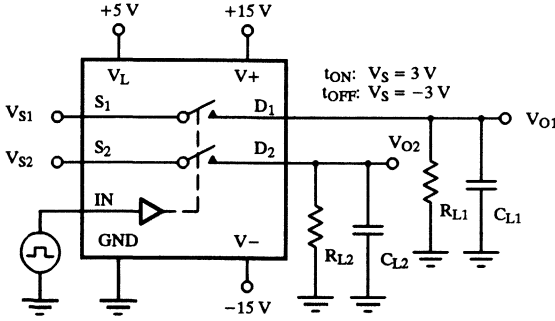


Figure 1.



**Test Circuits**

Feedthrough due to charge injection may result in spikes at the leading and trailing edge of the output waveform.



$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_s \times \frac{R_L}{R_L + r_{DS(on)}}$$

**Figure 2.** Switching Time

**Application Hints<sup>a</sup>**

Switch	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>L</sub> Logic Supply Voltage (V)	V <sub>R</sub> Reference Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> / V <sub>INL(max)</sub> (V)	V <sub>S</sub> Analog Voltage Range (V)
DG183 DG184	15 <sup>b</sup>	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
DG185	15 <sup>b</sup>	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

Notes:

- a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- b. Electrical Parameter Chart based on V+ = 15 V, V<sub>L</sub> = 5 V, V<sub>R</sub> = GND.

## High-Speed Drivers with SPDT JFET Switches

### Features

- Constant On-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Rad Hardness

### Benefits

- Low Distortion
- Eliminates Large Signal Errors
- High Precision
- High Bandwidth Capability
- Fault Protection

### Applications

- Audio Switching
- Video Switching
- Sample/Hold
- Guidance and Control Systems
- Telemetry

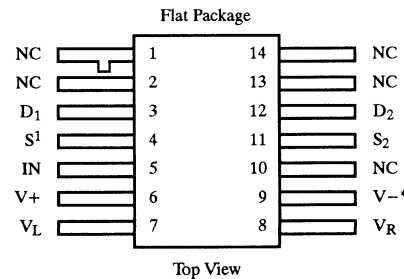
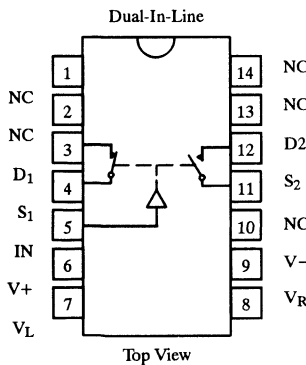
### Description

The DG186/187/188 are precision single-pole, double-throw (SPDT) analog switches designed to provide accurate switching of video and audio signals. This series is ideally suited for applications requiring a constant on-resistance over the entire analog range.

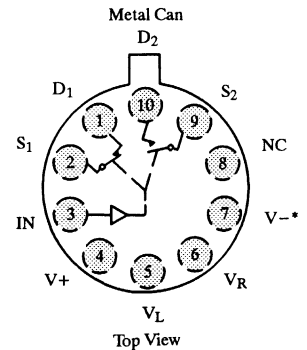
The major difference in the devices is the on-resistance (DG186—10  $\Omega$ , DG187—30  $\Omega$ , DG188—75  $\Omega$ ). Reduced errors are achieved through low leakage current ( $I_{D(on)} < 2$  nA). Applications which benefit from the flat JFET on-resistance include audio switching, video switching, and data acquisition.

To achieve fast and accurate switch performance, each device comprises two n-channel JFET transistors and a TTL compatible bipolar driver. The driver is designed to achieve break-before-make switching action, eliminating the inadvertent shorting between channels and the crosstalk which would result. In the on state, each switch conducts current equally well in either direction. In the off condition, the switches will block up to 20 V peak-to-peak, with feedthrough of less than -60 dB at 10 MHz.

### Functional Block Diagram and Pin Configuration



Refer to JAN38510 Information, Military Section



\*Common to Substrate and Case

#### Ordering Information – DG186/187/188

Temp Range	Package	Part Number
-25 to 85°C	10-Pin Metal Can	DG186BA
		DG187BA
		DG188BA
	14-Pin Sidebrazed	DG186BP
		DG187BP
		DG188BP
-55 to 125°C	10-Pin Metal Can	DG186AA/883
		DG187AA/883, JM38510/11105BIA
		DG188AA/883, JM38510/11106BIA
	14-Pin Sidebrazed	DG186AP/883
		DG187AP/883, JM38510/11105BCA
		DG188AP/883, JM38510/11106BCA
	14-Pin Flat Pack	JM38510/11105BXA
		JM38510/11106BXA

#### Truth Table

Logic	SW <sub>1</sub>	SW <sub>2</sub>
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8$  V

Logic "1"  $\geq 2.0$  V

Switches Shown for Logic "1" Input

**Absolute Maximum Ratings**

V+ to V~ .....	36 V	Current (S or D) DG187, DG188 .....	30 mA
V+ to V <sub>D</sub> .....	33 V	Current (All Other Pins) .....	30 mA
V <sub>D</sub> to V~ .....	33 V	Storage Temperature .....	-65 to 150°C
V <sub>D</sub> to V <sub>D</sub> .....	±22 V	Power Dissipation <sup>a</sup>	
V <sub>L</sub> to V~ .....	36 V	10-Pin Metal Can <sup>b</sup> .....	450 mW
V <sub>L</sub> to V <sub>IN</sub> .....	8 V	14-Pin Sidebraze <sup>c</sup> .....	825 mW
V <sub>L</sub> to V <sub>R</sub> .....	8 V	14-Pin Flat Pack <sup>d</sup> .....	900 mW
V <sub>IN</sub> to V <sub>R</sub> .....	8 V	Notes:	
V <sub>R</sub> to V~ .....	27 V	a. All leads welded or soldered to PC Board.	
V <sub>R</sub> to V <sub>IN</sub> .....	2 V	b. Derate 6 mW/°C above 75°C	
Current (S or D) DG186 .....	200 mA	c. Derate 11 mW/°C above 75°C	
		d. Derate 10 mW/°C above 75°C	

**Specifications<sup>a</sup> for DG186**

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V~ = -15 V, V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V, V <sub>IN</sub> = 0.8 or 2 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-7.5	15	-7.5	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = -7.5 V	Room Full	7.5		10 20		15 25	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V V+ = 10 V, V~ = -20 V	Room Hot	0.05		10 1000		15 300	nA
		V <sub>S</sub> = ±7.5 V, V <sub>D</sub> = ∓7.5 V	Room Hot	0.05		10 1000		15 300	
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V V+ = 10 V, V~ = -20 V	Room Hot	0.04		10 1000		15 300	nA
		V <sub>S</sub> = ±7.5 V, V <sub>D</sub> = ∓7.5 V	Room Hot	0.03		10 1000		15 300	
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = ±7.5 V	Room Hot	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I <sub>DSS</sub>	2 ms Pulse Duration	Room	300					mA
<b>Digital Input</b>									
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	Room Hot	<0.01		10 20		10 20	μA
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>on</sub>	See Switching Time Test Circuit	Room	240		400		425	ns
Turn-Off Time	t <sub>off</sub>		Room	140		200		225	
Source-Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz	Room	21					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		V <sub>S</sub> = -5 V, I <sub>D</sub> = 0	Room	17				
Channel-On Capacitance	C <sub>D(on)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	Room	17				
Off Isolation	OIRR	f = 1 MHz, R <sub>L</sub> = 75 Ω	Room	>55					dB
<b>Power Supplies</b>									
Positive Supply Current	I+	V <sub>IN</sub> = 0 V, or 5 V	Room			0.8		0.8	mA
Negative Supply Current	I-		Room		-3		-3		
Logic Supply Current	I <sub>L</sub>		Room			3.2		3.2	
Reference Supply Current	I <sub>R</sub>		Room		-2		-2		



## Specifications<sup>a</sup> for DG187

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, V_L = 5\text{ V}$ $V_R = 0\text{ V}, V_{IN} = 0.8\text{ or }2\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-7.5	15	-7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = -7.5\text{ V}$	Room Full	22		30 60		50 75	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.06		1 100		5 100	nA
		$V_S = \pm 7.5\text{ V}, V_D = \mp 7.5\text{ V}$	Room Hot	0.13		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.04		1 100		5 100	
		$V_S = \pm 7.5\text{ V}, V_D = \mp 7.5\text{ V}$	Room Hot	0.03		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 7.5\text{ V}$	Room Hot	-0.02	-2 -200		-10 -200		
<b>Digital Input</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Hot	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{on}$	See Switching Time Test Circuit	Room	85		150		180	ns
Turn-Off Time	$t_{off}$		Room	95		130		150	
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		$V_S = -5\text{ V}, I_D = 0$	Room	6				
Channel-On Capacitance	$C_{D(on)}$		$V_D = -5\text{ V}, I_S = 0$	Room	14				
Off Isolation	OIRR	$f = 1\text{ MHz}, R_L = 75\ \Omega$	Room	>50					dB
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V}, \text{ or }5\text{ V}$	Room			0.8		0.8	mA
Negative Supply Current	$I_-$		Room		-3		-3		
Logic Supply Current	$I_L$		Room			3.2		3.2	
Reference Supply Current	$I_R$		Room		-2		-2		

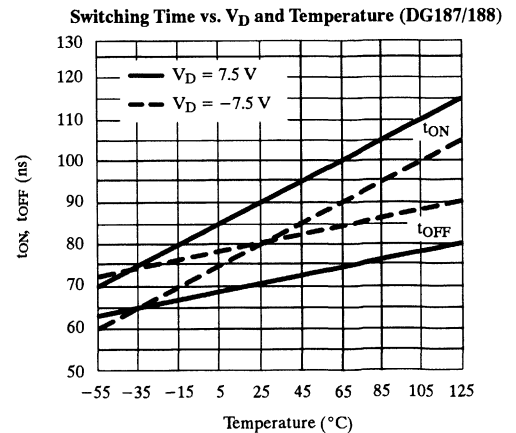
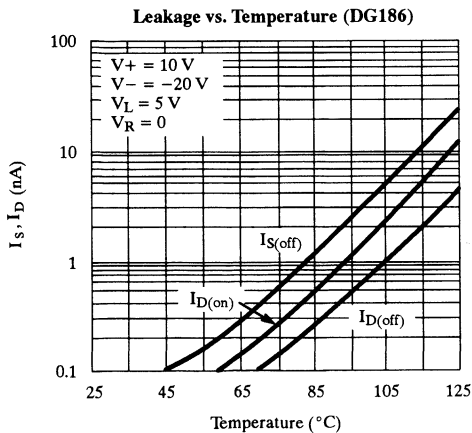
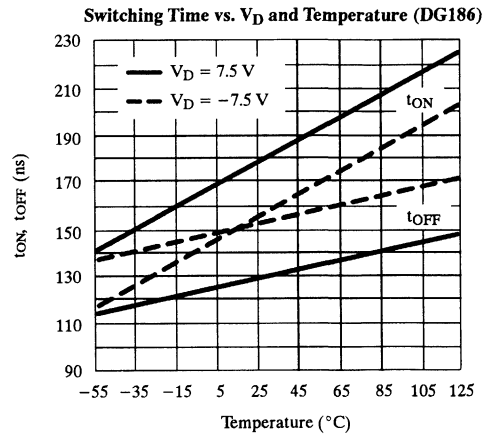
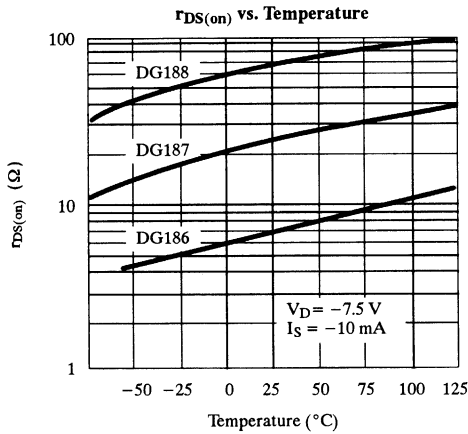
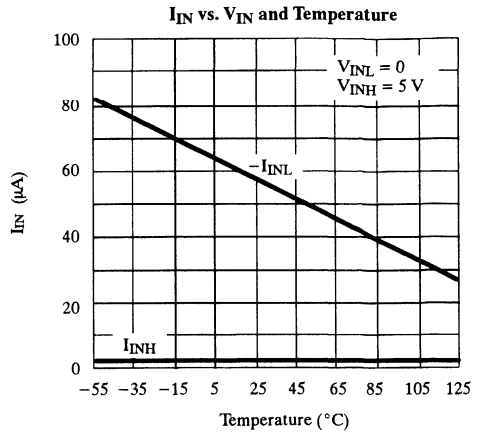
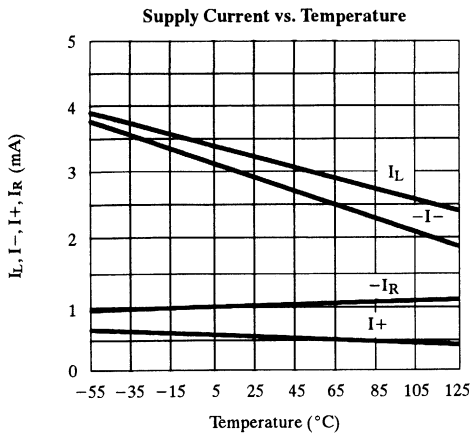
**Specifications<sup>a</sup> for DG188**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, V_I = 5\text{ V}$ $V_R = 0\text{ V}, V_{IN} = 0.8\text{ or }2\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-10	15	-10	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = -7.5\text{ V}$	Room Full	35		75 150		100 150	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.05		1 100		5 100	nA
		$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$	Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.04		1 100		5 100	
		$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$	Room Hot	0.50		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 10\text{ V}$	Room Hot	-0.03	-2 -200		-10 -200		
<b>Digital Input</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Hot	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{on}$	See Switching Time Test Circuit	Room	120		250		300	ns
Turn-Off Time	$t_{off}$		Room	100		130		150	
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		$V_D = -5\text{ V}, I_S = 0$	Room	6				
Channel-On Capacitance	$C_{D(on)}$		$V_D = V_S = 0\text{ V}$	Room	14				
Off Isolation	OIRR	$f = 1\text{ MHz}, R_L = 75\ \Omega$	Room	>50					dB
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V}, \text{ or }5\text{ V}$	Room			0.8		0.8	mA
Negative Supply Current	$I_-$		Room		-3		-3		
Logic Supply Current	$I_L$		Room			3.2		3.2	
Reference Supply Current	$I_R$		Room		-2		-2		

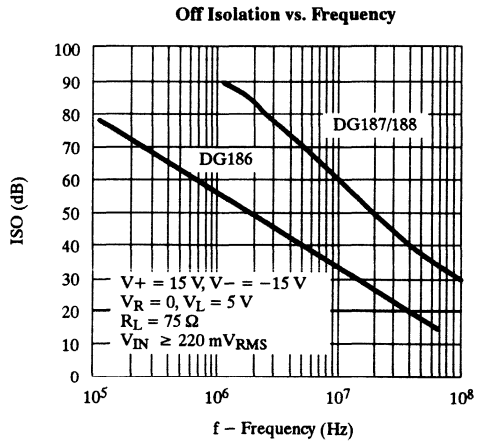
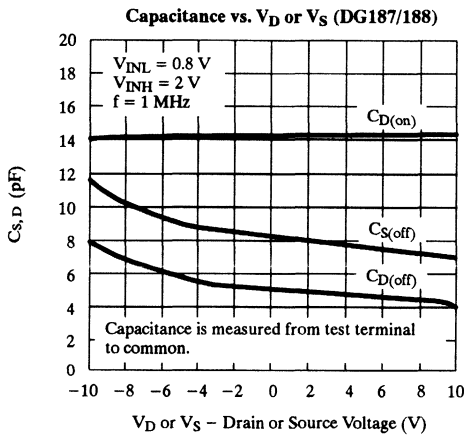
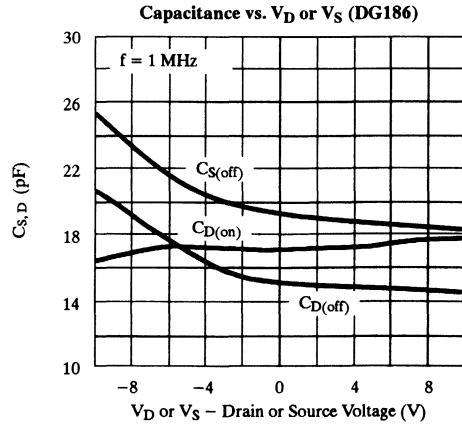
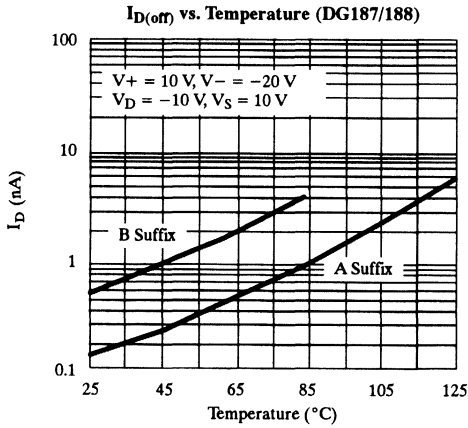
Notes:

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

## Typical Characteristics



## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

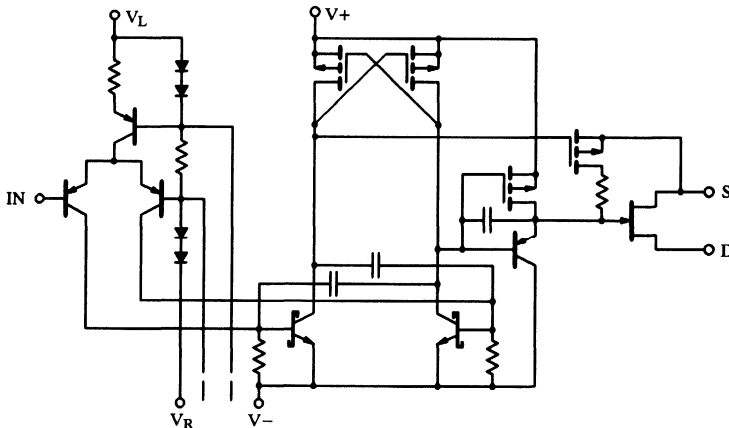


Figure 1.

## Test Circuits

Feedthrough due to charge injection may result in spikes at the leading and trailing edge of the output waveform.

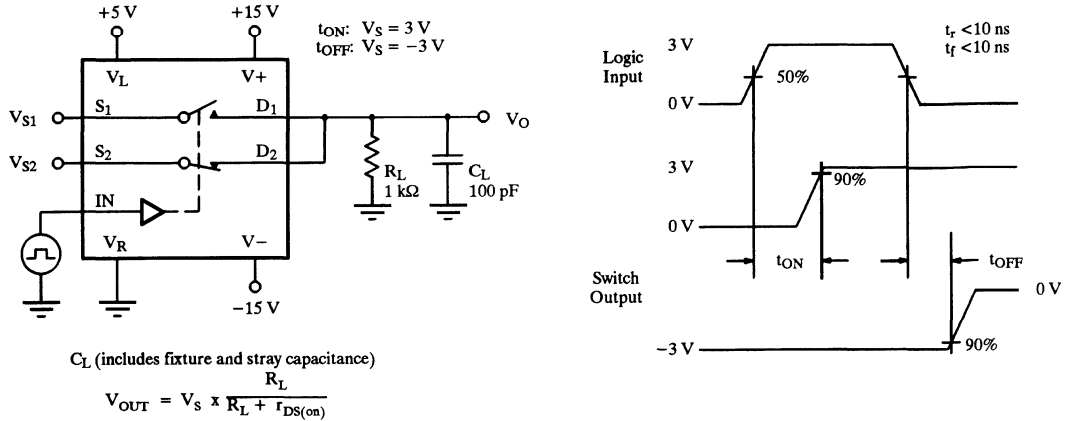


Figure 2. Switching Time

## Application Hints<sup>a</sup>

Switch	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>L</sub> Logic Supply Voltage (V)	V <sub>R</sub> Reference Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> / V <sub>INL(max)</sub> (V)	V <sub>S</sub> Analog Voltage Range (V)
DG186 DG187	15 <sup>b</sup>	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
DG188	15 <sup>b</sup>	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

Notes:

- Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- Electrical Parameter Chart based on V+ = 15 V, V<sub>L</sub> = 5 V, V<sub>R</sub> = GND



## High-Speed Drivers with Dual SPDT JFET Switches

### Features

- Constant On-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Rad Hardness

### Benefits

- Low Distortion
- Eliminates Large Signal Errors
- High Precision
- High Bandwidth Capability
- Fault Protection

### Applications

- Audio Switching
- Video Switching
- Sample/Hold
- Guidance and Control Systems
- Aerospace

### Description

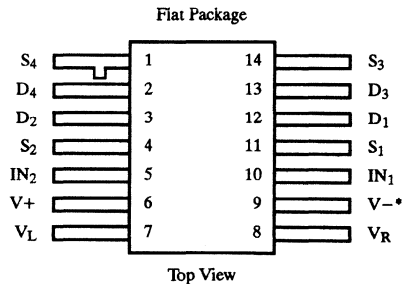
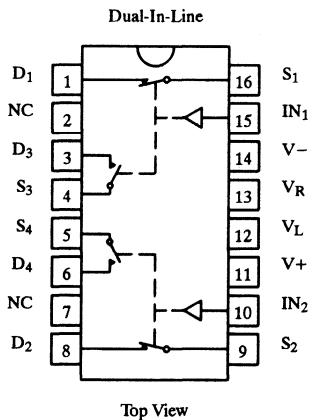
The DG189/190/191 are precision dual single-pole, double-throw (SPDT) analog switches designed to provide accurate switching of video and audio signals. This series is ideally suited for applications requiring a constant on-resistance over the entire analog range.

The major difference in the devices is the on-resistance (DG189—10  $\Omega$ , DG190—30  $\Omega$ , DG191—75  $\Omega$ ). Reduced errors are achieved through low leakage current ( $I_{D(on)} < 2$  nA). Applications which benefit from the flat JFET

on-resistance include audio switching, video switching, and data acquisition.

To achieve fast and accurate switch performance, each device comprises four n-channel JFET transistors and a TTL compatible bipolar driver. The driver is designed to achieve break-before-make switching action, eliminating the inadvertent shorting between channels and the crosstalk which would result. In the on state, each switch conducts current equally well in either direction. In the off condition, the switches will block up to 20 V peak-to-peak, with feedthrough of less than -60 dB at 10 MHz.

### Functional Block Diagram and Pin Configuration



Refer to JAN38510 Information, Military Section

\*Common to Substrate and Case

#### Ordering Information – DG189/190/191

Temp Range	Package	Part Number
-25 to 85°C	16-Pin Sidebraze	DG189BP
		DG190BP
		DG191BP
-55 to 125°C	16-Pin Sidebraze	DG189AP/883, 5962-9068901MEA
		DG190AP/883, JM38510/11107BEA
		DG191AP/883, JM38510/11108BEA
	14-Pin Flat Pack	JM38510/11107BXA
		JM38510/11108BXA

Truth Table		
Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V  
Switches Shown for Logic "1" Input

## Absolute Maximum Ratings

V+ to V-	36 V	Current (S or D) DG189	200 mA
V+ to V <sub>D</sub>	33 V	Current (S or D) DG190, DG191	30 mA
V <sub>D</sub> to V-	33 V	Current (All Other Pins)	30 mA
V <sub>D</sub> to V <sub>D</sub>	±22 V	Storage Temperature	-65 to 150°C
V <sub>L</sub> to V-	36 V	Power Dissipation <sup>a</sup>	
V <sub>L</sub> to V <sub>IN</sub>	8 V	16-Pin Sidebrazed <sup>b</sup>	900 mW
V <sub>L</sub> to V <sub>R</sub>	8 V	14-Pin Flat Pack <sup>c</sup>	900 mW
V <sub>IN</sub> to V <sub>R</sub>	8 V	Notes:	
V <sub>R</sub> to V-	27 V	a. All leads welded or soldered to PC Board.	
V <sub>R</sub> to V <sub>IN</sub>	2 V	b. Derate 12 mW/°C above 75°C.	
		c. Derate 10 mW/°C above 75°C.	

## Specifications<sup>a</sup> for DG189

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V, V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V, V <sub>IN</sub> = 0.8 V or 2 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-7.5	15	-7.5	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = -7.5 V	Room Full	7.5		10 20		15 25	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		10 1000		15 300	nA
		V <sub>S</sub> = ±7.5 V, V <sub>D</sub> = ∓7.5 V	Room Hot	0.05		10 1000		15 300	
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		10 1000		15 300	nA
		V <sub>S</sub> = ±7.5 V, V <sub>D</sub> = ∓7.5 V	Room Hot	0.03		10 1000		15 300	
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = ±7.5 V	Room Hot	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I <sub>DSS</sub>	2 ms Pulse Duration	Room	300					mA
<b>Digital Input</b>									
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	Room Hot	<0.01		10 20		10 20	μA
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>on</sub>	See Switching Time Test Circuit	Room	240		400		425	ns
Turn-Off Time	t <sub>off</sub>		Room	140		200		225	
Source-Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz	Room	21					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		V <sub>S</sub> = -5 V, I <sub>D</sub> = 0	Room	17				
Channel-On Capacitance	C <sub>D(on)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	Room	17				
Off Isolation	OIRR	f = 1 MHz, R <sub>L</sub> = 75 Ω	Room	>55					dB
<b>Power Supplies</b>									
Positive Supply Current	I+	V <sub>IN</sub> = 0 V, or 5 V	Room	0.6		1.5		1.5	mA
Negative Supply Current	I-		Room	-2.7	-5		-5		
Logic Supply Current	I <sub>L</sub>		Room	3.1		4.5		4.5	
Reference Supply Current	I <sub>R</sub>		Room	-1	-2		-2		

**Specifications<sup>a</sup> for DG190**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, V_L = 5\text{ V}$ $V_R = 0\text{ V}, V_{IN} = 0.8\text{ V or } 2\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-7.5	15	-7.5	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = -7.5\text{ V}$	Room Full	18		30 60		50 75	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.06		1 100		5 100	nA
		$V_S = \pm 7.5\text{ V}, V_D = \mp 7.5\text{ V}$	Room Hot	0.1		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.05		1 100		5 100	
		$V_S = \pm 7.5\text{ V}, V_D = \mp 7.5\text{ V}$	Room Hot	0.06		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 7.5\text{ V}$	Room Hot	-0.02	-2 -200		-10 -200		
<b>Digital Input</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Hot	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{on}$	See Switching Time Test Circuit	Room	85		150		180	ns
Turn-Off Time	$t_{off}$		Room	95		130		150	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		$V_S = -5\text{ V}, I_D = 0$	Room	6				
Channel-On Capacitance	$C_{D(on)}$		$V_D = -5\text{ V}, I_S = 0$	Room	14				
		$V_D = V_S = 0\text{ V}$	Room	>50					
Off Isolation	OIRR	f = 1 MHz, $R_L = 75\ \Omega$	Room	>50					dB
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V}, \text{ or } 5\text{ V}$	Room	0.6		1.5		1.5	mA
Negative Supply Current	$I_-$		Room	-2.7	-5		-5		
Logic Supply Current	$I_L$		Room	3.1		4.5		4.5	
Reference Supply Current	$I_R$		Room	-1	-2		-2		

## Specifications<sup>a</sup> for DG191

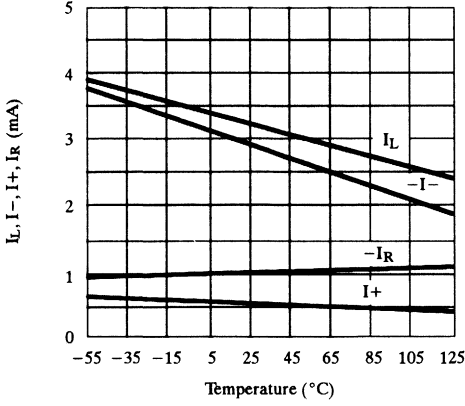
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, V_L = 5\text{ V}$ $V_R = 0\text{ V}, V_{IN} = 0.8\text{ V or } 2\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B Suffix -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-10	15	-10	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = -7.5\text{ V}$	Room Full	35		75 150		100 150	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.05		1 100		5 100	nA
		$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$	Room Hot	0.07		1 100		5 100	
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	Room Hot	0.04		1 100		5 100	
		$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$	Room Hot	0.05		1 100		5 100	
Channel On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 10\text{ V}$	Room Hot	-0.03	-2 -200		-10 -200		
<b>Digital Input</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Hot	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Full	-30	-250		-250		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{on}$	See Switching Time Test Circuit	Room	120		250		300	ns
Turn-Off Time	$t_{off}$		Room	100		130		150	
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	9					pF
Drain-Off Capacitance	$C_{D(off)}$		$V_S = -5\text{ V}, I_D = 0$	Room	6				
Channel-On Capacitance	$C_{D(on)}$		$V_D = -5\text{ V}, I_S = 0$	Room	14				
Off Isolation	OIRR	$f = 1\text{ MHz}, R_L = 75\ \Omega$	Room	>50					dB
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V, or } 5\text{ V}$	Room	0.6		1.5		1.5	mA
Negative Supply Current	$I_-$		Room	-2.7	-5		-5		
Logic Supply Current	$I_L$		Room	3.1		4.5		4.5	
Reference Supply Current	$I_R$		Room	-1	-2		-2		

**Notes:**

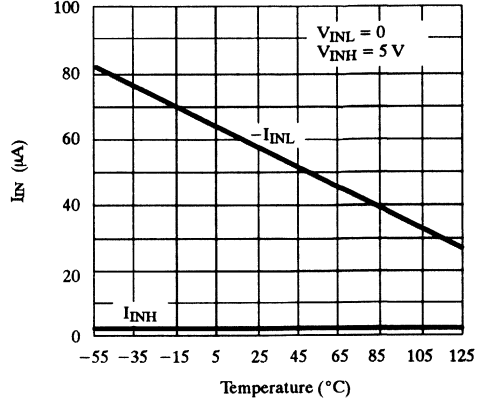
- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**

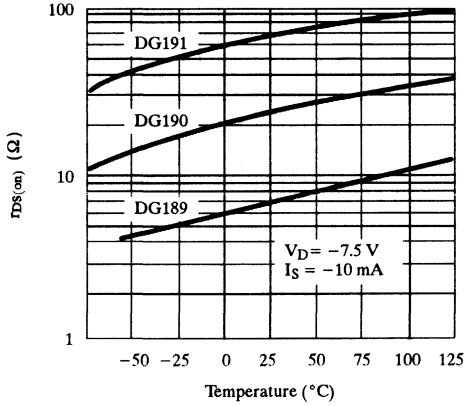
**Supply Current vs. Temperature**



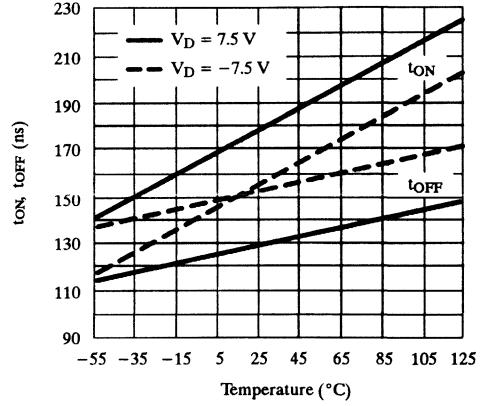
**$I_{IN}$  vs.  $V_{IN}$  and Temperature**



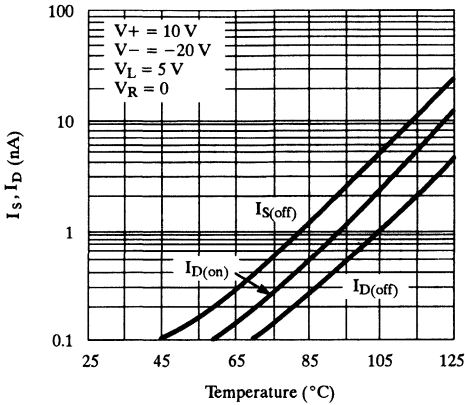
**$r_{DS(on)}$  vs. Temperature**



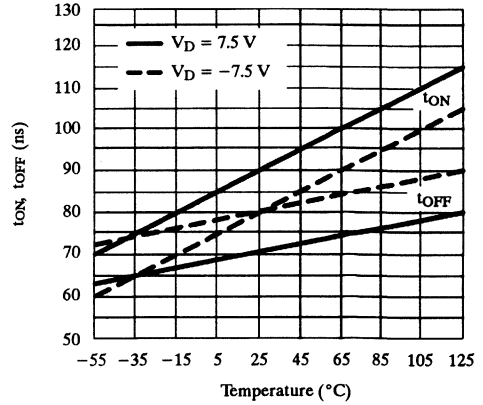
**Switching Time vs.  $V_D$  and Temperature (DG189)**



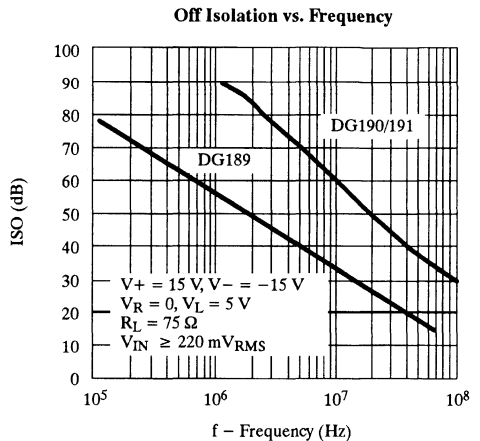
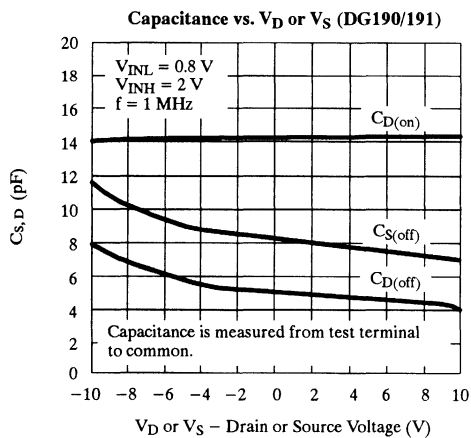
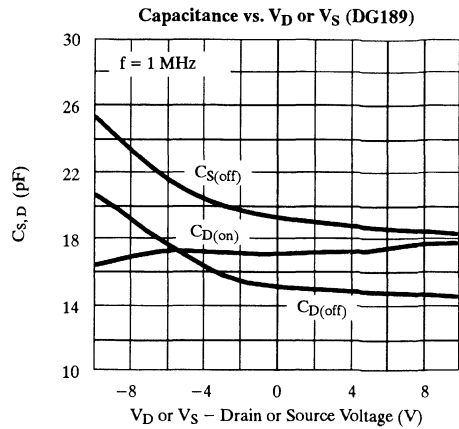
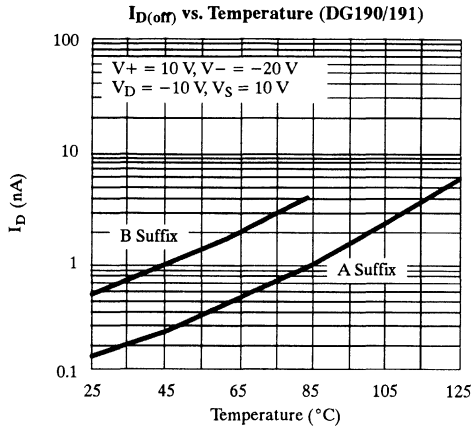
**Leakage vs. Temperature (DG189)**



**Switching Time vs.  $V_D$  and Temperature (DG190/191)**



## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

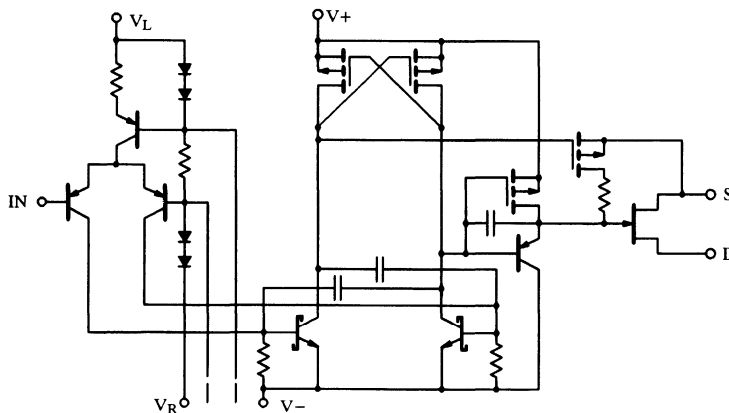
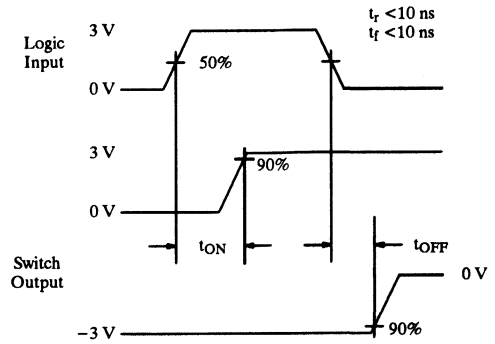
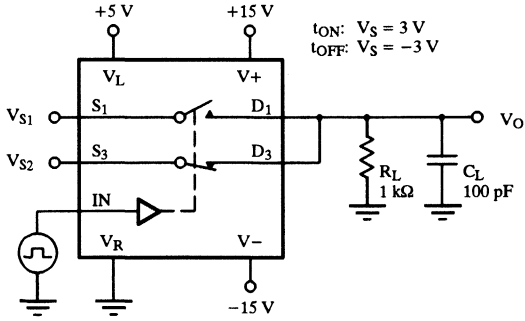


Figure 1.

**Test Circuits**

Feedthrough due to charge injection may result in spikes at the leading and trailing edge of the output waveform.



$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_S \times \frac{R_L}{R_L + \tau_{DS(on)}}$$

**Figure 2. Switching Time**

**Application Hints<sup>a</sup>**

Switch	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>L</sub> Logic Supply Voltage (V)	V <sub>R</sub> Reference Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage VINL(min)/ VINL(max) (V)	V <sub>S</sub> Analog Voltage Range (V)
DG189 DG190	15 <sup>b</sup>	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
DG191	15 <sup>b</sup>	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

Notes:

- a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- b. Electrical Parameter Chart based on V+ = 15 V, V<sub>L</sub> = 5 V, V<sub>R</sub> = GND

## Monolithic Dual SPST CMOS Analog Switch

### Features

- $\pm 15$  V Input Signal Range
- 44-V Maximum Supply Ranges
- On-Resistance: 45  $\Omega$
- TTL and CMOS Compatibility

### Benefits

- Wide Dynamic Range
- Simple Interfacing
- Reduced External Component Count

### Applications

- Servo Control Switching
- Programmable Gain Amplifiers
- Audio Switching
- Programmable Filters

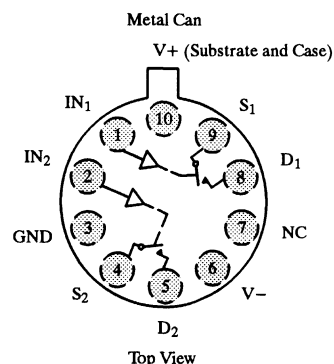
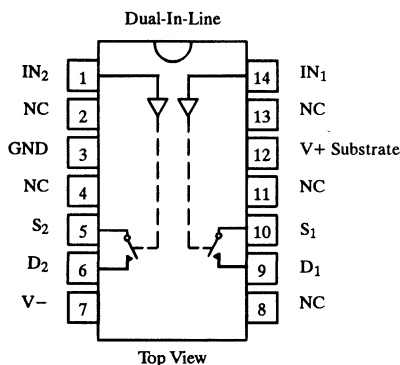
### Description

The DG200A is a dual, single-pole, single-throw analog switch designed to provide general purpose switching of analog signals. This device is ideally suited for designs requiring a wide analog voltage range coupled with low on-resistance.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. In the on condition, this bi-directional switch introduces no offset voltage of its own.

The DG200A is designed on Siliconix' improved PLUS-40 CMOS process. An epitaxial layer prevents latchup.

### Functional Block Diagram and Pin Configuration



#### Ordering Information

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG200ACJ
-25 to 85°C	14-Pin CerDIP	DG200ABK
	10-Pin Metal Can	DG200ABA
-55 to 125°C	14-Pin CerDIP	DG200AAK
		DG200AAK/883, JM38510/12301BCA
	10-Pin Metal Can	DG200AAA
		DG200AAA/883, JM38510/12301BIC
14-Pin Sidebrazed	JM38510/12301BCC	

#### Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

Switches Shown for Logic "1" Input



**Absolute Maximum Ratings**

V+ to V- .....	44 V
GND to V- .....	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub> .....	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Current (Any Terminal) Continuous .....	30 mA
Current S or D (Pulsed at 1 ms, 10% Duty Cycle Max) .....	100 mA
Storage Temperature (AX, BX Suffix) .....	-65 to 150°C
(CJ Suffix) .....	-65 to 125°C

Power Dissipation (Package) <sup>b</sup>	
10-Pin Metal Can <sup>c</sup> .....	450 mW
14-Pin CerDIP <sup>d</sup> .....	825 mW
14-Pin Plastic DIP <sup>e</sup> .....	470 mW

- Notes:
- Signals on S<sub>X</sub>, D<sub>X</sub>, or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads welded or soldered to PC Board.
  - Derate 6 mW/°C above 75°C
  - Derate 11 mW/°C above 75°C
  - Derate 6.5 mW/°C above 25°C

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C Suffix		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = -1 mA	Room Full	45		70 100		80 100	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room Full	±0.01	-2 -100	2 100	-5 -100	5 100	nA
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = ±14 V, V <sub>S</sub> = ∓14 V	Room Full	±0.01	-2 -100	2 100	-5 -100	5 100	
Channel On Leakage Current <sup>f</sup>	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = ±14 V	Room Full	±0.1	-2 -200	2 200	-5 -200	5 200	
<b>Digital Control</b>									
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2.4 V	Room Full	0.0009	-0.5 -1		-1 -10		μA
		V <sub>IN</sub> = 15 V	Room Full	0.005		0.5 1		1 10	
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Room Full	-0.0015	-0.5 -1		-1 -10		
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	See Switching Time Test Circuit	Room	440		1000		1000	ns
Turn-Off Time	t <sub>OFF</sub>		Room	340		425		425	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>g</sub> = 0 V, R <sub>g</sub> = 0 Ω	Room	-10					pC
Source-Off Capacitance	C <sub>S(off)</sub>	f = 140 kHz V <sub>IN</sub> = 5 V	Room	9					pF
Drain-Off Capacitance	C <sub>D(off)</sub>								
Channel-On Capacitance	C <sub>D(on)</sub> + C <sub>S(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V, V <sub>IN</sub> = 0 V	Room	25					
Off Isolation	OIRR	V <sub>IN</sub> = 5 V, R <sub>L</sub> = 75 Ω V <sub>S</sub> = 2 V, f = 1 MHz	Room	75					dB
Crosstalk (Channel-to-Channel)	X <sub>TALK</sub>		Room	90					



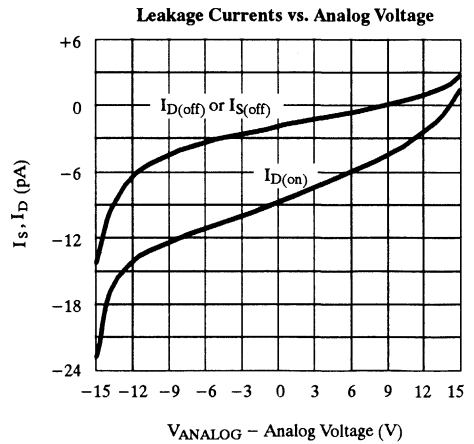
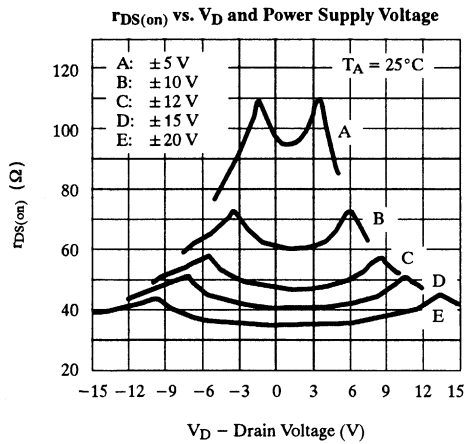
## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V+ = 15\text{ V}, V- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C Suffix		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	Both Channels On or Off $V_{IN} = 0\text{ V}$ and $2.4\text{ V}$	Room	0.8		2		2	mA
Negative Supply Current	I-		Room	-0.23	-1		-1		

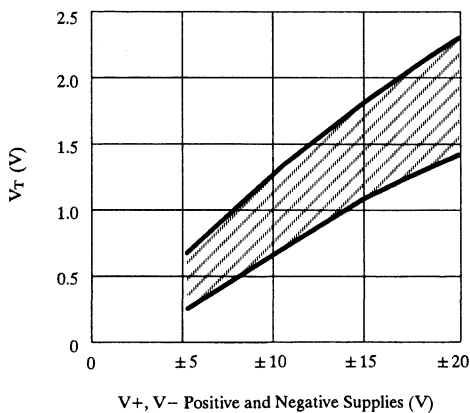
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
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- The algebraic convention whereby the most negative value is minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

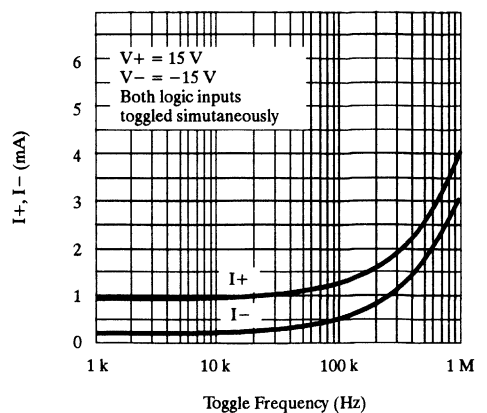
## Typical Characteristics



**Input Switching Threshold vs.  $V+$  and  $V-$  Supply Voltages**



**Supply Currents vs. Toggle Frequency**



**Schematic Diagram (Typical Channel)**

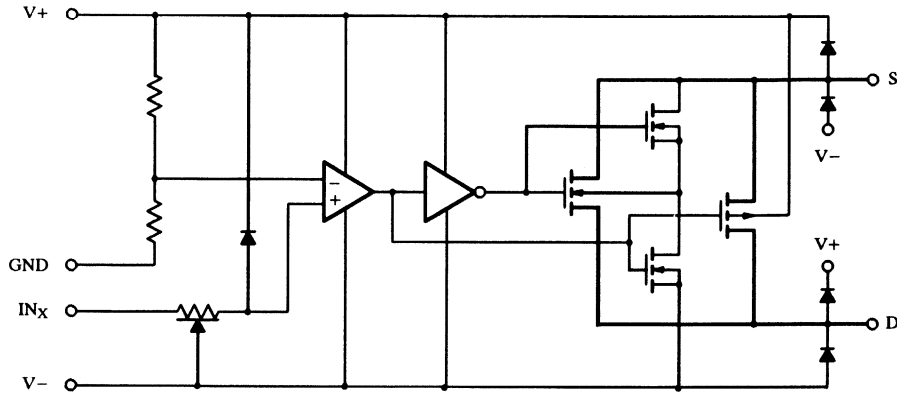


Figure 1.

**Test Circuits**

$V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

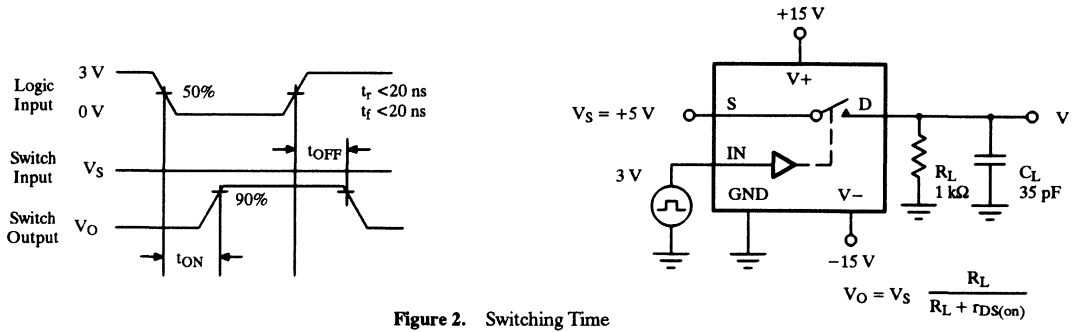
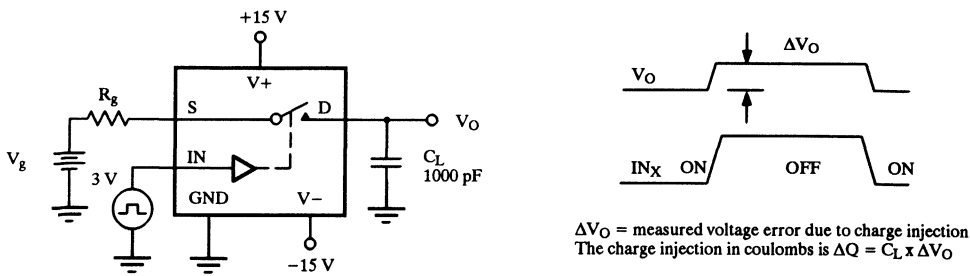


Figure 2. Switching Time

1

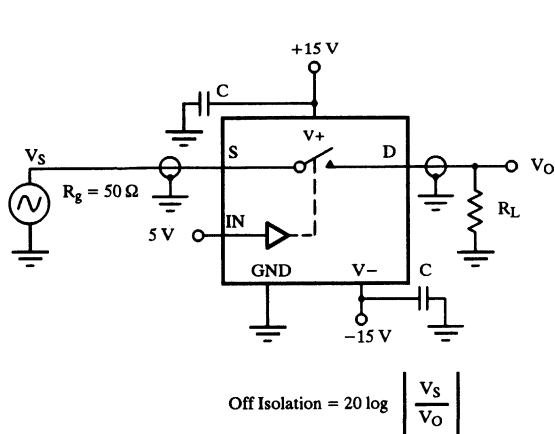


$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $\Delta Q = C_L \times \Delta V_O$

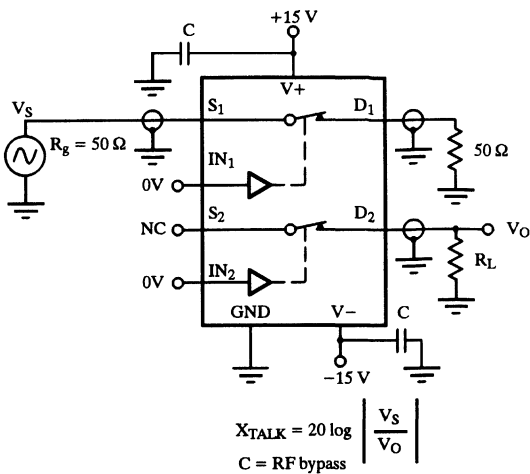
Figure 3. Charge Injection

## Test Circuits (Cont'd)

$V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



**Figure 4.** Off Isolation



**Figure 5.** Channel-to-Channel Crosstalk

## Monolithic Quad SPST CMOS Analog Switches

### Features

- $\pm 15\text{-V}$  Input Range
- Low Off Leakage— $I_{D(on)}$ : 0.1 nA
- Low On-Resistance— $r_{DS(on)}$ : 115  $\Omega$
- 44-V Maximum Supply Ratings
- TTL and CMOS Compatible

### Benefits

- Wide Input Range
- Low Distortion Switching
- Can Be Driven from Comparators or Op Amps Without Limiting Resistors

### Applications

- Disk Drives
- Radar Systems
- Communications Systems
- Sample-and-Hold

### Description

The DG201A and DG202 are quad SPST analog switches designed to provide accurate switching over a wide range of input signals. When combining a low on-resistance and a wide signal range ( $\pm 15\text{ V}$ ) with low charge-transfer these devices are well suited for industrial and military applications.

conducts equally well in both directions when on. When off these switches will block up to 30 V peak-to-peak and have a 44-V absolute maximum power supply rating.

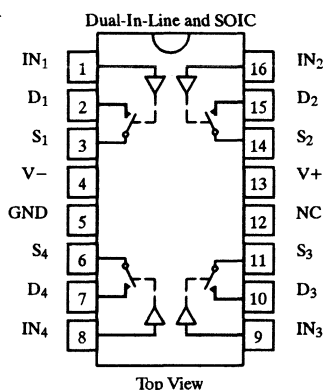
These two devices are differentiated by the type of switch actions. (See Truth Table).

Built on Siliconix' high voltage metal gate process to achieve optimum switch performance, each switch

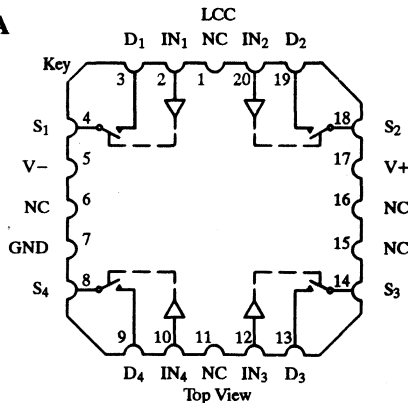
The DG201B/DG202B upgrades are recommended for new designs.

### Functional Block Diagram and Pin Configuration

DG201A



DG201A



#### Ordering Information – DG201A/202

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG201ACJ
		DG202CJ
-25 to 85°C	16-Pin CerDIP	DG201ABK
-40 to 85°C	16-Pin Narrow SOIC	DG201ADY
		DG201AAK
	16-Pin CerDIP	DG201AAK/883, JM38510/12302BEA
		7705301EA
		DG202AK
		DG202AK/883
	16-Pin Sidebrazed	JM38510/12302BEC
		7705301EC
	LCC-20	DG201AAZ/883, 77053012A

#### Truth Table

Logic	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8\text{ V}$   
Logic "1"  $\geq 2.4\text{ V}$

Switches Shown for DG201A Logic "1" Input



## Absolute Maximum Ratings

Voltages Referenced to V-

V+ .....	44 V
GND .....	25 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub> .....	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Current, Any Terminal Except S or D .....	30 mA
Continuous Current, S or D .....	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max) .....	70 mA
Storage Temperature (K, Z Suffix) .....	-65 to 150°C
(J, Y Suffix) .....	-65 to 125°C

Power Dissipation (Package)<sup>b</sup>

16-Pin Plastic DIP <sup>c</sup> .....	470 mW
16-Pin SOIC <sup>d</sup> .....	640 mW
16-Pin CerDIP and Sidebrazed <sup>e</sup> .....	900 mW
LCC-20 <sup>f</sup> .....	750 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C
- Derate 7.6 mW/°C above 75°C
- Derate 12 mW/°C above 75°C
- Derate 10 mW/°C above 75°C

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C, D Suffix		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = 1 mA	Room	115				175	Ω
			Full					250	
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room Full	±0.02	-1 -100	1 100	-5 -100	5 100	nA
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = ±14 V, V <sub>S</sub> = ∓14 V	Room Full	±0.02	-1 -100	1 100	-5 -100	5 100	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V	Room Full	±0.15	-1 -200	1 200	-5 -200	5 200	
<b>Digital Control</b>									
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2.4 V	Room Full	-0.0004	-1 -1		-1 -10		μA
		V <sub>IN</sub> = 15 V	Room Full	0.003		1 10		1 10	
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Room Full	-0.0004	-1 -10		-1 -10		
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	See Switching Time Test Circuit	Room	480		600		600	ns
Turn-Off Time	t <sub>OFF</sub>		Room	370		450		450	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>g</sub> = 0 V, R <sub>g</sub> = 0 Ω	Room	20					pC
Source-Off Capacitance	C <sub>S(off)</sub>	V <sub>S</sub> = 0 V, V <sub>IN</sub> = 5 V, f = 1 MHz	Room	5					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room	5					
Channel On Capacitance	C <sub>D(on)</sub> + C <sub>S(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V, V <sub>IN</sub> = 0 V f = 1 MHz	Room	16					
Off Isolation	OIRR	V <sub>IN</sub> = 5 V, R <sub>L</sub> = 75 Ω V <sub>S</sub> = 2 V, f = 100 kHz	Room	70					dB
Channel-to-Channel Crosstalk	X <sub>TALK</sub>		Room	90					

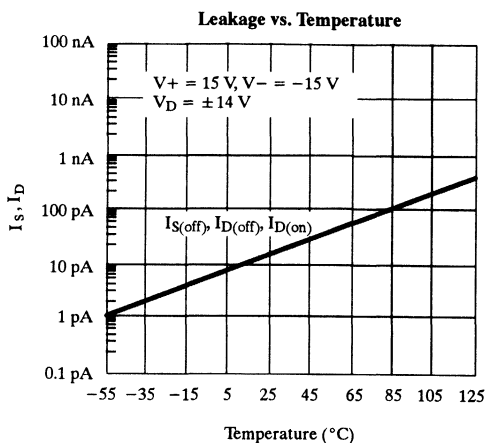
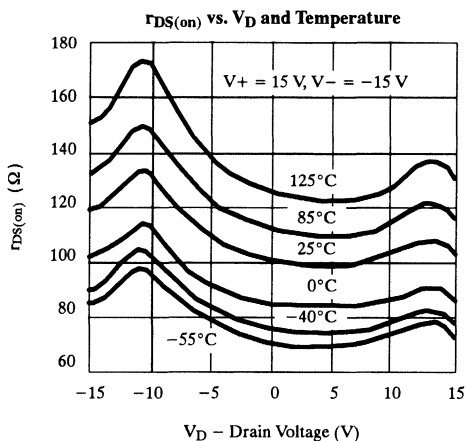
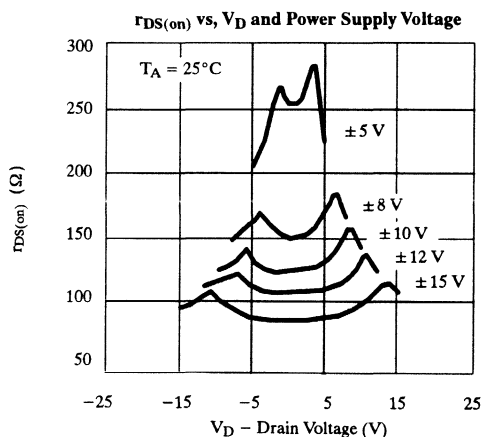
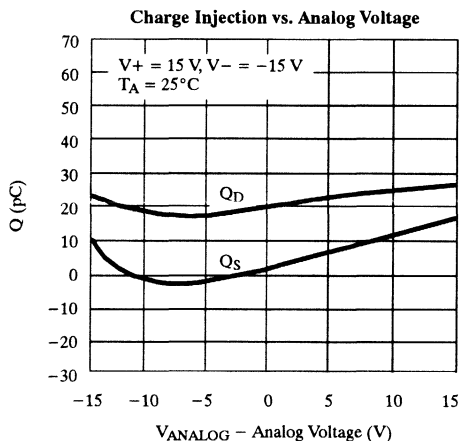
**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C, D Suffix		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supply</b>									
Positive Supply Current	I+	All Channels On or Off	Room	0.9		2		2	mA
Negative Supply Current	I-		Room	-0.3	-1		-1		

**Notes:**

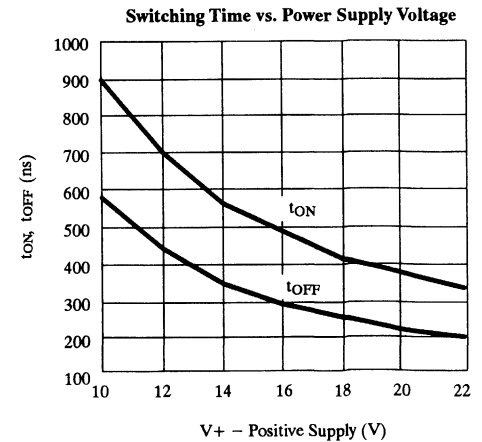
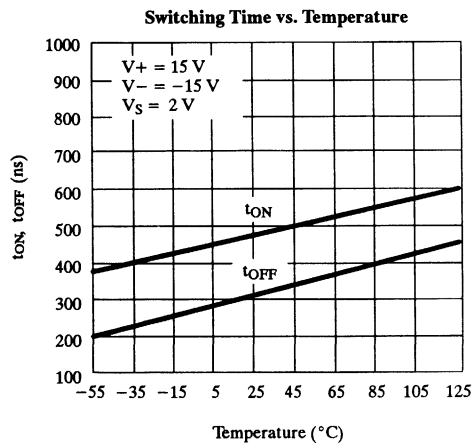
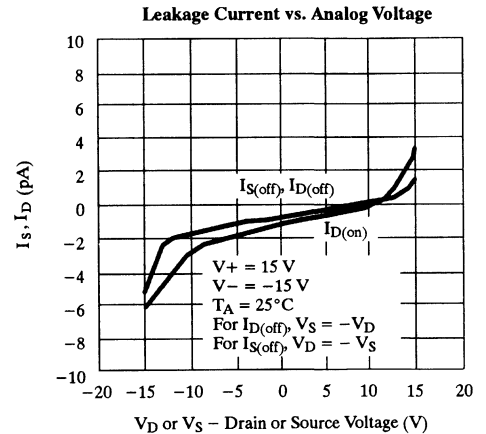
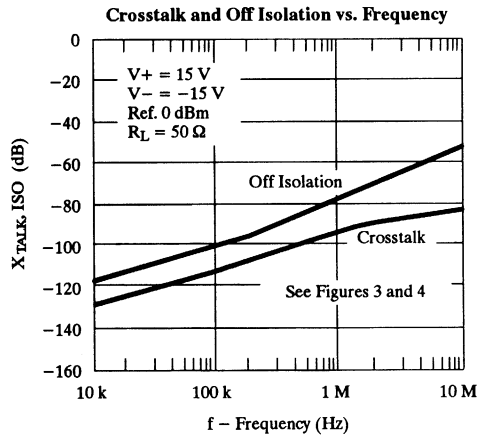
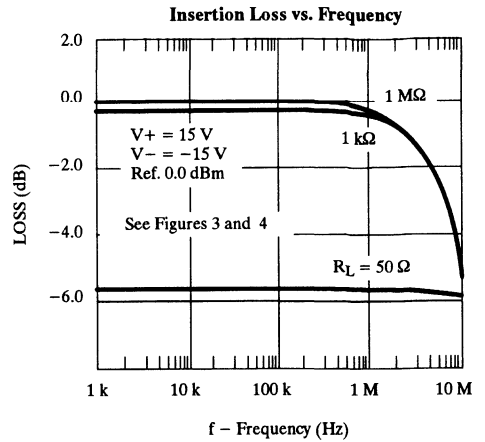
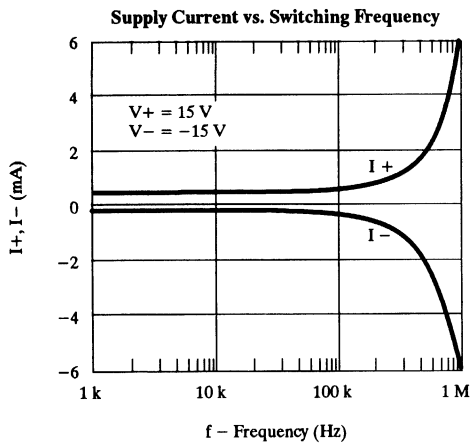
- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**



**1**

## Typical Characteristics (Cont'd)





**Schematic Diagram (Typical Channel)**

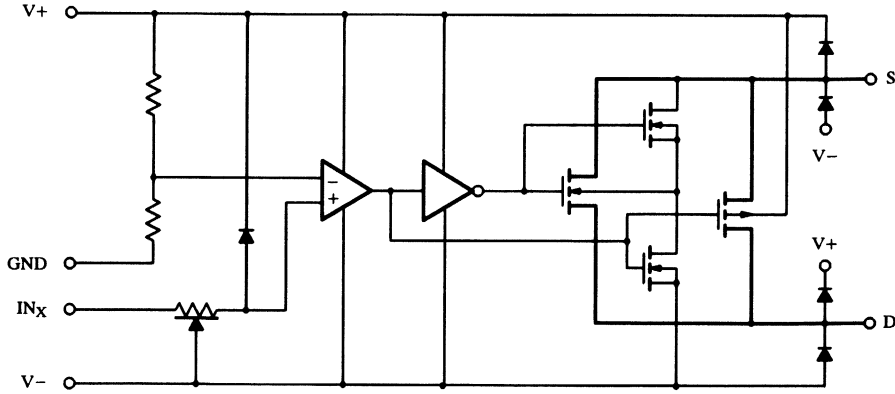


Figure 1.

**Test Circuits**

V<sub>O</sub> is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

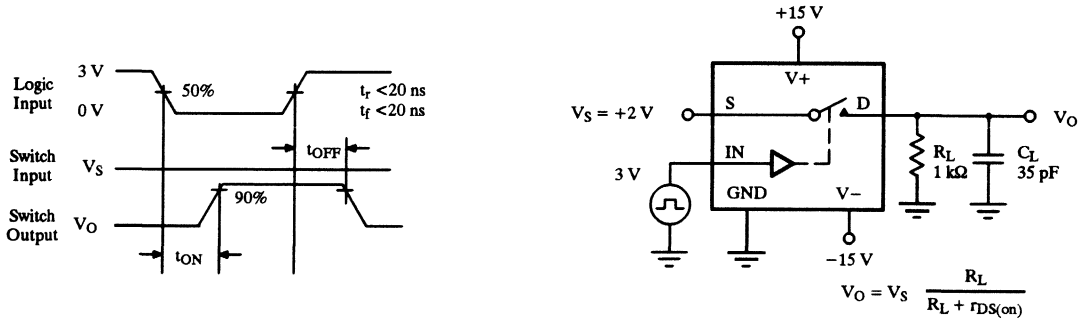


Figure 2. Switching Time

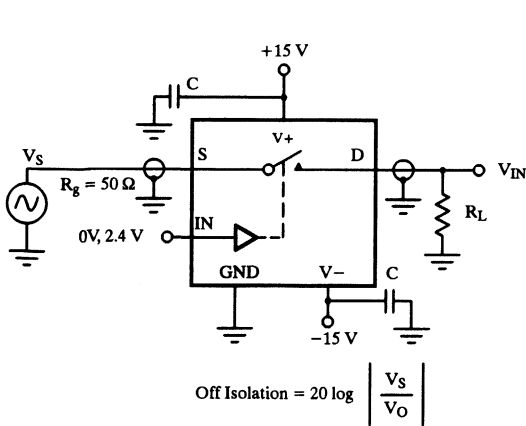


Figure 3. Off Isolation

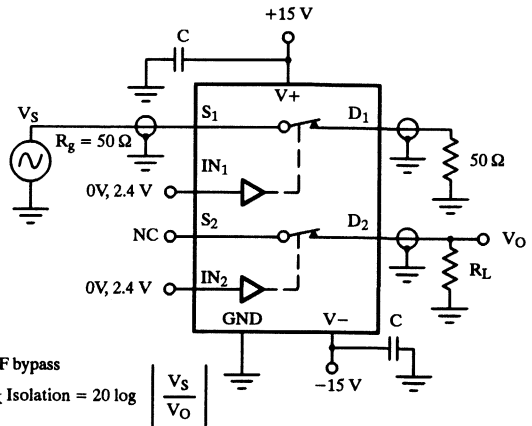
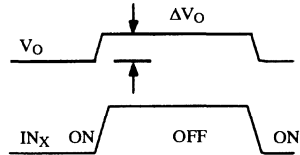
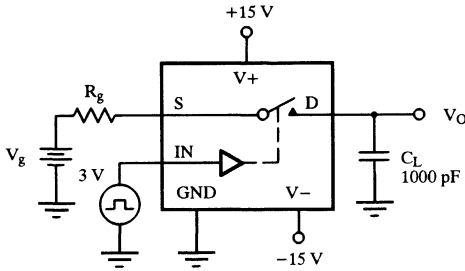


Figure 4. Channel-to-Channel Crosstalk

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## Test Circuits (Cont'd)



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $\Delta Q = C_L \times \Delta V_O$

Figure 5. Charge Injection

## Application Hints<sup>a</sup>

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15	-15	2.4/0.8	-15 to 15
10	-12	2.4/0.8	-12 to 12
12	-10	2.2/0.6	-10 to 10
8 <sup>b</sup>	-8	2.0/0.5	-8 to 8

Notes:

- Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- Operation below  $\pm 8$  V is not recommended.

## Applications

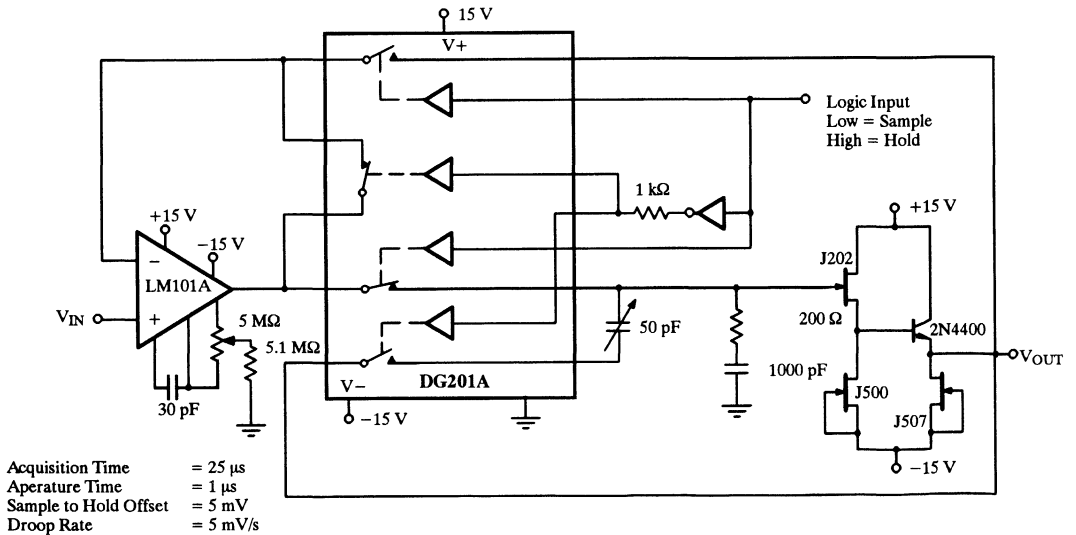
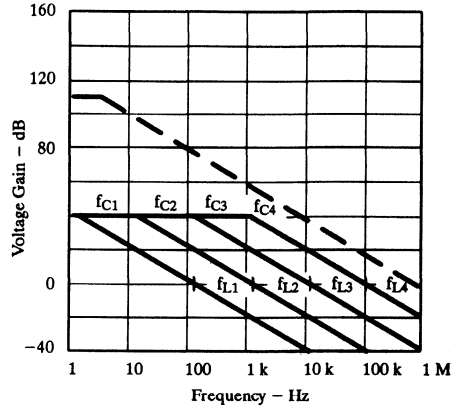
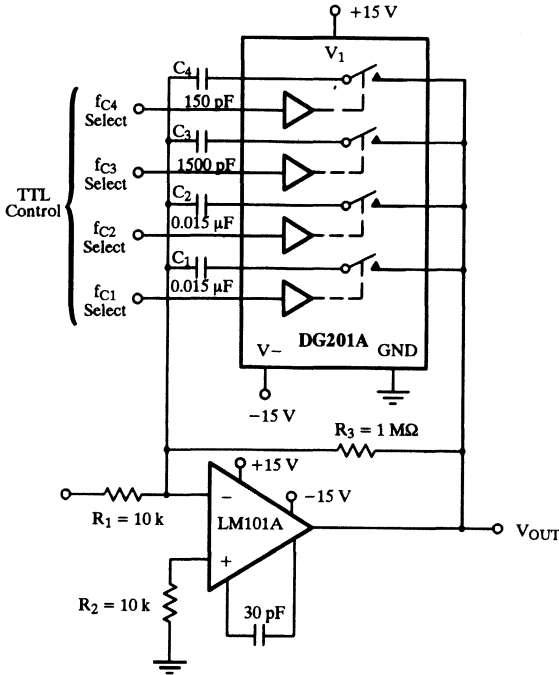


Figure 6. Sample-and-Hold

**Applications (Cont'd)**



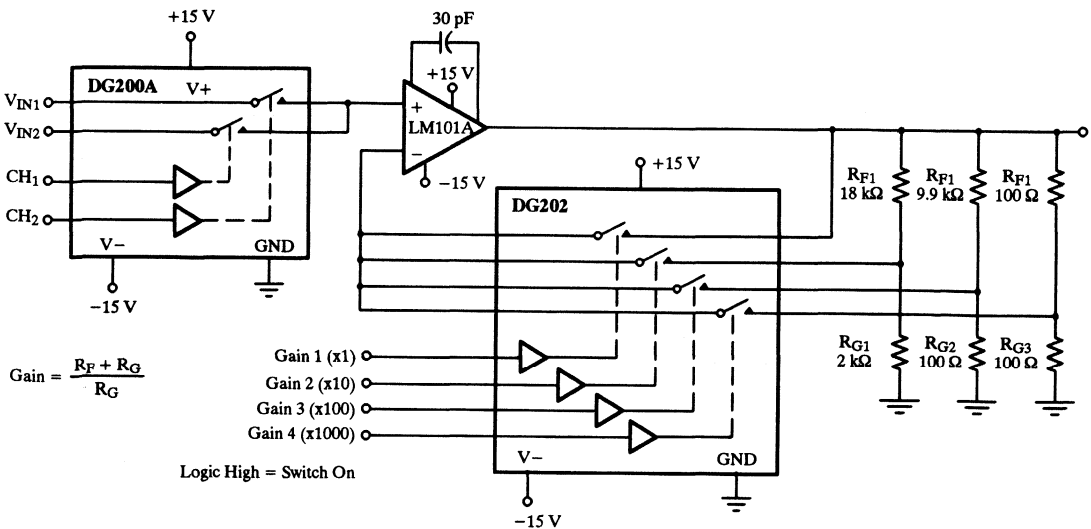
$$A_L \text{ (Voltage Gain Below Break Frequency)} = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (Break Frequency)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (Unity Gain Frequency)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{Max Attenuation} = \frac{f_{DS(on)}}{10 \text{ k}} \approx -40 \text{ dB}$$

**Figure 7.** Active Low Pass Filter with Digitally Selected Break Frequency



$$\text{Gain} = \frac{R_F + R_G}{R_G}$$

Logic High = Switch On

**Figure 8.** A Precision Amplifier with Digitally Programmable Input and Gains

## Improved Quad CMOS Analog Switches

### Features

- $\pm 22\text{-V}$  Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance— $r_{DS(on)}$ :  $45\ \Omega$
- Low Leakage— $I_{D(on)}$ :  $20\ \text{pA}$
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching— $t_{ON}$ :  $120\ \text{ns}$
- Low Glitching— $Q$ :  $1\ \text{pC}$

### Benefits

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG201A/202

### Applications

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

### Description

The DG201B/202B analog switches are highly improved versions of the industry-standard DG201A/202. These devices are fabricated in Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design

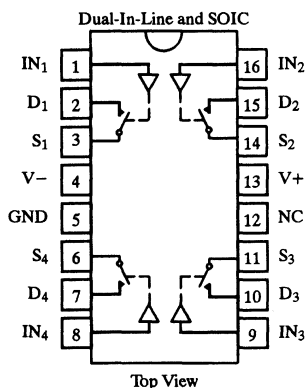
minimizes switching transients. The DG201B and DG202B can handle up to  $\pm 22\text{-V}$  input signals, and have an improved continuous current rating of  $30\ \text{mA}$ . An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply voltages in the off condition.

The DG201B is a normally closed switch and the DG202B is a normally open switch. (See Truth Table.)

### Functional Block Diagram and Pin Configuration

#### DG201B



Truth Table

Logic	DG201B	DG202B
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8\ \text{V}$   
Logic "1"  $\geq 2.4\ \text{V}$

Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
-40 to $85^\circ\text{C}$	16-Pin Plastic DIP	DG201BDJ
		DG202BDJ
	16-Pin CerDIP	DG201BDK
		DG202BDK
	16-Pin Narrow SOIC	DG201BDY
		DG202BDY
-55 to $125^\circ\text{C}$	16-Pin CerDIP	DG201BAK
		DG201BAK/883
		DG202BAK
		DG202BAK/883

**Absolute Maximum Ratings**

Voltages Referenced to V-

V+ ..... 44 V  
 GND ..... 25 V  
 Digital Inputs<sup>a</sup> V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2 V  
 or 30 mA, whichever occurs first

Current, Any Terminal ..... 30 mA

Peak Current, S or D  
 (Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (AK, DK Suffix) ..... -65 to 150°C  
 (DJ, DY Suffix) ..... -65 to 125°C

Power Dissipation (Package)<sup>b</sup>

16-Pin Plastic DIP<sup>c</sup> ..... 470 mW  
 16-Pin Narrow SOIC<sup>d</sup> ..... 640 mW  
 16-Pin CerDIP<sup>e</sup> ..... 900 mW

Notes:

- a. Signals on S<sub>X</sub>, D<sub>X</sub>, or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 6.5 mW/°C above 75°C
- d. Derate 7.6 mW/°C above 75°C
- e. Derate 12 mW/°C above 75°C

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = 1 mA	Room	45		85		85	Ω
			Full				100		
r <sub>DS(on)</sub> Match	Δr <sub>DS(on)</sub>		Room	2					
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room	±0.01	-0.5	0.5	-0.5	0.5	nA
			Full		-20	20	-5	5	
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = ±14 V, V <sub>S</sub> = ∓14 V	Room	±0.01	-0.5	0.5	-0.5	0.5	
			Full		-20	20	-5	5	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V	Room	±0.02	-0.5	0.5	-0.5	0.5	
			Full		-40	40	-10	10	
<b>Digital Control</b>									
Input Voltage High	V <sub>INH</sub>		Full		2.4		2.4		V
Input Voltage Low	V <sub>INL</sub>		Full			0.8		0.8	
Input Current	I <sub>INH</sub> or I <sub>INL</sub>	V <sub>INH</sub> or V <sub>INL</sub>	Full		-1	1	-1	1	μA
Input Capacitance	C <sub>IN</sub>		Room	5					pF
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	V <sub>S</sub> = 2 V See Switching Time Test Circuit	Room	120		300		300	ns
			Full						
Turn-Off Time	t <sub>OFF</sub>		Room	65		200		200	
			Full						
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>g</sub> = 0 V, R <sub>g</sub> = 0 Ω	Room	1					pC
Source-Off Capacitance	C <sub>S(off)</sub>	V <sub>S</sub> = 0 V, f = 1 MHz	Room	5					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room	5					
Channel On Capacitance	C <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V, f = 1 MHz	Room	16					
Off Isolation	OIRR	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω V <sub>S</sub> = 1 V <sub>RMS</sub> , f = 100 kHz	Room	90					dB
Channel-to-Channel Crosstalk	X <sub>TALK</sub>		Room	95					



## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supply</b>									
Positive Supply Current	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			50 100		50 100	$\mu\text{A}$
Negative Supply Current	I-		Room Full		-1 -5		-1 -5		
Power Supply Range for Continuous Operation	V <sub>OP</sub>		Full		±4.5	±22	±4.5	±22	V

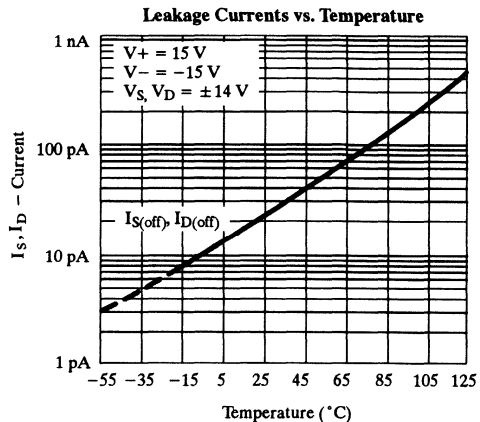
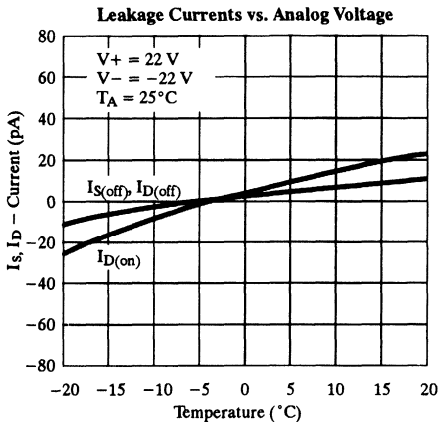
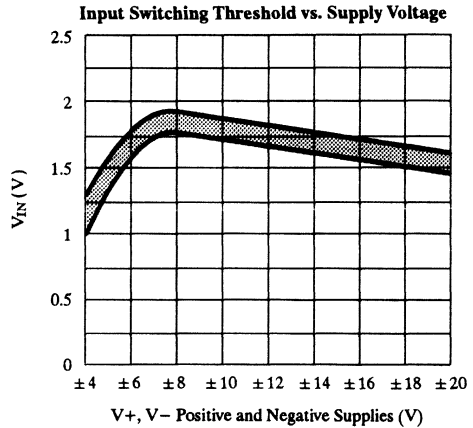
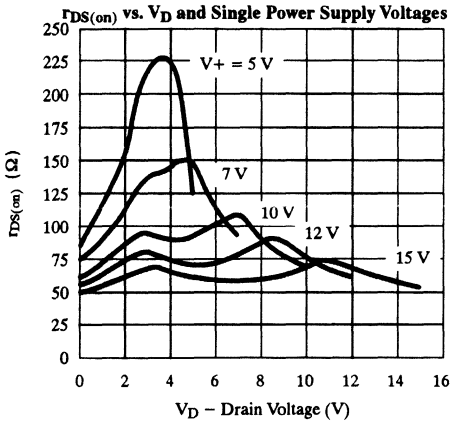
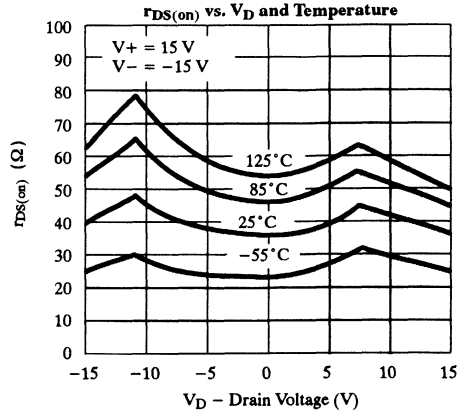
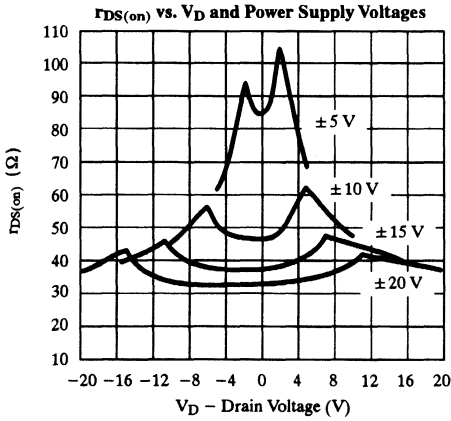
## Specifications<sup>a</sup> for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		0	12	0	12	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	$V_D = 3\text{ V}, 8\text{ V}, I_S = 1\text{ mA}$	Room Full	90		160 200		160 200	$\Omega$
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	$V_S = 8\text{ V}$ See Switching Time Test Circuit	Room	120		300		300	ns
Turn-Off Time	t <sub>OFF</sub>		Room	60		200		200	
Charge Injection	Q	$C_L = 1\text{ nF}, V_{gen} = 6\text{ V}, R_{gen} = 0\ \Omega$	Room	4					pC
<b>Power Supply</b>									
Positive Supply Current	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			50 100		50 100	$\mu\text{A}$
Negative Supply Current	I-		Room Full		-1 -5		-1 -5		
Power Supply Range for Continuous Operation	V <sub>OP</sub>		Full		+4.5	+25	+4.5	+25	V

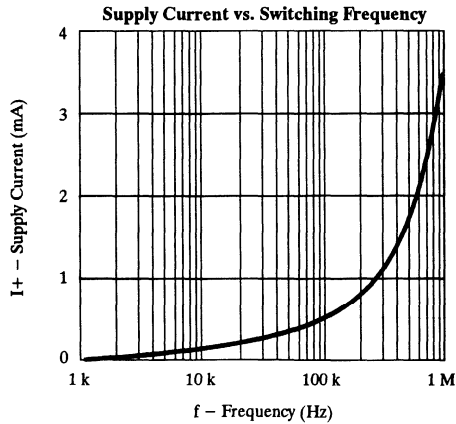
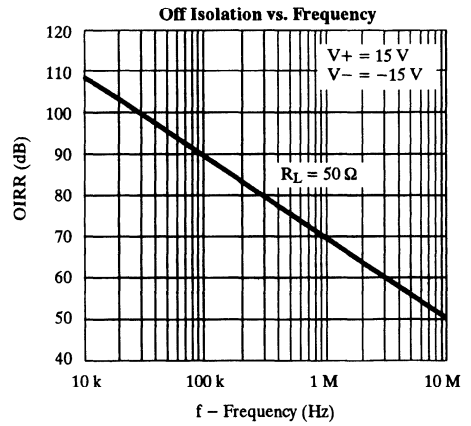
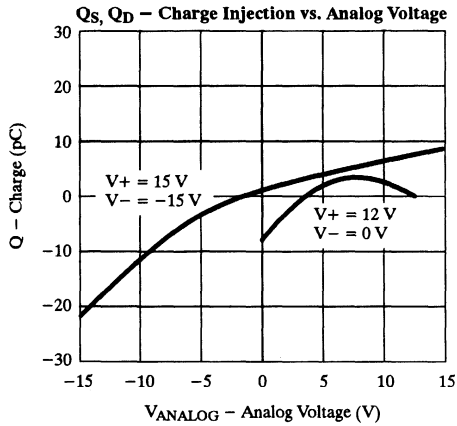
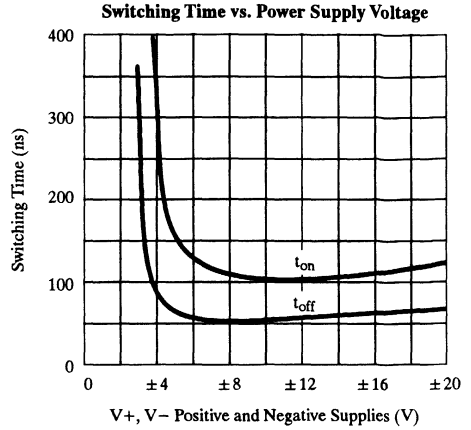
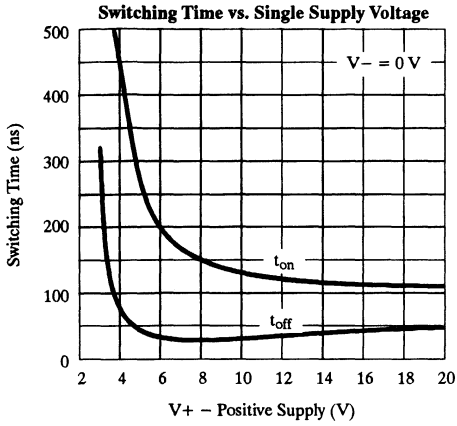
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**



## Typical Characteristics (Cont'd)





**Schematic Diagram (Typical Channel)**

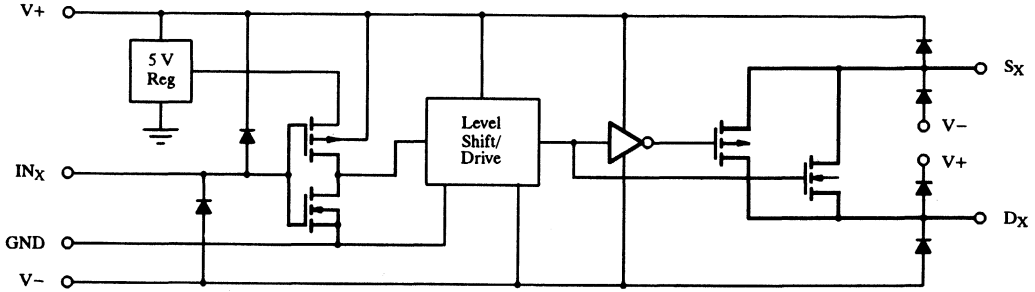


Figure 1.

**Test Circuits**

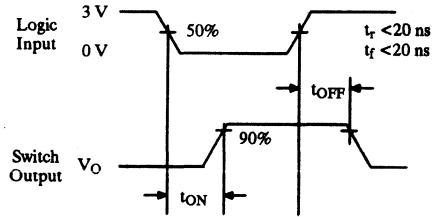
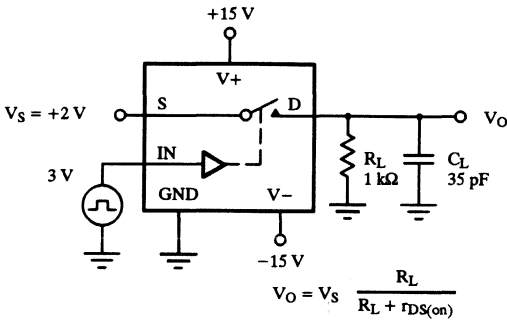


Figure 2. Switching Time

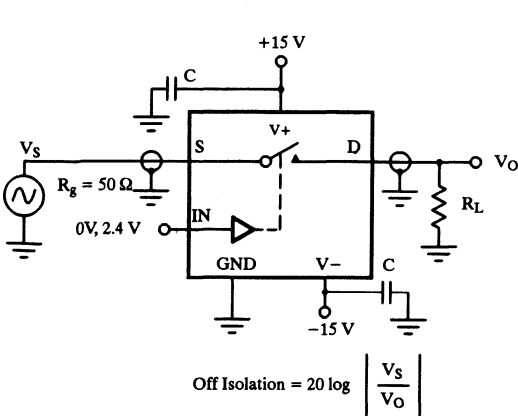


Figure 3. Off Isolation

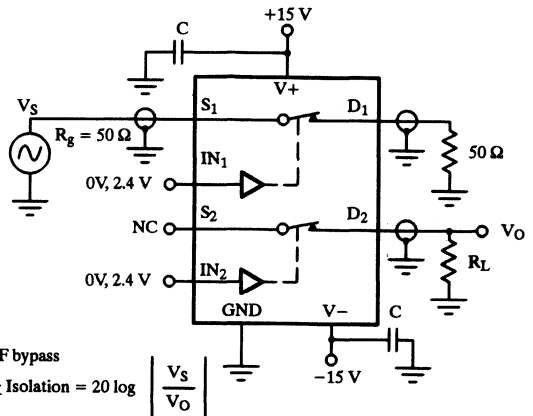


Figure 4. Channel-to-Channel Crosstalk

# DG201B/202B

## Test Circuits (Cont'd)

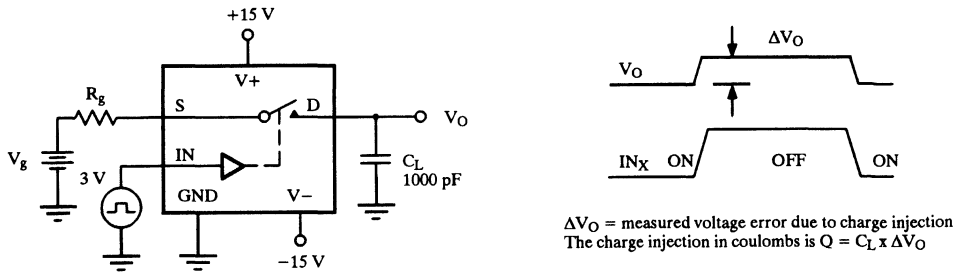


Figure 5. Charge Injection

## Applications

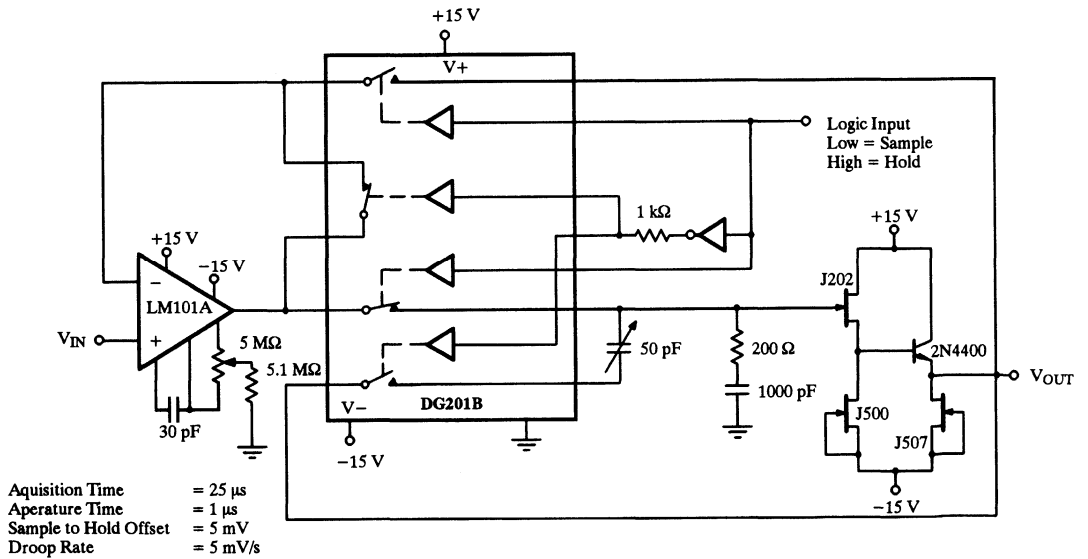
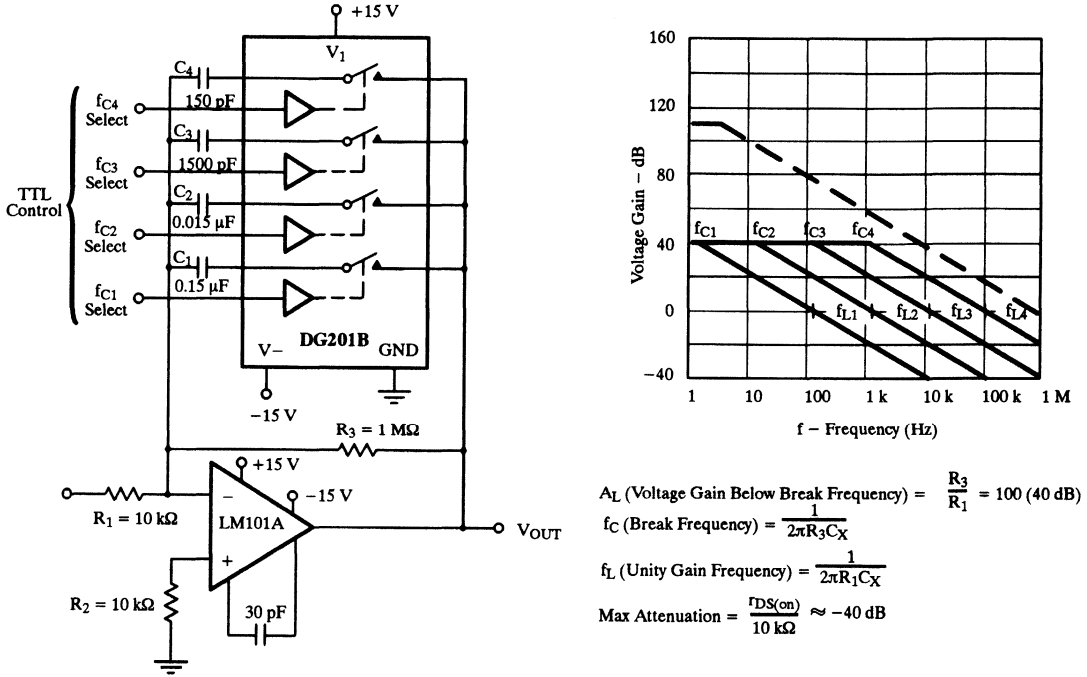
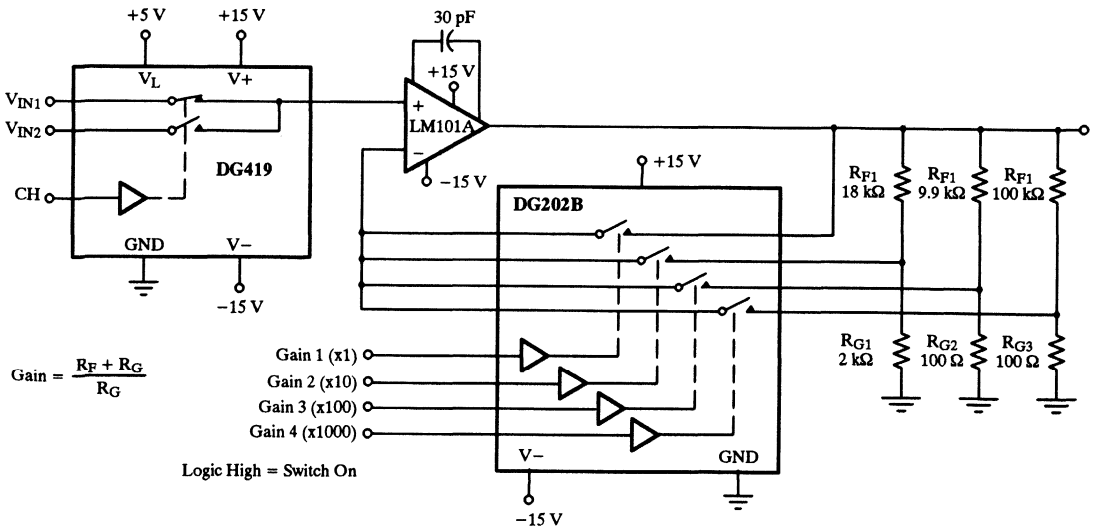


Figure 6. Sample-and-Hold

**Applications (Cont'd)**



**Figure 7.** Active Low Pass Filter with Digitally Selected Break Frequency



**Figure 8.** A Precision Amplifier with Digitally Programmable Input and Gains

## High-Speed Quad SPST CMOS Analog Switch

### Features

- Fast Switching— $t_{ON}$ : 38 ns
- Low On-Resistance: 25  $\Omega$
- Low Leakage: 100 pA
- Low Charge Injection
- TTL/CMOS Logic Compatible
- Single Supply Compatibility
- High Current Rating: -30 mA

### Benefits

- Faster Throughput
- Higher Accuracy
- Reduced Pedestal Error
- Upgrades Existing Designs
- Simple Interfacing
- Replaces HI201HS, ADG201HS

### Applications

- Data Acquisition
- Hi-Rel Systems
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Integrator Reset Circuits
- Choppers
- Gain Switching
- Avionics

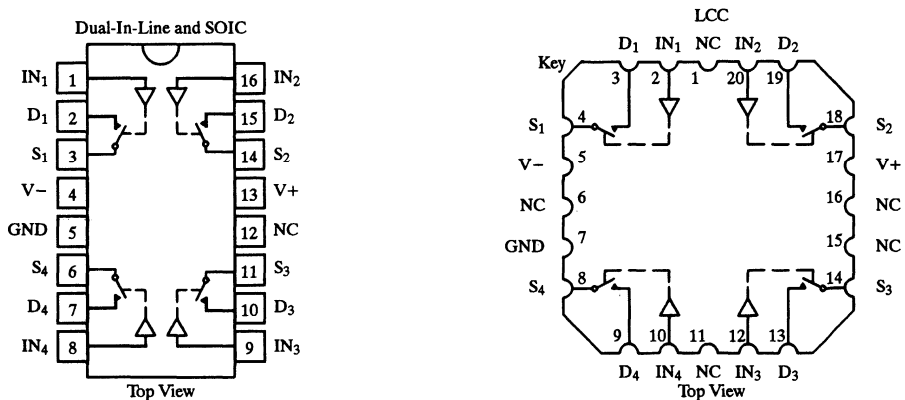
### Description

The DG201HS is an improved monolithic device containing four independent analog switches. It is designed to provide high speed, low error switching of analog signals. Combining low on-resistance (25  $\Omega$ ) with high speed ( $t_{ON}$ : 38 ns), the DG201HS is ideally suited for high speed data acquisition requirements.

To achieve high voltage ratings and superior switching performance, the DG201HS is built on a proprietary high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply values, when off.

### Functional Block Diagram and Pin Configuration



#### Ordering Information

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG201HSDJ
	16-Pin Narrow SOIC	DG201HSDY
-55 to 125°C	16-Pin CerDIP	DG201HSAK/883
	LCC-20	DG201HSAZ/883

#### Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0"  $\leq$  0.8 V  
Logic "1"  $\geq$  2.4 V  
Switches Shown for Logic "1" Input

**Absolute Maximum Ratings**

V+ to V- ..... 44 V  
 GND to V- ..... 25 V  
 Digital Inputs<sup>a</sup> V<sub>S</sub>, V<sub>D</sub> ..... (V-) -4 V to (V+) +4 V  
 or 30 mA, whichever occurs first  
 Continuous Current (Any Terminal) ..... 30 mA  
 Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA  
 Storage Temperature (A Suffix) ..... -65 to 150°C  
 (D Suffix) ..... -65 to 125°C  
 Power Dissipation (Package)  
 16-Pin Plastic DIP<sup>c</sup> ..... 470 mW

16-Pin CerDIP<sup>d</sup> ..... 900 mW  
 16-Pin Narrow Body SOIC<sup>c</sup> ..... 600 mW  
 LCC-20<sup>d</sup> ..... 900 mW

**Notes:**

- a. Signals on S<sub>X</sub>, D<sub>X</sub>, or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6 mW/°C above 75°C.
- d. Derate 12 mW/°C above 75°C.
- e. Derate 7.6 mW/°C above 75°C.

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 3 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		V-	V+	V-	V+	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±8.5 V V+ = 13.5 V, V- = -13.5 V	Room Full	25		50 75		50 75	Ω
r <sub>DS(on)</sub> Match			Room	3					%
Switch Off Leakage Current	I <sub>S(off)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ∓15.5 V	Room Full	0.1	-1 -60	1 60	-1 -20	1 20	nA
	I <sub>D(off)</sub>		Room Full	0.1	-1 -60	1 60	-1 -20	1 20	
Channel On Leakage Current	I <sub>D(on)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>S</sub> = V <sub>D</sub> = ∓15.5 V	Room Full	0.1	-1 -60	1 60	-1 -20	1 20	
<b>Digital Control</b>									
Input, High Voltage	V <sub>INH</sub>		Full		2.4		2.4		V
Input, Low Voltage	V <sub>INL</sub>		Full			0.8	0.8		
Input Capacitance	C <sub>in</sub>		Full	5					pF
Input Current	I <sub>INL</sub> or I <sub>INH</sub>	V <sub>IN</sub> under test = 0.8 V, 3 V	Full		-1	1	-1	1	μA
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF V <sub>S</sub> = ±10 V, V <sub>INH</sub> = 3 V See Figure 3	Room Full	38		50 70		50 70	ns
Turn-Off Time	t <sub>OFF1</sub>		Room Full	30		50 70		50 70	
	t <sub>OFF2</sub>		Room	150					
Output Settling Time to 0.1%	t <sub>s</sub>		Room	180					
Charge Injection	Q	C <sub>L</sub> = 1 nF, V <sub>S</sub> = 0 V V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	Room	-5					pC
OFF Isolation	OIRR	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 10 pF f = 100 kHz	Room	85					dB

## Specifications<sup>a</sup> (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 3\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Dynamic Characteristics (Cont'd)</b>									
Crosstalk (Channel-to-Channel)	$X_{TALK}$	Any Other Channel Switches $R_L = 1\text{ k}\Omega, C_L = 10\text{ pF}$ $f = 100\text{ kHz}$	Room	100					dB
Source Off Capacitance	$C_{S(off)}$	$V_S, V_D = 0\text{ V}, f = 1\text{ MHz}$	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	30					
Drain-to-Source Capacitance	$C_{DS(off)}$		Room	0.5					
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room Full	4.5		10		10	mA
Negative Supply Current	$I_-$		Room Full	3.5	-6		-6		
Power Consumption <sup>e</sup>	$P_C$		Full				240		240

## Specifications<sup>a</sup> for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 10.8\text{ V to }16.5\text{ V}$ $V_- = \text{GND} = 0\text{ V}, V_{IN} = 3\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		0	$V_+$	0	$V_+$	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = 8.5\text{ V}$ $V_+ = 10.8\text{ V}$	Room Full	65		90 120		90 120	$\Omega$
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 16.5\text{ V}, V_S = 0.5\text{ V}, 10\text{ V}$ $V_D = 10\text{ V}, 0.5\text{ V}$	Room Full	0.1	-1 -60	1 60	-1 -20	1 20	nA
	$I_{D(off)}$		Room Full	0.1	-1 -60	1 60	-1 -20	1 20	
Channel On Leakage Current	$I_{D(on)} + I_{S(on)}$	$V_+ = 16.5\text{ V}, V_D = 0.5\text{ V}, 10\text{ V}$	Room Full	0.1	-1 -60	1 60	-1 -20	1 20	
<b>Digital Control</b>									
Input, High Voltage	$V_{INH}$		Full		2.4		2.4		V
Input, Low Voltage	$V_{INL}$		Full			0.8		0.8	
Input Capacitance	$C_{in}$		Full	5					pF
Input Current	$I_{INL}$ OR $I_{INH}$	$V_+ = 16.5\text{ V}$ $V_{IN}$ under test = 0.8 V, 3 V	Full		-1	1	-1	1	$\mu\text{A}$
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}, V_S = 2\text{ V}$ $V_- = 10.8\text{ V}, \text{ See Figure 3}$	Room Full			50 70		50 70	ns
Turn-Off Time	$t_{OFF1}$		Room Full			50 70		50 70	
	$t_{OFF2}$		Room	150					

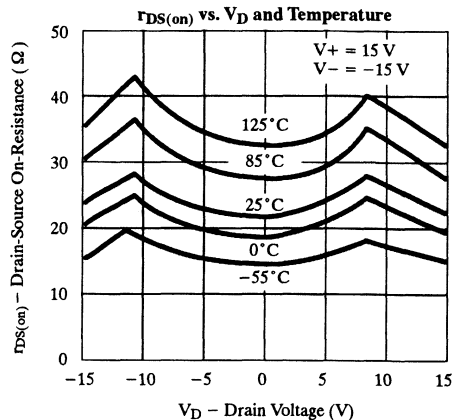
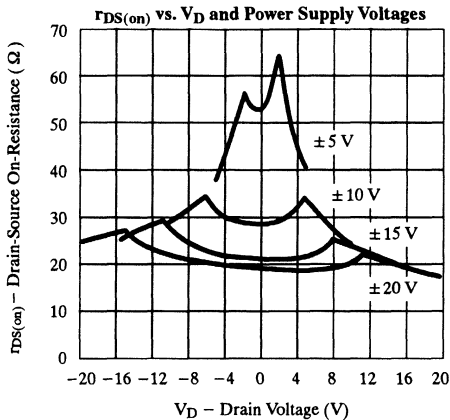
**Specifications<sup>a</sup> for Single Supply**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 10.8\text{ V to }16.5\text{ V}$ $V_- = \text{GND} = 0\text{ V}, V_{IN} = 3\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Dynamic Characteristics (Cont'd)</b>									
Output Settling Time to 0.1%	$t_s$		Room	180					ns
Charge Injection	Q	$C_L = 1\text{ nF}, V_S = 0\text{ V}$ $V_{gen} = 0\text{ V}, R_{gen} = 0\ \Omega$	Room	10					pC
Off Isolation	OIRR	$R_L = 1\text{ k}\Omega, C_L = 10\text{ pF}$ $f = 100\text{ kHz}$	Room	85					dB
Crosstalk (Channel-to-Channel)	X <sub>TALK</sub>	Any Other Channel Switches $R_L = 1\text{ k}\Omega, C_L = 10\text{ pF}, f = 100\text{ kHz}$	Room	100					
Source Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	10					pF
Drain Off Capacitance	$C_{D(off)}$		Room	10					
Channel On Capacitance	$C_{D(on)}$	$V_{ANALOG} = 0\text{ V}$	Room	30					
<b>Power Supplies</b>									
Positive Supply Current	I <sup>+</sup>	$V_+ = 15\text{ V}, V_{IN} = 0\text{ or }5\text{ V}$	Full			10		10	mA
Power Consumption <sup>c</sup>	P <sub>C</sub>		Full			150		150	mW

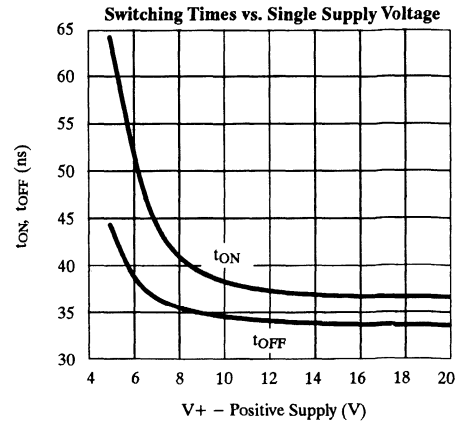
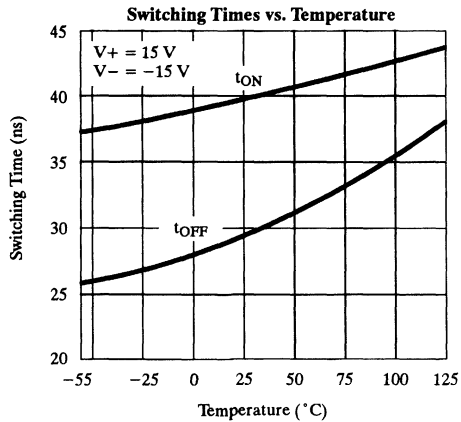
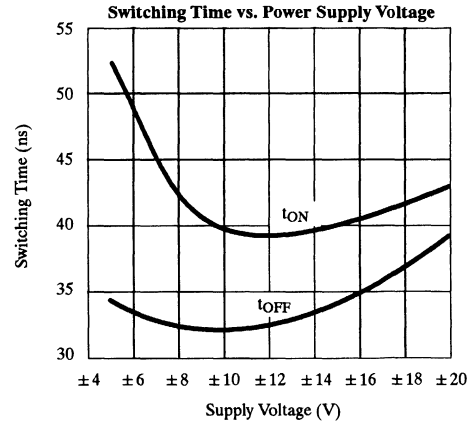
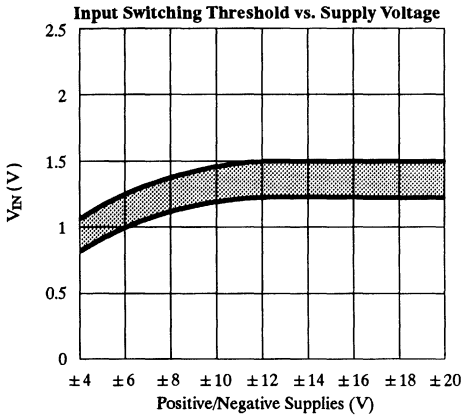
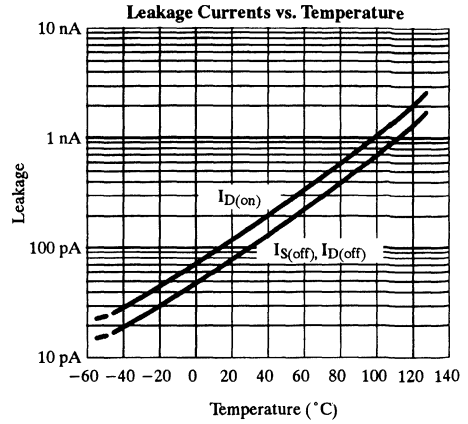
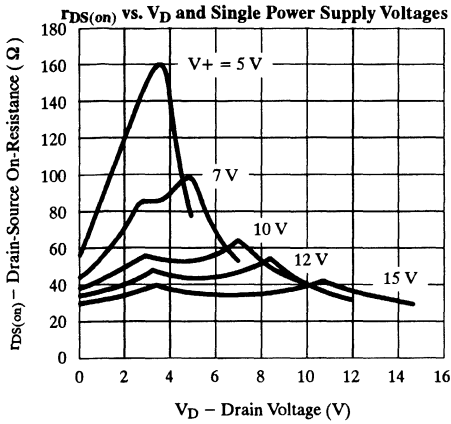
Notes:

- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**

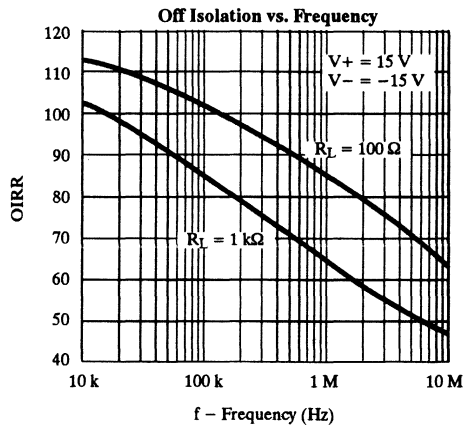
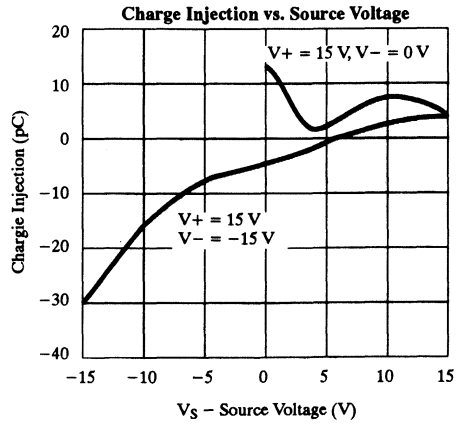
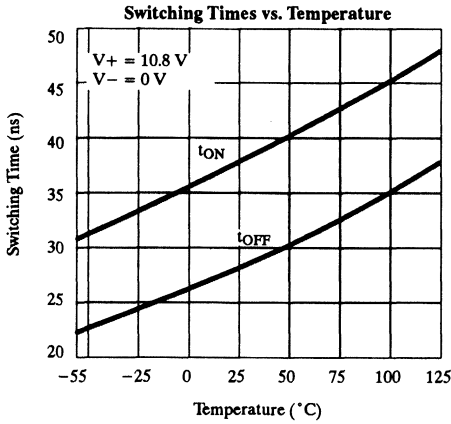


## Typical Characteristics (Cont'd)

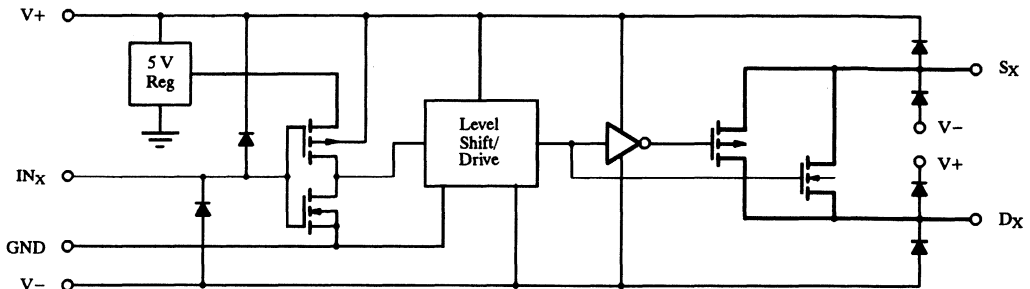




**Typical Characteristics (Cont'd)**

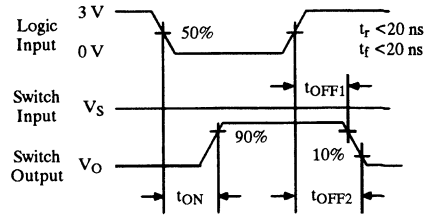
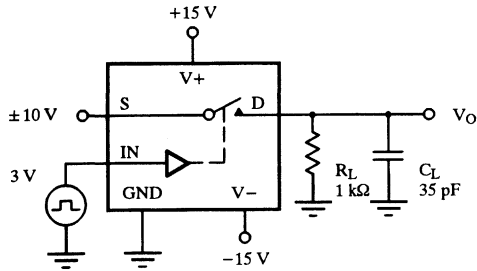


**Test Circuits**



**Figure 1.**

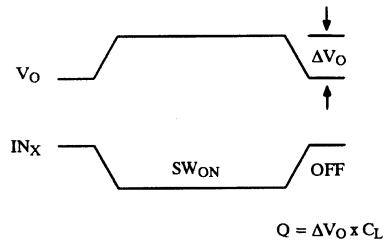
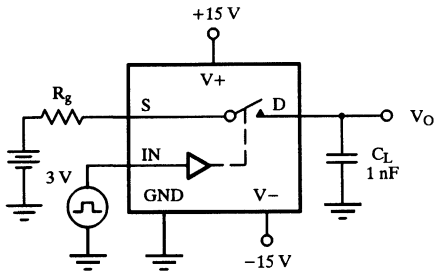
## Test Circuits (Cont'd)



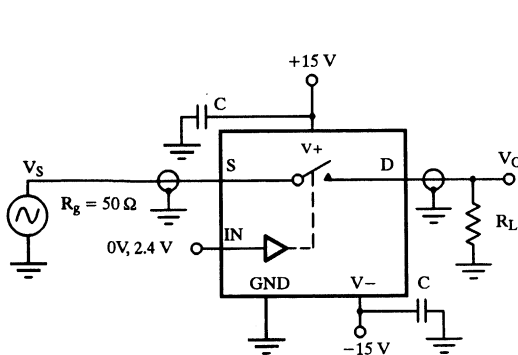
$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

**Figure 2.** Switching Time

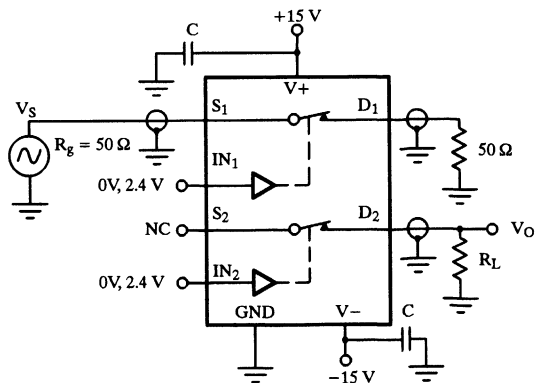


**Figure 3.** Charge Injection



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

**Figure 4.** Off Isolation



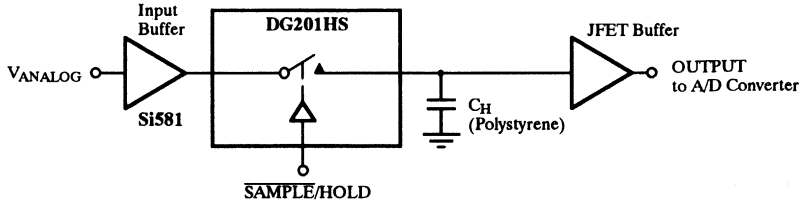
$$X_{\text{TALK}} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

$C = \text{RF bypass}$

**Figure 5.** Crosstalk

## Applications

A high-speed, low-glitch analog switch such as Siliconix's DG201HS improves the accuracy and shortens the acquisition and settling times of a sample-and-hold circuit.



## Low Cost Monolithic Quad SPST CMOS Analog Switches

### Features

- $\pm 15\text{-V}$  Analog Signal Range
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- On-Resistance— $r_{DS(on)}$ : 115  $\Omega$

### Benefits

- Wide Signal Range
- Simple Logic Interface
- Reduced Power Consumption

### Applications

- Disk Drives
- Test Equipment
- Communication Systems
- Sample-and-Holds

### Description

The DG211 and DG212 are low cost quad single-pole single-throw analog switches for use in general purpose switching applications in communication, instrumentation and process control. These devices differ only in that the digital control logic is inverted (see Truth Table). The use of both p- and n-channel devices minimizes on-resistance variation over the analog signal range.

voltage rating of 40 V, both switches will handle  $\pm 15\text{-V}$  input signals with ease, and have a continuous current rating of 20 mA. An epitaxial layer prevents latchup.

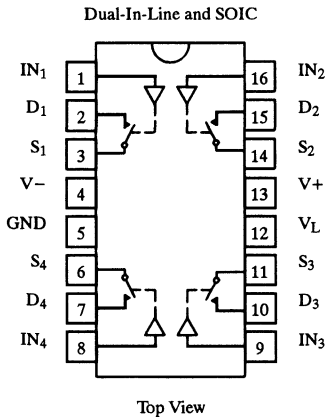
Both devices feature true bi-directional performance (with no offset voltage) in the on condition, and will block signals to 30 V peak-to-peak in the off condition.

Designed with the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown

For new designs we recommend the silicon-gate DG211A/212A upgrades.

### Functional Block Diagram and Pin Configuration

#### DG211



#### Truth Table

Logic	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8\text{ V}$   
Logic "1"  $\geq 2.4\text{ V}$

Switches Shown for DG211 Logic "1" Input

#### Ordering Information – DG211/212

Temp Range	Package	Part Number
0°C to 70°C	16-Pin Plastic DIP	DG211CJ
		DG212CJ
-40°C to 85°C	16-Pin Narrow SOIC	DG211DY
		DG212DY

## Absolute Maximum Ratings

V+ to V-	44 V
V <sub>IN</sub> to GND <sup>a</sup>	V-, V+
V <sub>L</sub> to GND	-0.3 V, 25 V
V <sub>S</sub> or V <sub>D</sub> to V+ <sup>a</sup>	0, -40 V
V <sub>S</sub> or V <sub>D</sub> to V- <sup>a</sup>	0, 40 V
V+ to GND	25 V
V- to GND	-25 V
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	70 mA

Storage Temperature	-65 to 125°C
Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	470 mW
16-Pin Narrow SOIC <sup>d</sup>	600 mW

**Notes:**

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C
- Derate 7.6 mW/°C above 75°C

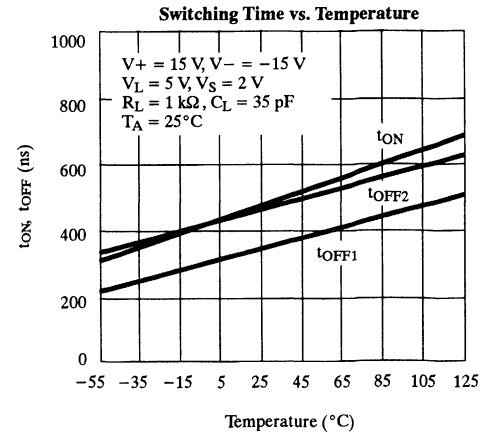
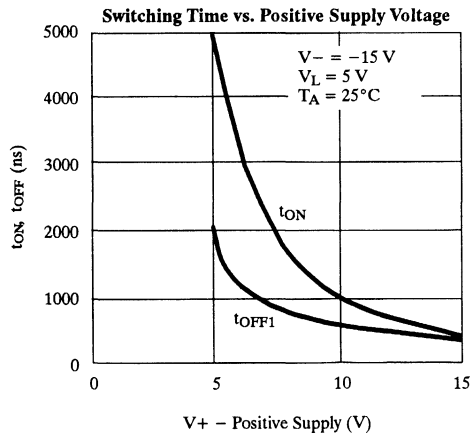
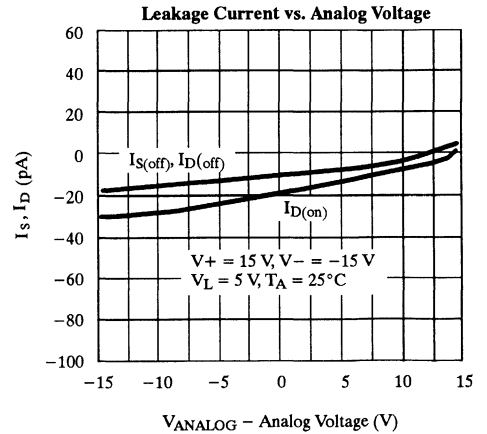
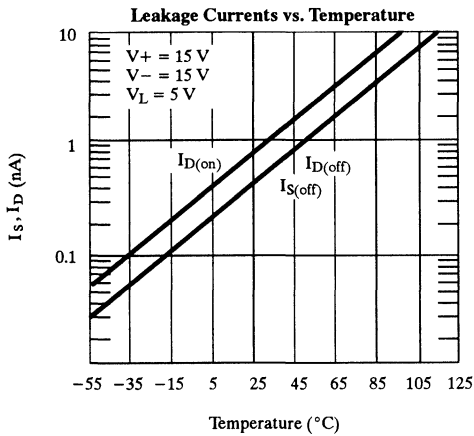
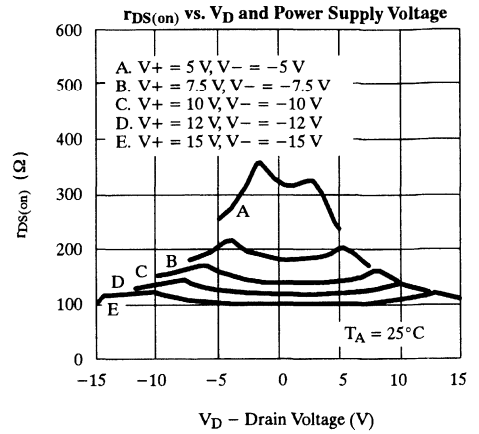
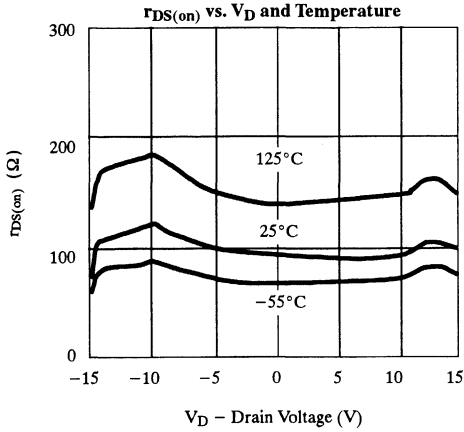
## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	Temp <sup>a</sup>	Limits			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	-15		15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±10 V	Room		115	175	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room	-5	±0.02	5	nA
Drain Off Leakage Current	I <sub>D(off)</sub>		Room	-5	±0.02	5	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = ±14 V	Room	-5	±0.15	5	
<b>Digital Control</b>							
Input Current—Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2.4 V	Room	-1	-0.0004		μA
		V <sub>IN</sub> = 15 V	Room		0.003	1	
Input Current—Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Room	-1	-0.0004		
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	See Switching Time Test Circuit, V <sub>S</sub> = 2 V	Room		460	1000	ns
			Room		360	500	
			Room		450	450	
Turn-Off Time	t <sub>OFF1</sub>	See Switching Time Test Circuit, V <sub>S</sub> = 2 V	Room		5		pF
			Room		5		
Source-Off Capacitance	C <sub>S(off)</sub>	V <sub>S</sub> = 0 V, V <sub>IN</sub> = 5 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room		5		
Channel On Capacitance	C <sub>ON</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V, V <sub>IN</sub> = 0 V, f = 1 MHz	Room		16		
Off Isolation	OIRR	V <sub>IN</sub> = 5 V, R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 15 pF, V <sub>S</sub> = 1 V <sub>RMS</sub> , f = 100 kHz	Room		70		dB
			Room		90		
<b>Power Supplies</b>							
Positive Supply Current	I+	V <sub>IN</sub> = 0 or 5 V	Room		0.35	0.48	mA
Negative Supply Current	I-		Room		0.3	0.48	
Logic Supply Current	I <sub>L</sub>		Room		0.5	1.2	

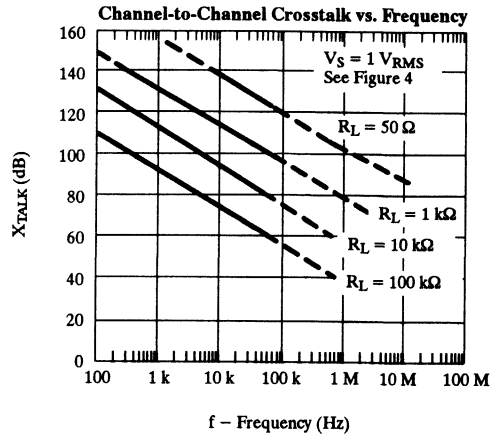
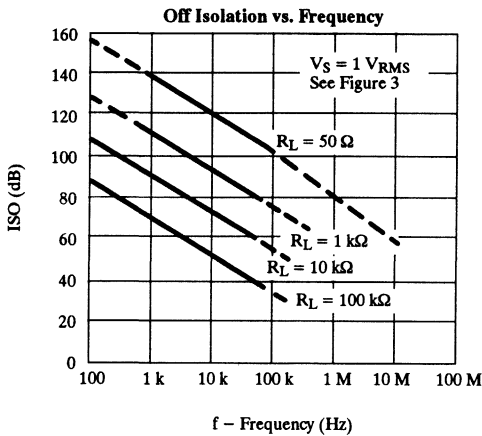
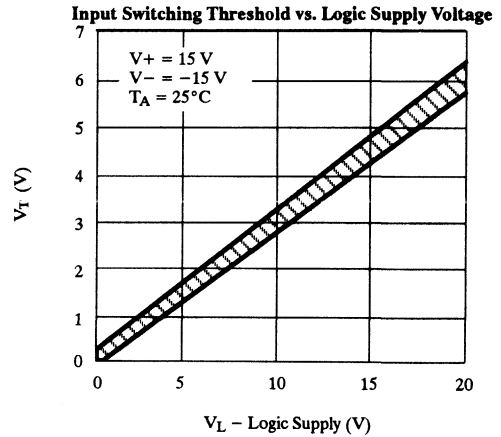
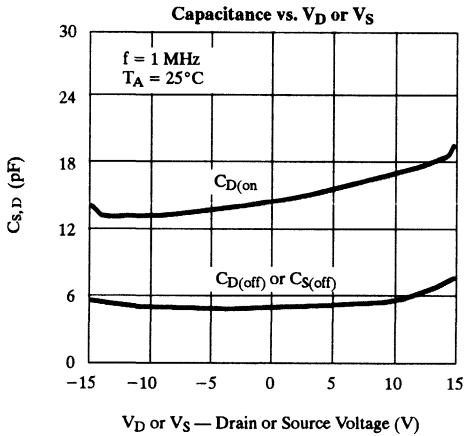
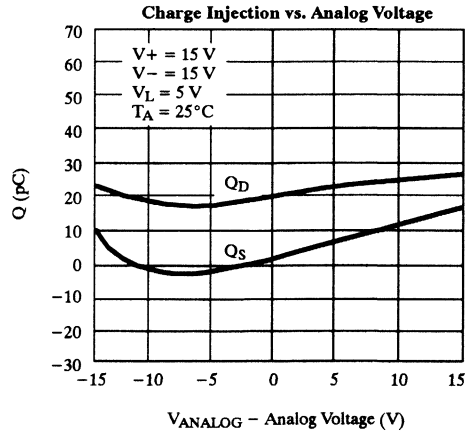
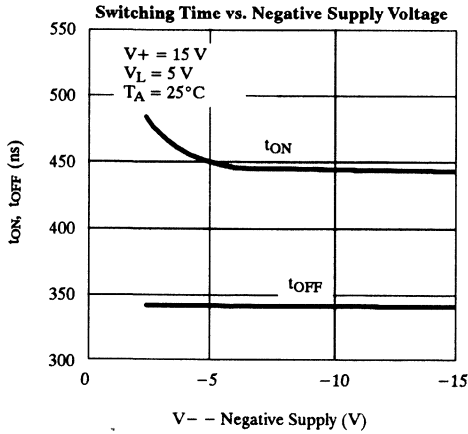
**Notes:**

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

## Typical Characteristics



**Typical Characteristics (Cont'd)**



## Schematic Diagram (Typical Channel)

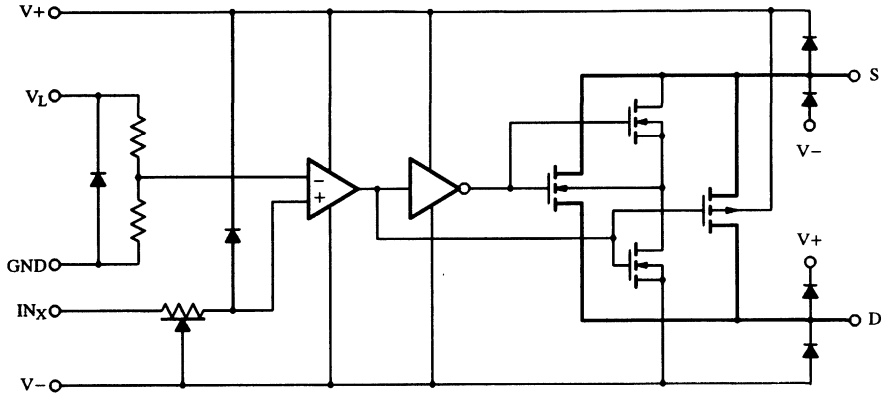


Figure 1.

## Test Circuits

$V_O$  is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

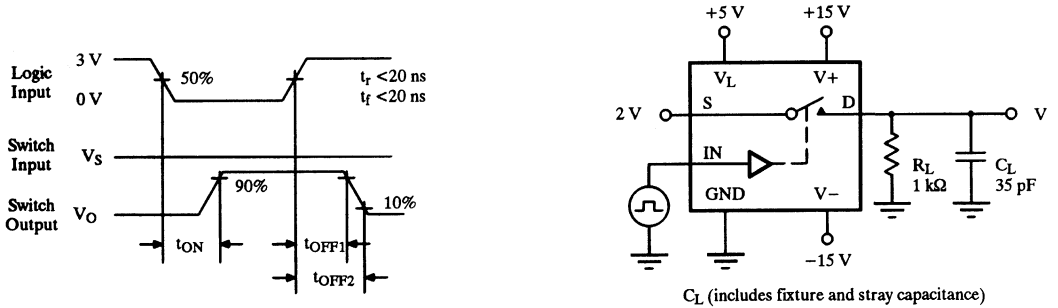


Figure 2. Switching Time

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

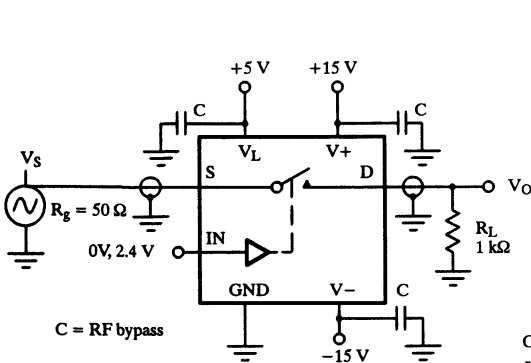


Figure 3. Off Isolation vs. Frequency

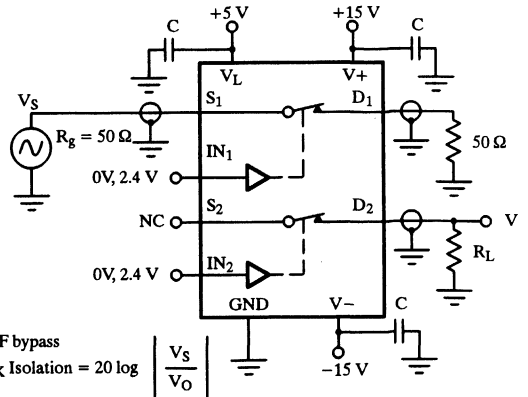


Figure 4. Crosstalk vs. Frequency

$$X_{TALK} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$



**Applications Hints<sup>a</sup>**

Some applications of the DG211 or DG212 will find the logic control inputs  $IN_X$  driven from the output of comparators or op-amps with nearly plus to minus 15-V transitions. In these applications the user can shift the input

logic transition voltage from the normal 1.6 V of TTL to zero volts by connecting the  $V_L$  pin to the GND pin. In this mode of operation the input offset voltage between  $IN_X$  and  $V_L (= GND)$  measures less than  $\pm 500$  mV.

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>L</sub> Logic Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
20	-20	5	2.4/0.8	-20 to 20
15	-15	5	2.4/0.8	-15 to 15
12	-12	5	2.4/0.8	-12 to 12
10	-10	5	2.4/0.8	-10 to 10
8 <sup>b</sup>	-8	5	2.4/0.8	-8 to 8
10	-10	10	5/2	-10 to 10

Notes:

- a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- b. Operation below  $\pm 8$  V is not recommended.

**Applications**

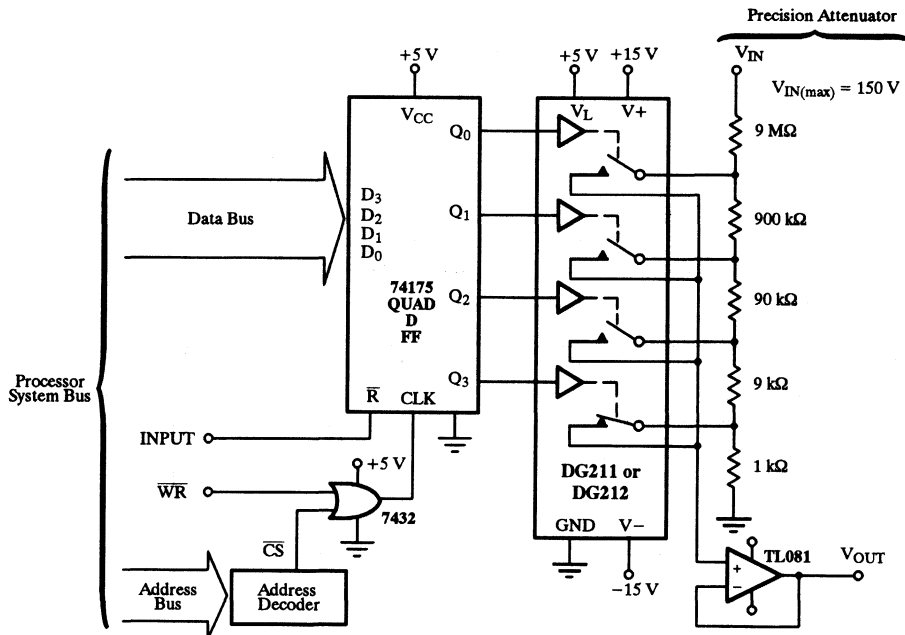


Figure 5. Microprocessor Controlled Analog Signal Attenuator

## Applications (Cont'd)

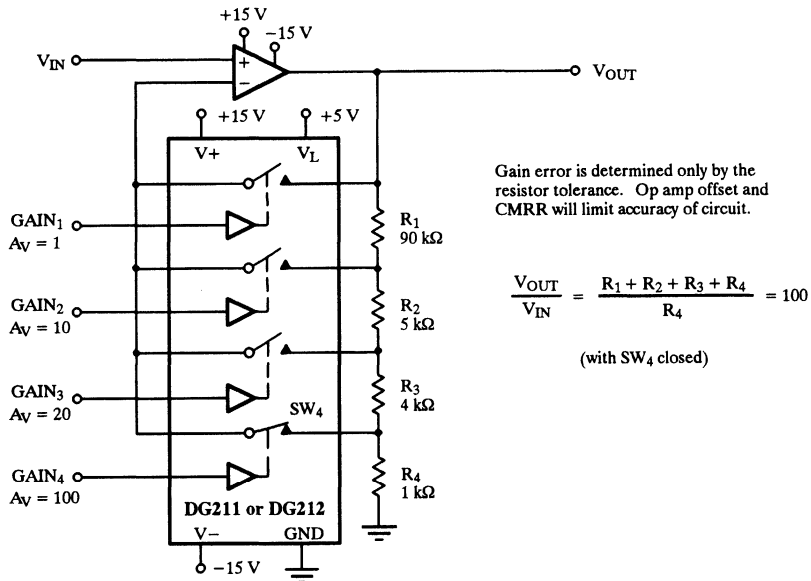


Figure 6. Precision-Weighted Resistor Programmable-Gain Amplifier

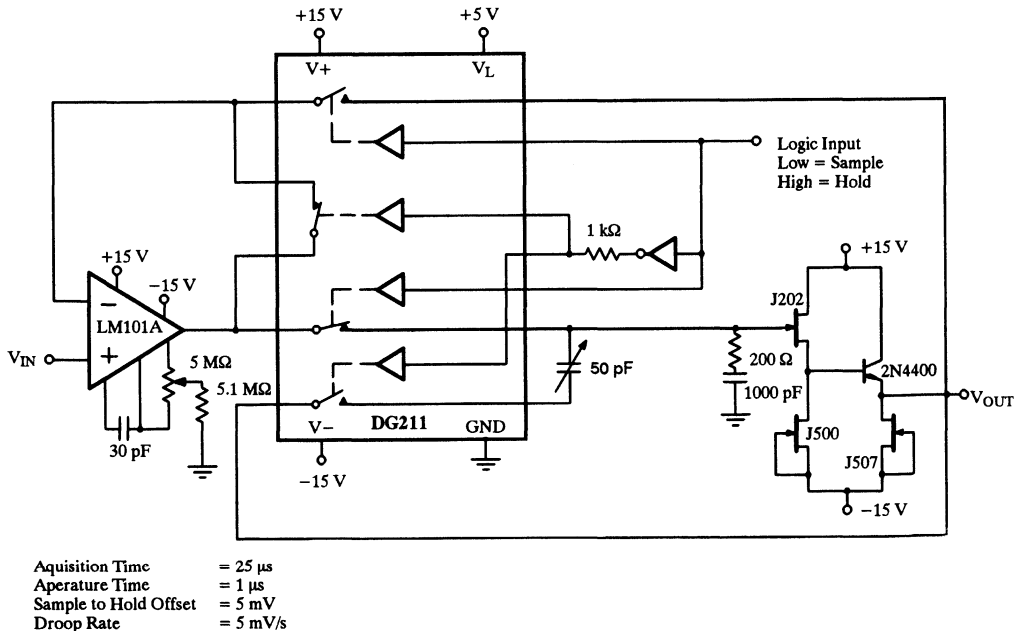
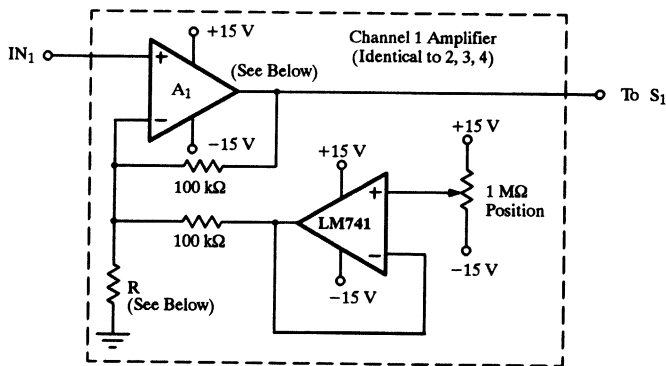
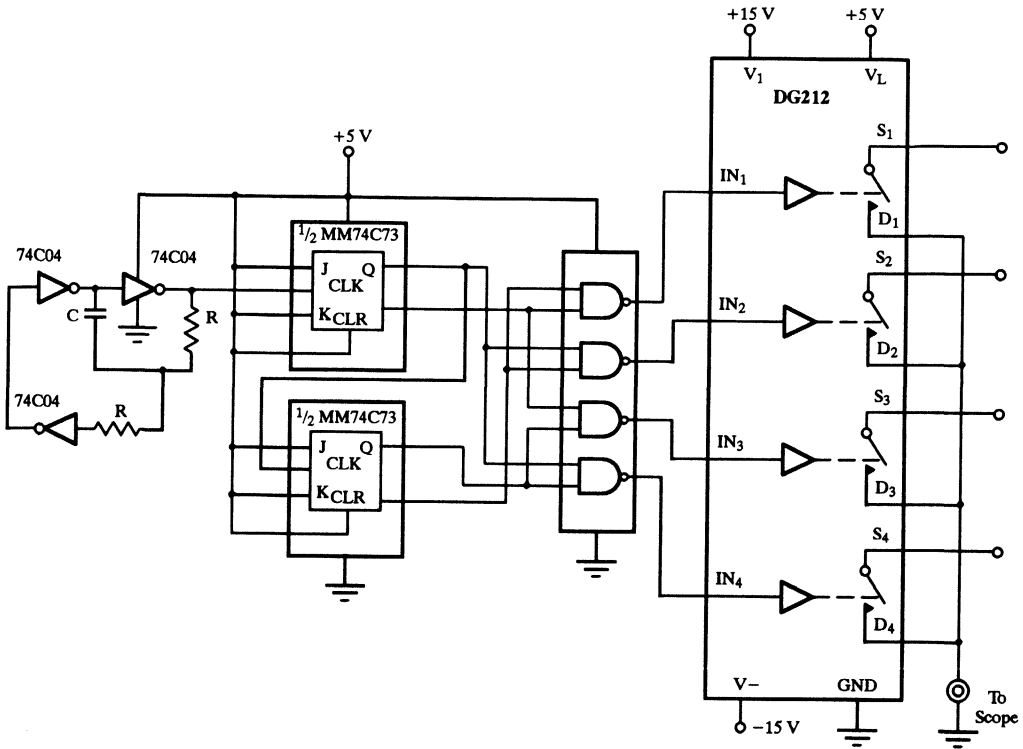


Figure 7. DG211 Sample-and-Hold

**Applications (Cont'd)**



A<sub>1</sub> is op amp with suitable bandwidth, slew rate, etc., for desired signals.  
R is added for extra gain according to formula: Voltage Gain =  $1 + \frac{100 \text{ k}\Omega}{R}$

**Figure 8.** The "Scope Extender" Which Displays 4-Channels Simultaneously on a Single Trace Scope

## Improved Quad CMOS Analog Switches

### Features

- $\pm 22\text{-V}$  Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance— $r_{DS(on)}$ : 50  $\Omega$
- Low Leakage— $I_{D(on)}$ : 20 pA
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching— $t_{ON}$ : 120 ns
- Low Glitching—Q: 1 pC

### Benefits

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG211/212

### Applications

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

### Description

The DG211B/212B analog switches are highly improved versions of the industry-standard DG211/212. These devices are fabricated in Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

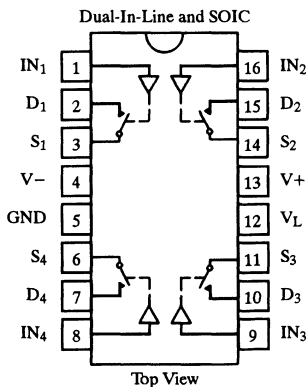
These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design

minimizes switching transients. The DG211B and DG212B can handle up to  $\pm 22\text{ V}$ , and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

The DG211B is a normally closed switch and the DG212B is a normally open switch. (See Truth Table.)

### Functional Block Diagram and Pin Configuration



Truth Table

Logic	DG211B	DG212B
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8\text{ V}$   
Logic "1"  $\geq 2.4\text{ V}$

Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG211BDJ
		DG212BDJ
	16-Pin Narrow SOIC	DG211BDY
		DG212BDY

**Absolute Maximum Ratings**

Voltages Referenced to V-

V+	44 V
GND	25 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Current, Any Terminal	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	100 mA
Storage Temperature	-65 to 125°C

Power Dissipation (Package)<sup>b</sup>

16-Pin Plastic DIP <sup>c</sup>	470 mW
16-Pin Narrow SOIC <sup>d</sup>	640 mW

- Notes:
- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads welded or soldered to PC Board.
  - Derate 6.5 mW/°C above 75°C
  - Derate 7.6 mW/°C above 75°C

**Specifications**

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>L</sub> = 5 V, V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	-15		15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = 1 mA	Room		45	85	Ω
r <sub>DS(on)</sub> Match	Δr <sub>DS(on)</sub>		Full			100	
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room	-0.5	±0.01	0.5	nA
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = ±14 V, V <sub>S</sub> = ∓14 V	Full	-5		5	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V	Full	-10	±0.02	10	
<b>Digital Control</b>							
Input Voltage High	V <sub>INH</sub>		Full	2.4			V
Input Voltage Low	V <sub>INL</sub>		Full			0.8	
Input Current	I <sub>INH</sub> or I <sub>INL</sub>	V <sub>INH</sub> or V <sub>INL</sub>	Full	-1		1	μA
Input Capacitance	C <sub>IN</sub>		Room		5		pF
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>S</sub> = 2 V See Figure 2	Room			300	ns
Turn-Off Time	t <sub>OFF</sub>		Room			200	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>g</sub> = 0 V, R <sub>g</sub> = 0 Ω	Room		1		pC
Source-Off Capacitance	C <sub>S(off)</sub>	V <sub>S</sub> = 0 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room		5		
Channel On Capacitance	C <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V, f = 1 MHz	Room		16		
Off Isolation	OIRR	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω V <sub>S</sub> = 1 V <sub>RMS</sub> , f = 100 kHz	Room		90		dB
Channel-to-Channel Crosstalk	X <sub>TALK</sub>		Room		95		



## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ , $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Power Supply</b>							
Positive Supply Current	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			10 50	$\mu\text{A}$
Negative Supply Current	I-		Room Full	-10 -50			
Logic Supply Current	I <sub>L</sub>	Room Full				10 50	
Power Supply Range for Continuous Operation	V <sub>OP</sub>		Full	± 4		± 22	V

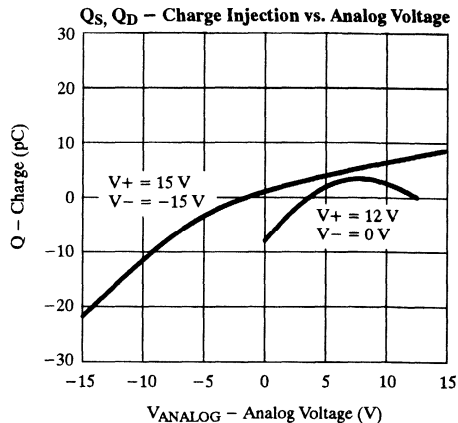
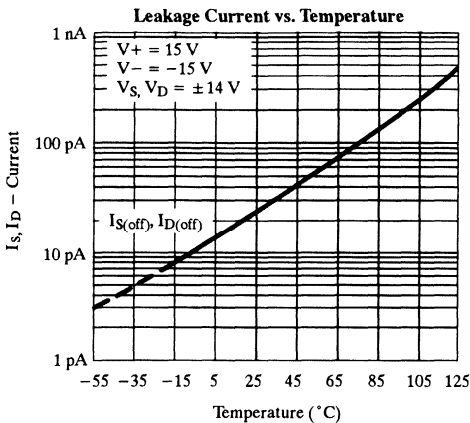
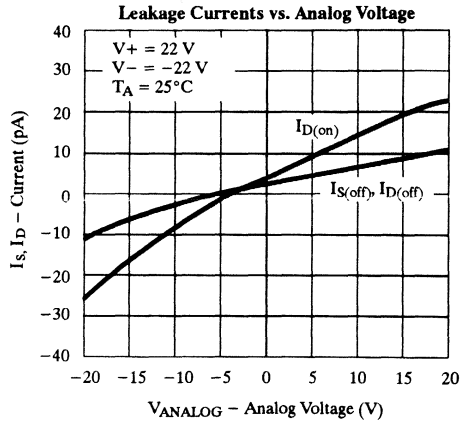
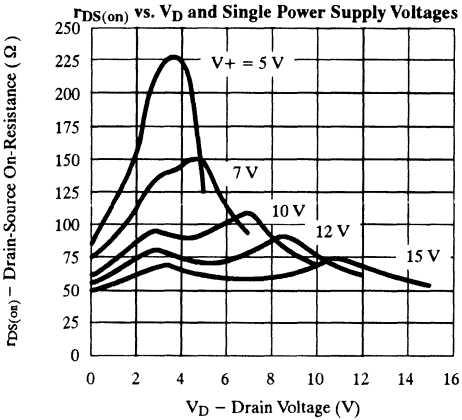
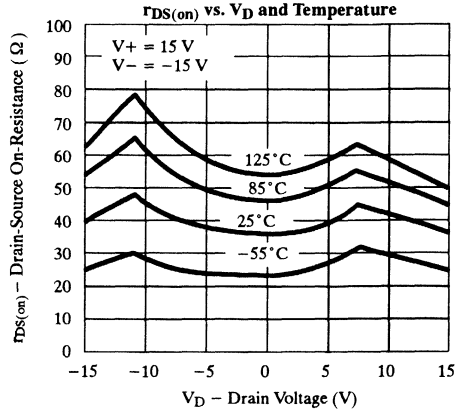
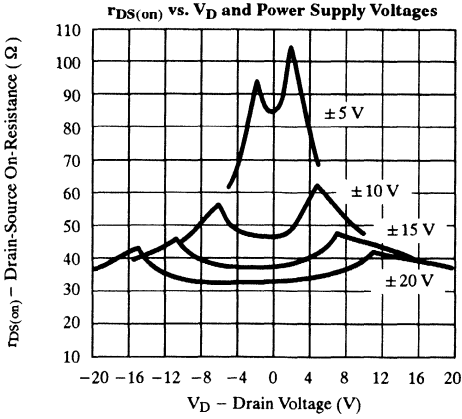
## Specifications for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}$ , $V_- = 0\text{ V}$ $V_L = 5\text{ V}$ , $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	0		12	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	$V_D = 3\text{ V}$ , $8\text{ V}$ , $I_S = 1\text{ mA}$	Room Full		90	160 200	$\Omega$
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	$V_S = 8\text{ V}$ See Figure 2	Room			300	ns
Turn-Off Time	t <sub>OFF</sub>		Room				
Charge Injection	Q	$C_L = 1\text{ nF}$ , $V_{gen} = 6\text{ V}$ , $R_{gen} = 0\ \Omega$	Room		4		pC
<b>Power Supply</b>							
Positive Supply Current	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			10 50	$\mu\text{A}$
Negative Supply Current	I-		Room Full	-10 -50			
Logic Supply Current	I <sub>L</sub>	Room Full				10 50	
Power Supply Range for Continuous Operation	V <sub>OP</sub>		Full	+ 4		+ 44	V

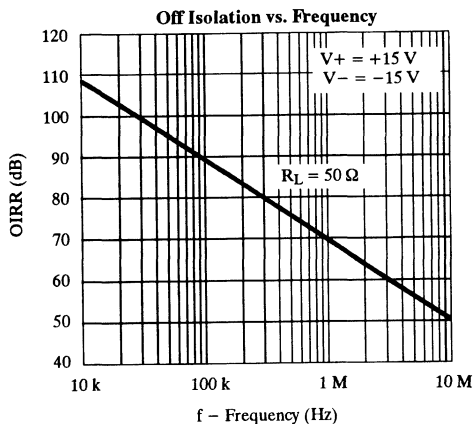
**Notes:**

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**



## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

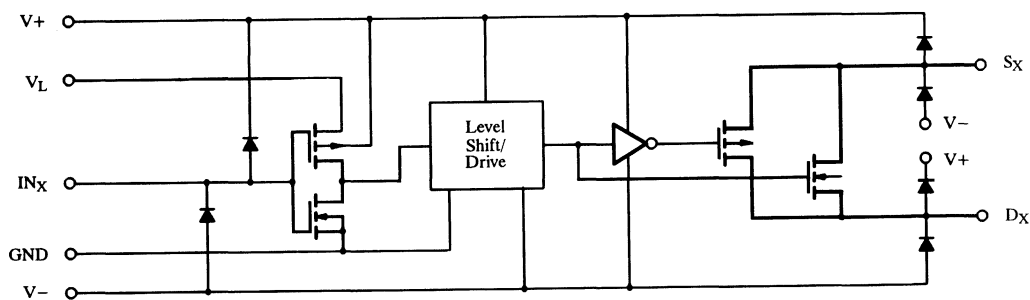


Figure 1.

## Test Circuits

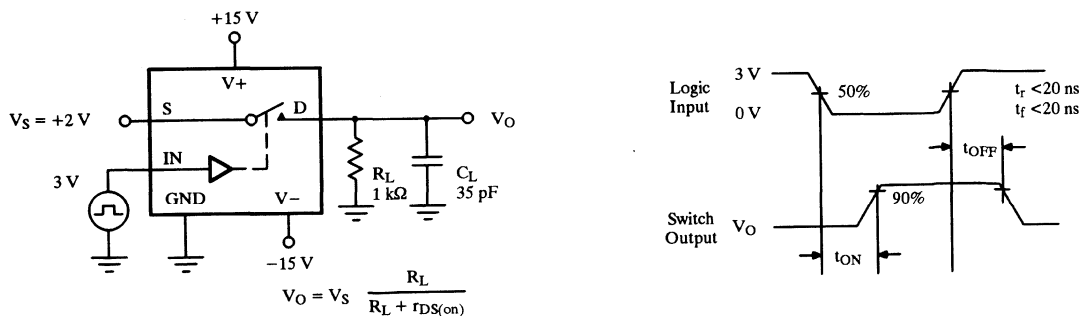


Figure 2. Switching Time



## Test Circuits (Cont'd)

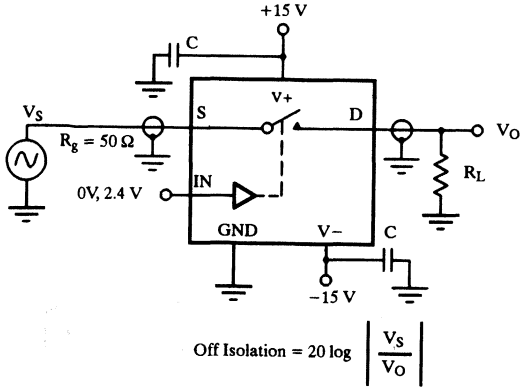


Figure 3. Off Isolation

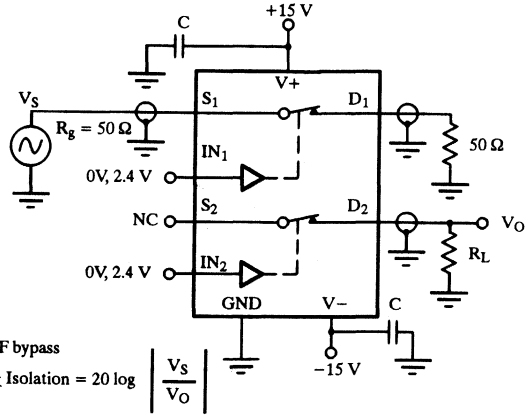


Figure 4. Channel-to-Channel Crosstalk

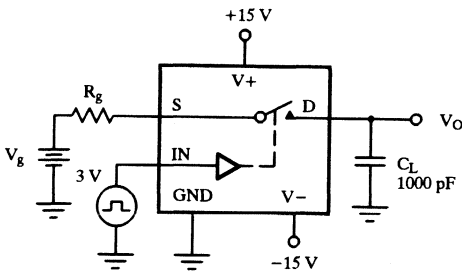
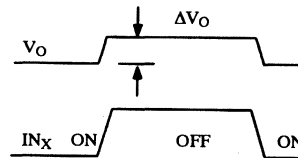


Figure 5. Charge Injection



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

## Applications

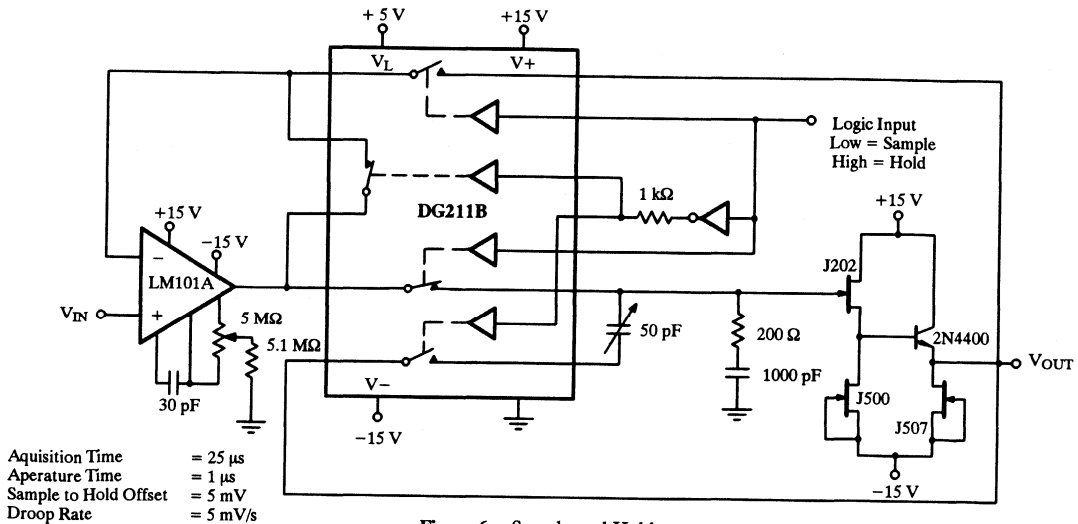
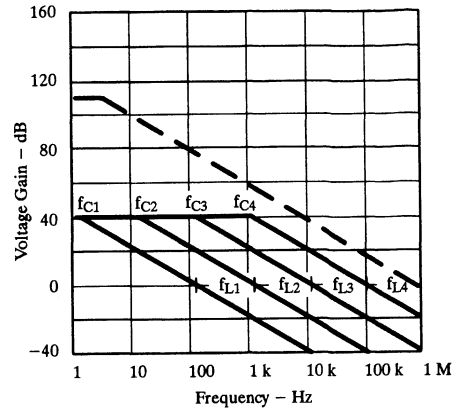
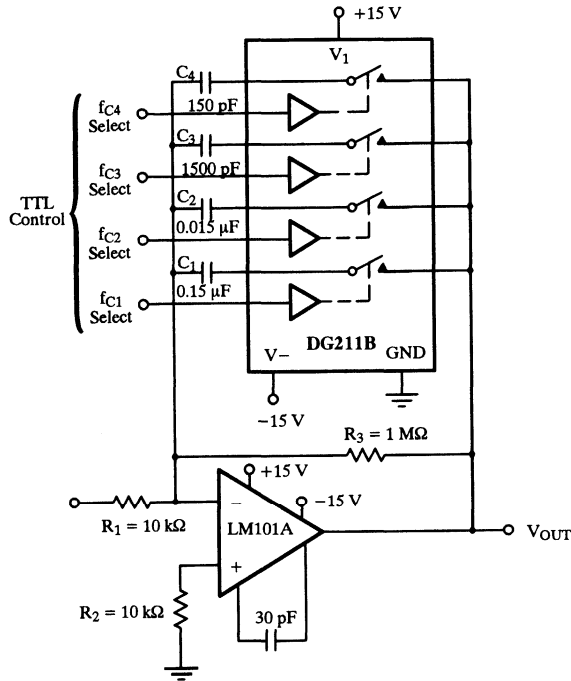


Figure 6. Sample-and-Hold

## Applications (Cont'd)



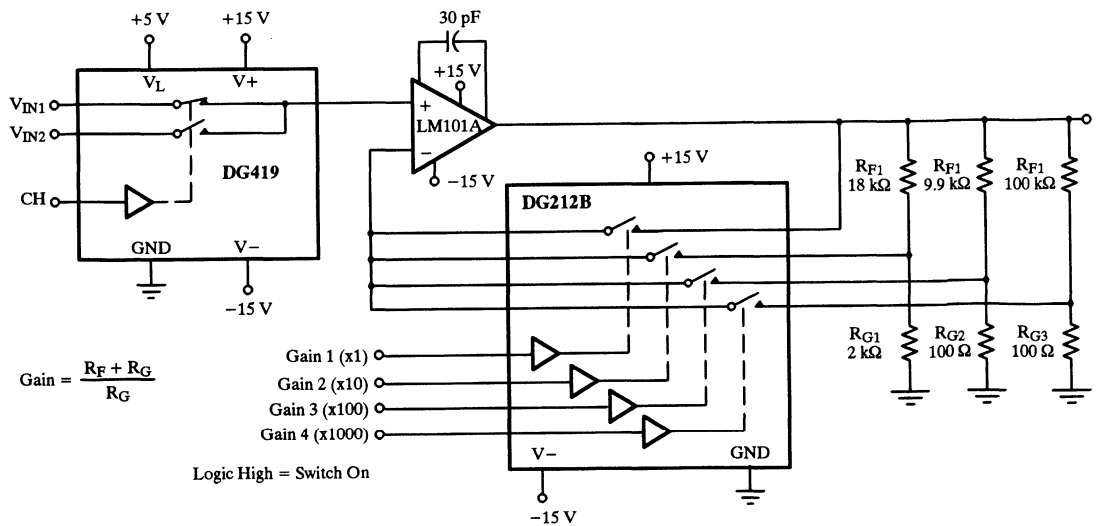
$$A_L \text{ (Voltage Gain Below Break Frequency)} = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (Break Frequency)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (Unity Gain Frequency)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{Max Attenuation} = \frac{r_{DS(on)}}{10 \text{ k}\Omega} \approx -40 \text{ dB}$$

Figure 7. Active Low Pass Filter with Digitally Selected Break Frequency



$$\text{Gain} = \frac{R_F + R_G}{R_G}$$

Logic High = Switch On

Figure 8. A Precision Amplifier with Digitally Programmable Input and Gains

# Quad SPST CMOS Analog Switch with Latches

## Features

- Accepts 150-ns Write Pulse Width
- 5-V On-Chip Regulator
- Built on PLUS-40 Process
- Latches Are Transparent with  $\overline{WR}$  Low
- Low On-Resistance: 60  $\Omega$

## Benefits

- Compatible with Most  $\mu$ P Buses
- Allows Wide Power Supply Tolerance Without Affecting TTL Compatibility
- Reduced Power Consumption
- Allows Flexibility of Design

## Applications

- $\mu$ P Based Systems
- Automatic Test Equipment
- Communication Systems
- Data Acquisition Systems
- Medical Instrumentation
- Factory Automation

## Description

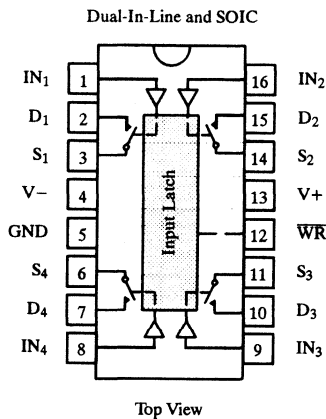
The DG221 is a monolithic quad single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems. Featuring independent onboard latches and a common  $\overline{WR}$  pin, each DG221 can be memory mapped, and addressed as a single data byte for simultaneous switching.

Designed on the Siliconix PLUS-40 CMOS process, the

DG221 combines low power and low on-resistance (60  $\Omega$  typical) while handling continuous currents up to 20 mA. An epitaxial layer prevents latchup.

The device features true bidirectional performance in the on condition. These switches guarantee a rail-to-rail blocking capability (44 V max), in the off condition.

## Functional Block Diagram and Pin Configuration



Four Latchable SPST Switches per Package

Truth Table

$IN_x$	$\overline{WR}$	Switch
0	0	ON
1	0	OFF
X		Control data latched-in, switches on or off as selected by last $IN_x$
X	1	Maintains previous state

Logic "0"  $\leq$  0.8 V  
Logic "1"  $\geq$  2.4 V

Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
0°C to 70°C	16-Pin Plastic DIP	DG221CJ
-40°C to 85°C	16-Pin Narrow SOIC	DG221DY
-55°C to 125°C	16-Pin CerDIP	DG221AK/883

1

## Absolute Maximum Ratings

Voltages Referenced to V-

V+	44 V
GND	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed 1 ms, 10% duty cycle)	70 mA
Storage Temperature:	(AK Suffix) -65 to 150°C (CJ and DY Suffix) -65 to 125°C

Power Dissipation (Package)<sup>b</sup>

16-Pin CerDIP <sup>c</sup>	900 mW
16-Pin Plastic DIP <sup>d</sup>	470 mW
16-Pin SOIC <sup>e</sup>	600 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 12 mW/°C above 75°C
- Derate 6.5 mW/°C above 25°C
- Derate 7.7 mW/°C above 75°C

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 2.4 V, 0.8 <sup>f</sup> V, WR = 0	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±10 V	Room Full	60		90 135		90 135	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room Full	±0.01	-1 -100	1 100	-5 -100	5 100	nA
Drain Off Leakage Current	I <sub>D(off)</sub>		Room Full	±0.02	-1 -100	1 100	-5 -100	5 100	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = ±14 V	Room Full	±0.01	-1 -200	1 200	-5 -200	5 200	
<b>Digital Control</b>									
Input Current	I <sub>INL</sub> , I <sub>INH</sub>	V <sub>IN</sub> = 0 V or = 2.4 V	Room Full	-0.0004	-1 -10	1 10	-1 -10	1 10	μA
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	See Figure 2	Room			550		550	ns
Turn-Off Time	t <sub>OFF</sub>		Room			340		340	
Turn-On Time Write	t <sub>ON</sub> , WR	See Figure 3	Room			550		550	
Turn-Off Time Write	t <sub>OFF</sub> , WR		Room			340		340	
Write Pulse Width	t <sub>w</sub>	See Figure 4	Room	120	150		150		
Input Setup Time	t <sub>s</sub>		Room	130	180		180		
Input Hold Time	t <sub>H</sub>		Full	0	20		20		
Charge Injection	Q	C <sub>L</sub> = 1000 pF V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω	Room	20					pC
Source-Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz, V <sub>S</sub> , V <sub>D</sub> = 0 V	Room	8					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room	9					
Channel-On Capacitance	C <sub>D(on)</sub>		Room	29					
Off Isolation	OIRR	V <sub>S</sub> = 1 V <sub>p-p</sub> , f = 100 kHz C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ	Room	70					dB
Interchannel Crosstalk	X <sub>TALK</sub>		Room	90					

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8^f\text{ V}, WR = 0$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	All Channels On or Off $V_{IN} = 0\text{ V or } 2.4\text{ V}$	Full	0.8		1.5		1.5	mA
Negative Supply Current	I-		Room	-0.4	-1		-1		

Notes:

- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

**Schematic Diagram (Typical Channel)**

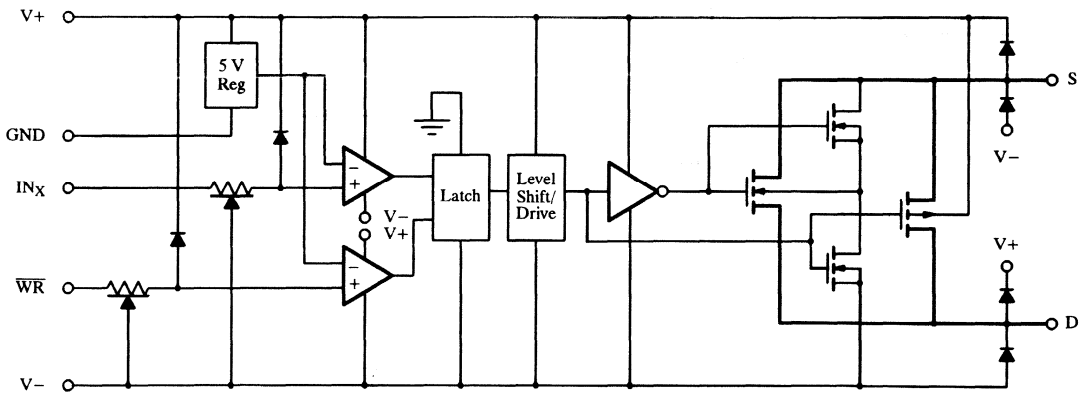
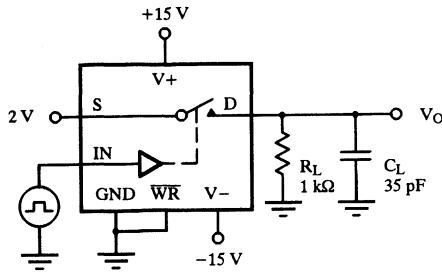


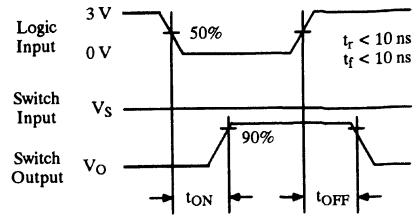
Figure 1.

## Test Circuits

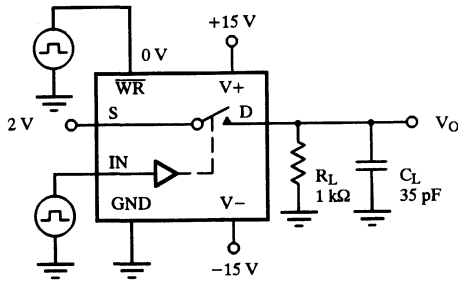


$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

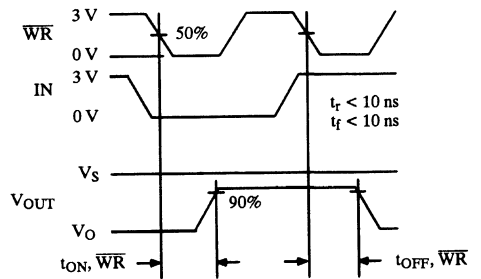


**Figure 2.** Switching Time

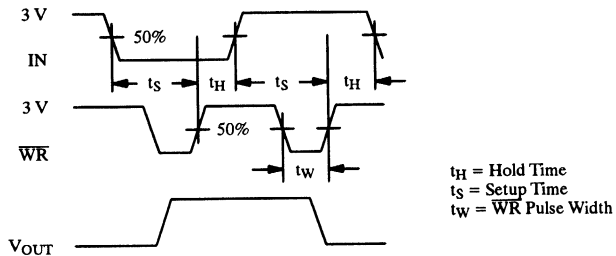


$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



**Figure 3.**  $\overline{WR}$  Switching Time

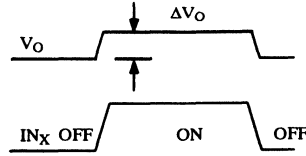
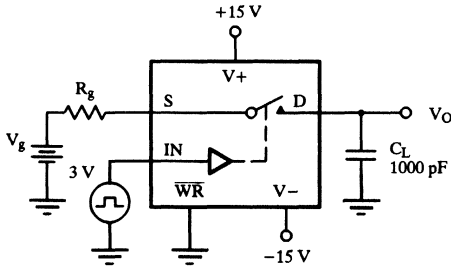


$t_H$  = Hold Time  
 $t_S$  = Setup Time  
 $t_W$  =  $\overline{WR}$  Pulse Width

The latches are level sensitive. When  $\overline{WR}$  is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of  $\overline{WR}$ .

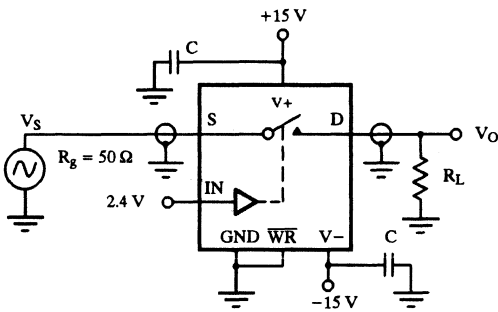
**Figure 4.**  $\overline{WR}$  Setup Conditions

**Test Circuits (Cont'd)**



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

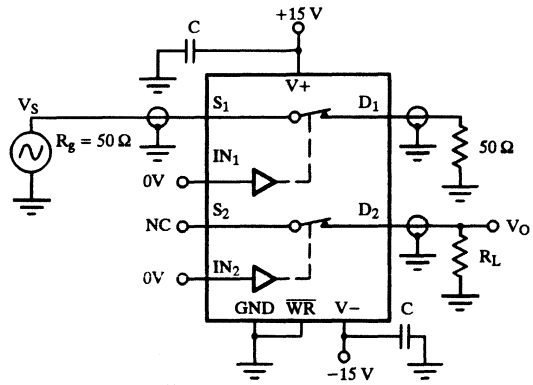
**Figure 5. Charge Injection**



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

**Figure 6. Off Isolation**



$$X_{\text{TALK}} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

**Figure 7. Channel-to-Channel Crosstalk**

**Application Hints<sup>a</sup>**

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND (V)	WR (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15	-15	0	2.4/0.8	2.4/0.8	-15 to 15
20	-20	0	2.4/0.8	2.4/0.8	-20 to 20
10	-10	0	2.4/0.8	2.4/0.8	-10 to 10
10	-5	0	2.4/0.8	2.4/0.8	-5 to 10

Notes:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

## Applications

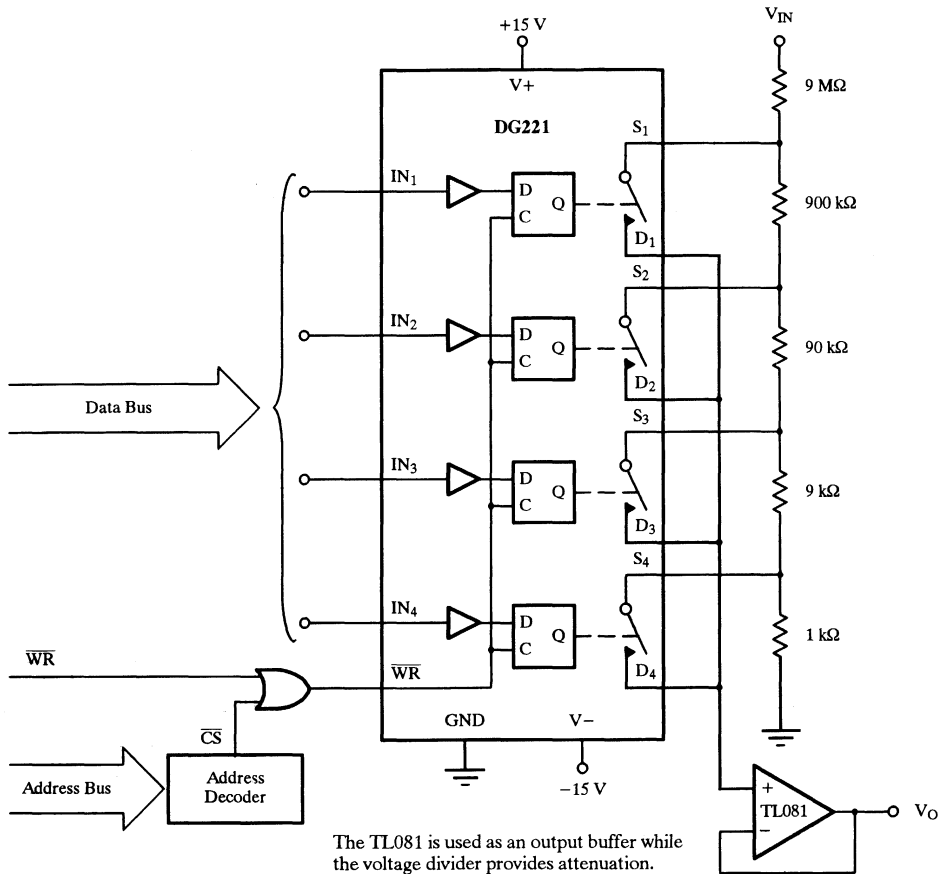


Figure 8.  $\mu$ P-Controlled Analog Signal Attenuator

Truth Table

IN <sub>1</sub>	IN <sub>2</sub>	IN <sub>3</sub>	IN <sub>4</sub>	$\overline{WR}$ <sup>a</sup>	On Switch
0	0	0	0	0	All
1	1	1	1	0	None
0	1	1	1	0	1
1	0	1	1	0	2
1	1	0	1	0	3
1	1	1	0	0	4

Output Attenuation for Figure 8

$\overline{WR}$	IN <sub>1</sub>	IN <sub>2</sub>	IN <sub>3</sub>	IN <sub>4</sub>	Gain
0	0	1	1	1	0.1
0	1	0	1	1	0.01
0	1	1	0	1	0.001
0	1	1	1	0	0.0001

Notes:

- a.  $\overline{WR}$  may be held at "0" for temporary operation similar to DG201A's. With  $\overline{WR}$  at "0" SW<sub>1</sub> will remain on as long as IN<sub>1</sub> is held at "0".



# General Purpose Monolithic Dual SPDT CMOS Analog Switch

## Features

- PLUS-40 Process
- Make-Before-Break Operation
- Full Rail-to-Rail Analog Signal Range
- True TTL Compatibility
- Low  $r_{DS(on)}$ : 30  $\Omega$

## Benefits

- Low Power
- Reduced Switching Noise
- Reduced Need for Buffers

## Applications

- Programmable Gain Amplifiers
- Analog Multiplexing
- Servo Control Systems
- Programmable Filters
- Audio Switching

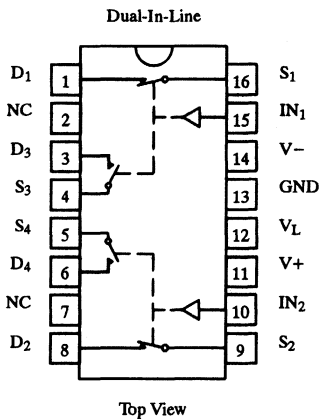
## Description

The DG243 is a monolithic dual SPDT analog switch designed for general switching applications in communication, instrumentation, and process control systems. Featuring make-before-break action, the DG243 is used in closed loop systems to switch gain or bandwidth networks without opening the loop.

The DG243 is designed on the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 44 V. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off.

## Functional Block Diagram and Pin Configuration



**Truth Table**

Logic	$SW_1, SW_2$	$SW_3, SW_4$
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.0$  V

Switches Shown for Logic "1" Input

**Ordering Information**

Temp Range	Package	Part Number
0°C to 70°C	16-Pin Plastic DIP	DG243CJ

## Absolute Maximum Ratings

V+ to V-	44 V
GND to V-	25 V
V <sub>L</sub>	(GND - 0.3 V) to 44 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous	30 mA
Current, S or D (Pulsed 1 ms 10% duty)	100 mA
Storage Temperature	-65 to 125°C

Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	450 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C

## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>L</sub> = 5 V, V <sub>IN</sub> = 2.0 V, 0.8 V <sup>c</sup>	Temp <sup>a</sup>	C Suffix 0 to 70°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	-15		15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±10 V	Room Full		30	50 75	Ω
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>D</sub> = ±14 V, V <sub>S</sub> = ∓14 V	Room Full	-1 -100	±0.3	1 100	nA
	I <sub>D(off)</sub>		Room Full	-1 -100	±0.3	1 100	
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = ±14 V	Room Full	-2 -200	±0.5	2 200	
<b>Digital Control</b>							
Input Current with V <sub>IN</sub> Low	I <sub>IL</sub>	V <sub>IN</sub> = 0.8 V	Full	-1	-0.005	1	μA
Input Current with V <sub>IN</sub> High	I <sub>IH</sub>	V <sub>IN</sub> = 2.0 V	Full	-1	-0.01	1	
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF, See Figure 2	Room		250	700	ns
Turn-Off Time	t <sub>OFF</sub>		Room		390	1200	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω	Room		60		pC
Off Isolation Reject Ratio	OIRR	R <sub>L</sub> = 75 Ω, f = 1 MHz	Room		75		dB
Crosstalk (Channel-to-Channel)	X <sub>TALK</sub>		Room		89		
Source-Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V	Room		15		pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room		17		
Channel-On Capacitance	C <sub>D</sub> + S <sub>(on)</sub>		Room		45		
<b>Power Supplies</b>							
Positive Supply Current	I <sub>+</sub>	All Channels On or Off	Room		180	300	μA
Negative Supply Current	I <sub>-</sub>		Room	-300	-150		
Logic Supply Current	I <sub>L</sub>		Room		100	300	
Ground Current	I <sub>GND</sub>		Room	-300	-140		

Notes:

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

**Schematic Diagram (Typical Channel)**

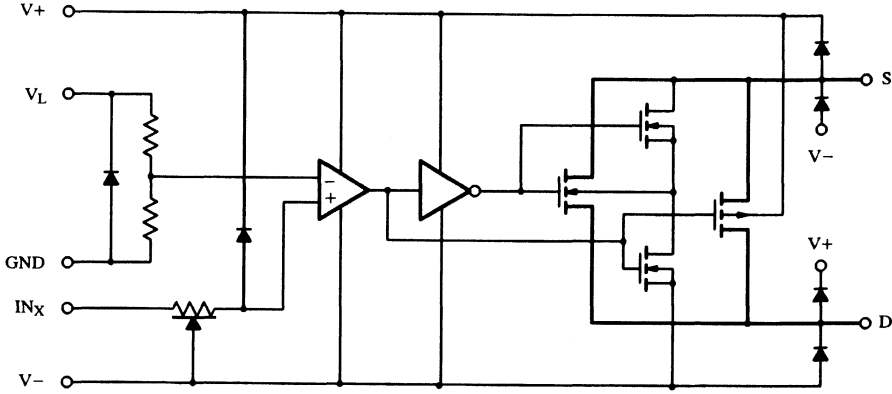
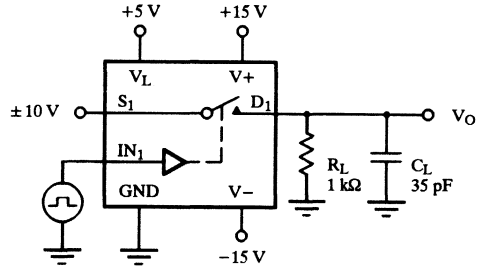
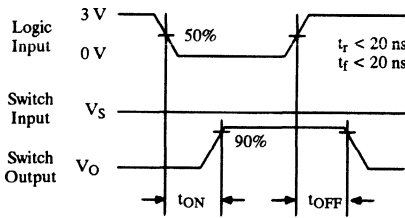


Figure 1.

**Test Circuits**

$V_O$  is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



$$C_L \text{ (includes fixture and stray capacitance)}$$

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2. Switching Time

1

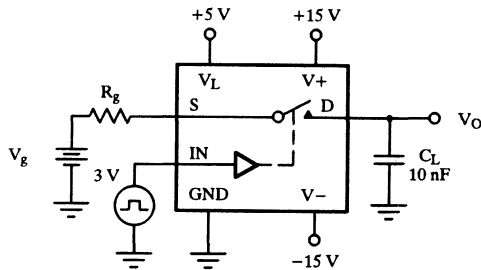


Figure 3. Charge Injection

## Applications

The make-before-break operation of the DG243 provides simple transient suppression in these two important applications.

Figure 3 shows a minimum amount of glitching during changes of gain states. The relatively low impedance of the gain setting resistors (10 k $\Omega$ , 1 k $\Omega$ , and 100  $\Omega$ ) shunt the injected charge-to-ground minimizing transient effects

occurring at the inverting input of the op amp. Consequently, these transients are not amplified to  $V_{OUT}$ .

Figure 4 takes advantage of the make-before-break operation of the DG243 by shorting transition current to real ground instead of virtual ground. The best results are obtained by selecting an op amp with the proper offset voltage specification.

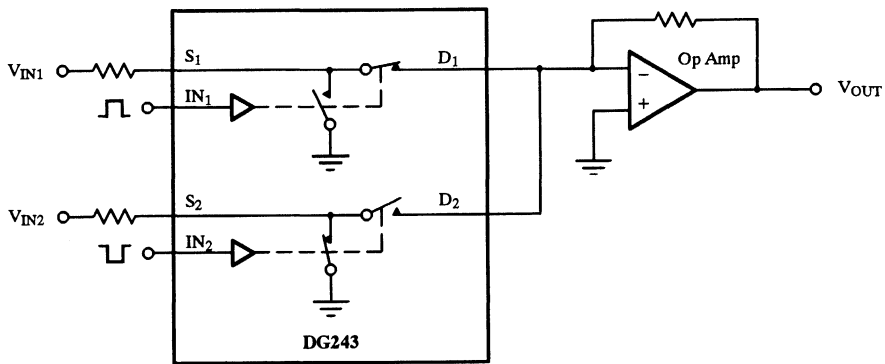


Figure 4. Minimizing Glitches in Audio Switching

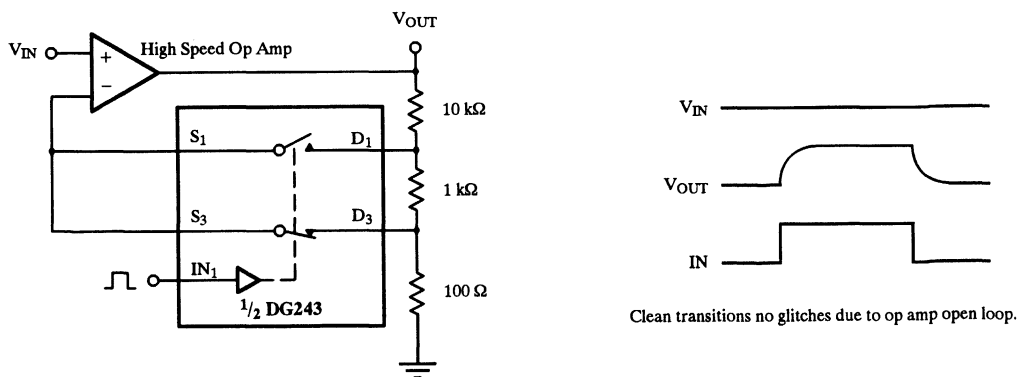


Figure 5. Make-Before-Break Improves Transient Response in Programmable Gain Amplifiers

# High-Speed Quad Monolithic SPST CMOS Analog Switch

## Features

- Fast Switching  $t_{ON}$ : 55 ns
- Low Charge Injection: 9 pC
- Low  $r_{DS(on)}$ : 32  $\Omega$
- TTL Compatible
- Low Leakage: 50 pA

## Benefits

- Fast Settling Times
- Reduced Switching Glitches
- High Precision

## Applications

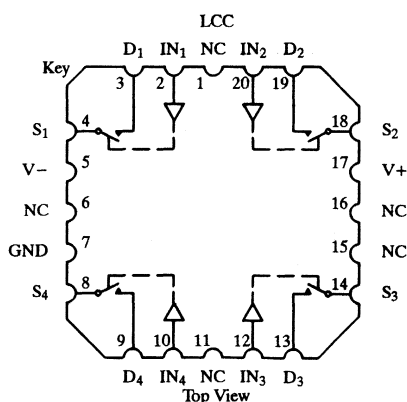
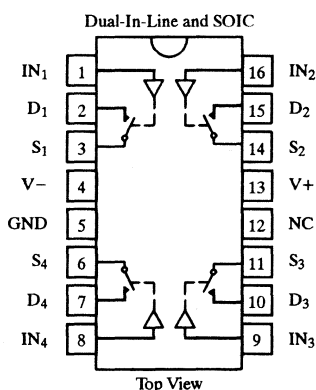
- High Speed Switching
- Sample/Holds
- Digital Filters
- Op Amp Gain Switching
- Flight Control Systems

## Description

The DG271 high speed quad single-pole single-throw analog switch is intended for applications that require low on-resistance, low leakage currents, and fast switching speeds.

Built on Siliconix' proprietary high voltage silicon gate process to achieve superior on/off performance, each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. An epitaxial layer prevents latchup.

## Functional Block Diagram and Pin Configuration



### Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG271CJ
-40 to 85°C	16-Pin Narrow SOIC	DG271DY
-55 to 125°C	16-Pin CerDIP	DG271AK
		DG271AK/883
		5962-8671602MEA
	LCC-20	DG271AZ/883
		5962-8671602M2A

### Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0"  $\leq$  0.8 V  
Logic "1"  $\geq$  2 V  
Switches Shown for Logic "1" Input

## Absolute Maximum Ratings

V+ to V-	44 V
GND to V-	25 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	100 mA
Storage Temperature (AK, AZ, DY Suffix)	-65 to 150°C
(CJ Suffix)	-65 to 125°C
Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	470 mW
16-Pin Plastic Narrow SOIC <sup>d</sup>	600 mW
16-Pin CerDIP <sup>e</sup>	900 mW
LCC-20 <sup>f</sup>	750 mW

### Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 75°C
- Derate 7.6 mW/°C above 75°C
- Derate 12 mW/°C above 75°C
- Derate 10 mW/°C above 75°C

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified  V+ = 15 V, V- = -15 V V <sub>IN</sub> = 2 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		C, D Suffix 0 to 70°C -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±10 V	Room Full	32		50 75		50 75	Ω
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>D</sub> = ±14 V, V <sub>S</sub> = ∓14 V	Room Full	±0.05	-1 -100	1 100	-1 -100	1 100	nA
	I <sub>D(off)</sub>		Room Full	±0.05	-1 -100	1 100	-1 -100	1 100	
Channel On Leakage Current	I <sub>D(on)</sub> + I <sub>S(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = ±14 V	Room Full	±0.05	-1 -200	1 200	-1 -200	1 200	
<b>Digital Control</b>									
Input Current with Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2 V	Room Full	0.010	-1 -10		-1 -10		μA
		V <sub>IN</sub> = 15 V	Room Full	0.010		1 10		1 10	
Input Current with Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Room Full	0.010	-1 -10		-1 -10		
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	V <sub>S</sub> = ±10 V See Figure 2	Room Full	55		65 80		65 80	ns
Turn-Off Time	t <sub>OFF</sub>		Room Full	50		65 80		65 80	
Charge Injection	Q	C <sub>L</sub> = 100 pF, V <sub>gen</sub> = 0 V R <sub>gen</sub> = 0 Ω	Room	9					pC

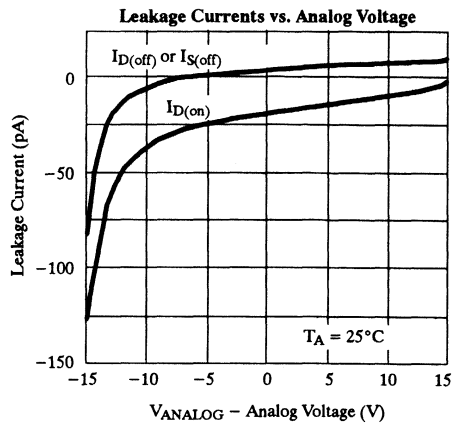
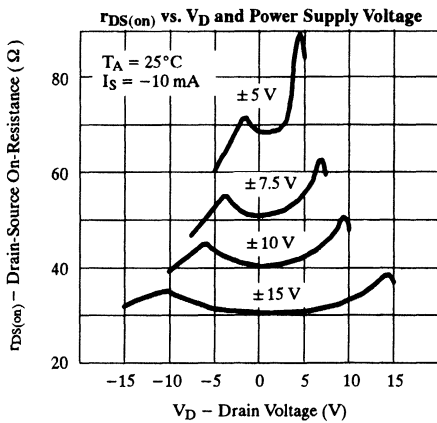
**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 2\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		C, D Suffix 0 to 70°C -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Dynamic Characteristics (Cont'd)</b>									
Source Off Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}, V_{IN} = 5\text{ V}$ $f = 1\text{ MHz}$	Room	6					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$	$V_D = V_S = 0\text{ V}, V_{IN} = 0\text{ V}$	Room	24					
Off Isolation	OIRR	$R_L = 50\ \Omega, f = 1\text{ MHz}$	Room	75					dB
Crosstalk	XTALK		Room	95					
<b>Supply</b>									
Positive Supply Current	I+	All Channels On or Off	Room Full	4.3		7.5 11		7.5 11	mA
Negative Supply Current	I-		Room Full	-3.4	-6 -10		-6 -10		

**Notes:**

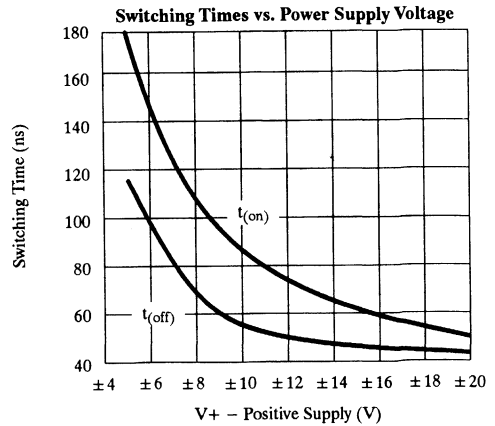
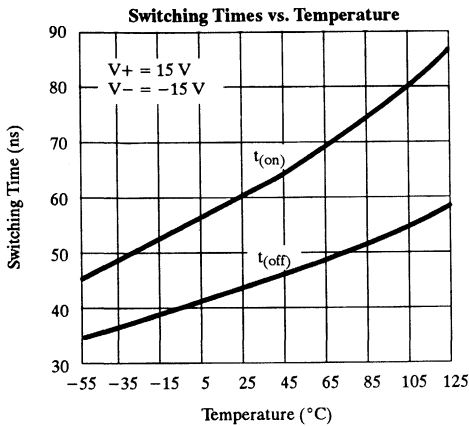
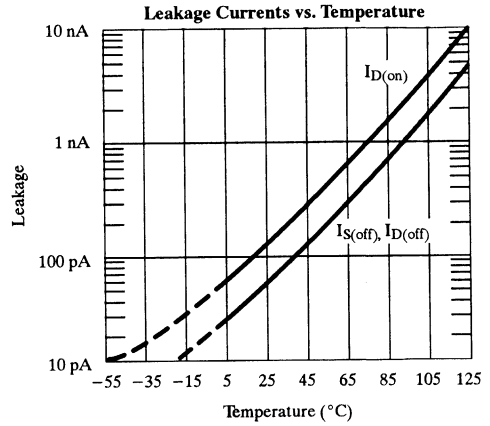
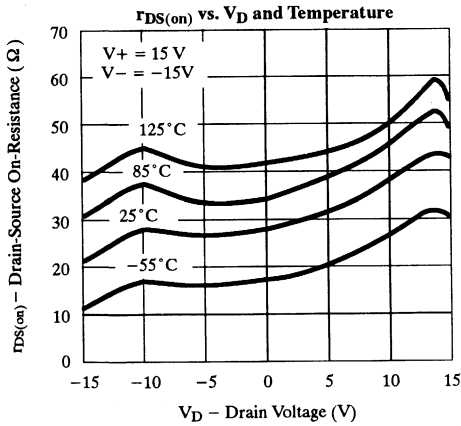
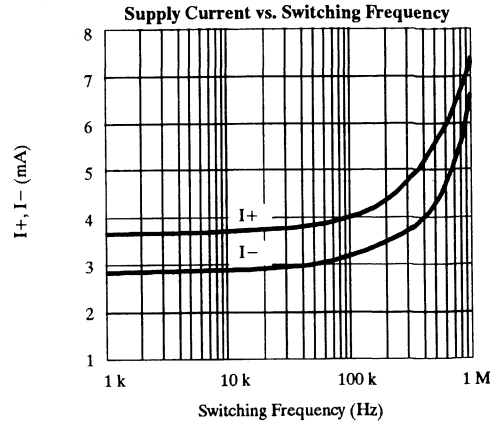
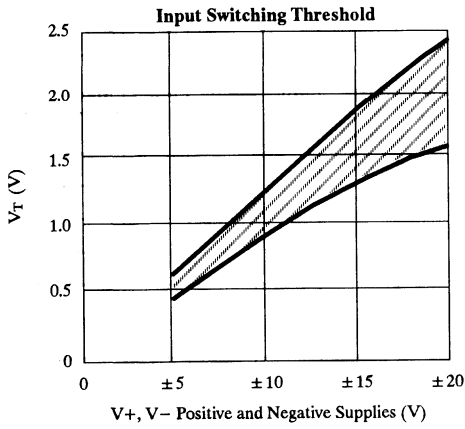
- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**



**1**

## Typical Characteristics (Cont'd)





**Schematic Diagram (Typical Channel)**

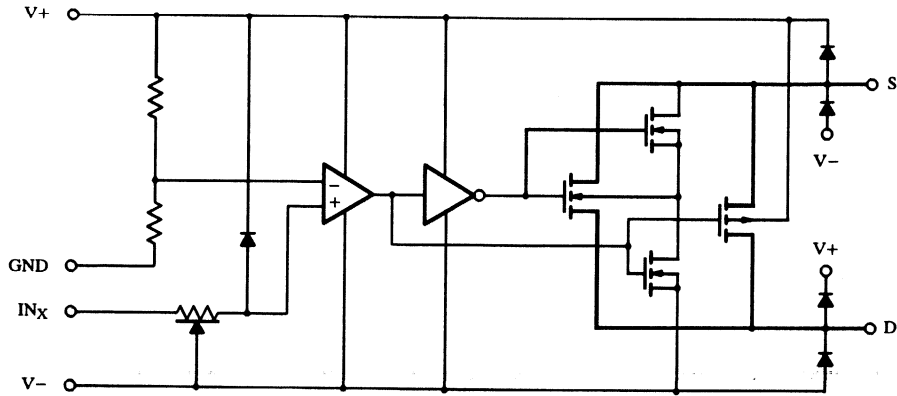


Figure 1.

**Test Circuits**

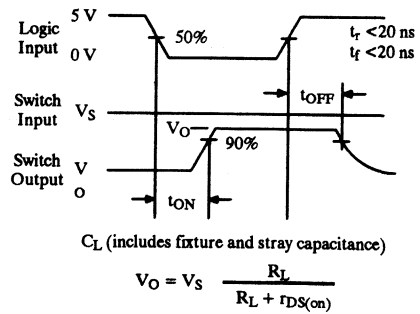
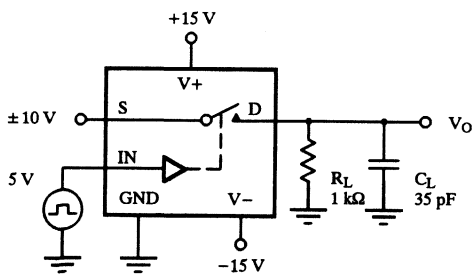


Figure 2. Switching Time

**1**

## CMOS Analog Switches

### Features

- Analog Signal Range:  $\pm 15\text{ V}$
- Fast Switching— $t_{ON}$ : 150 ns
- Low On-Resistance— $r_{DS(on)}$ : 30  $\Omega$
- Single Supply Operation
- Latch-up Proof
- CMOS Compatible

### Benefits

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Low Power Dissipation

### Applications

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

### Description

The DG300A-DG303A family of monolithic CMOS switches feature three switch configuration options (SPST, SPDT, and DPST) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power consumption are required.

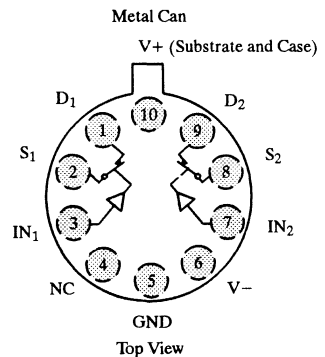
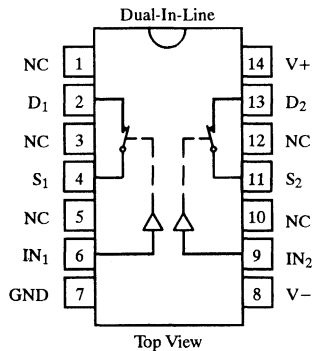
Designed on the Siliconix PLUS-40 CMOS process, these switches are latch-up proof, and are designed to block up to 30 V peak-to-peak when off. An epitaxial layer prevents latchup.

In the on condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their low on-resistance.

Featuring low power consumption (3.5 mW typ) these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, these devices are CMOS and quasi TTL compatible. Single supply operation is allowed by connecting the V- rail to 0 V.

### Functional Block Diagram and Pin Configuration

DG300A



Ordering Information – DG300A

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG300ACJ
	14-Pin CerDIP	DG300ABK
-25 to 85°C	10-Pin Metal Can	DG300ABA
		DG300AAK
-55 to 125°C	14-Pin CerDIP	DG300AAK/883
		JM38510/11601BCA
		JM38510/11601BCC
	14-Pin Sidebrazed	DG300AAA/883
	10-Pin Metal Can	JM38510/11601BIA

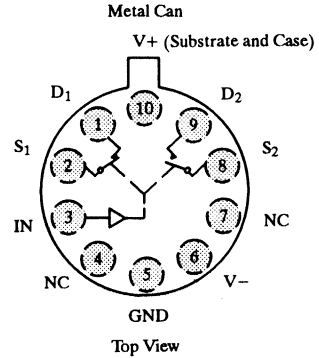
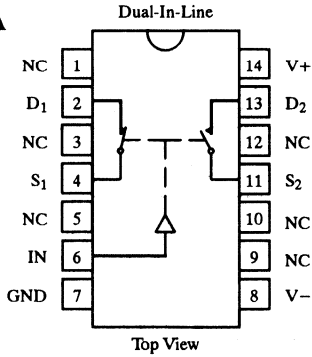
Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq 0.8\text{ V}$   
Logic "1"  $\geq 4\text{ V}$   
Switches Shown for Logic "1" Input

## Functional Block Diagram and Pin Configuration (Cont'd)

### DG301A



### Ordering Information – DG301A

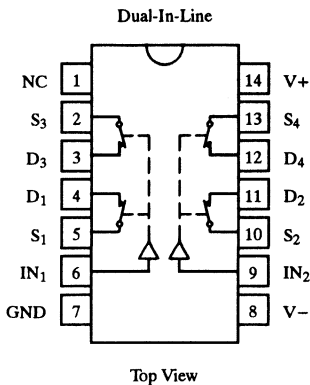
Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG301ACJ
-25 to 85°C	14-Pin CerDIP	DG301ABK
	10-Pin Metal Can	DG301ABA
-55 to 125°C	14-Pin CerDIP	DG301AAK
		DG301AAK/883
		JM38510/11602BCA
	14-Pin Sidebrazed	JM38510/11602BCC
	10-Pin Metal Can	DG301AAA
		DG301AAA/883
JM38510/11602BIA		

### Truth Table

Logic	SW <sub>1</sub>	SW <sub>2</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 4 V  
Switches Shown for Logic "1" Input

### DG302A



### Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 4 V  
Switches Shown for Logic "1" Input

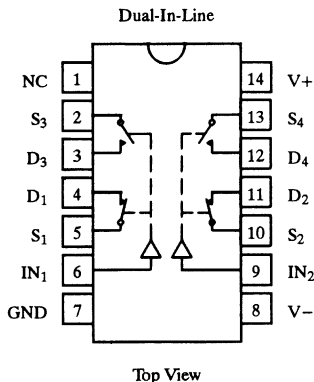
### Ordering Information – DG302A

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG302ACJ
-55 to 125°C	14-Pin CerDIP	DG302AAK
		DG302AAK/883
		JM38510/11603BCA
	14-Pin Sidebrazed	JM38510/11603BCC

# DG300A/301A/302A/303A

## Functional Block Diagram and Pin Configuration (Cont'd)

### DG303A



### Truth Table

Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 4 V

Switches Shown for Logic "1" Input

### Ordering Information – DG303A

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG303ACJ
-25 to 85°C	14-Pin CerDIP	DG303ABK
		DG303AAK
		DG303AAK/883
		JM38510/11604BCA
-55 to 125°C	14-Pin Sidebraz	JM38510/11604BCC

## Absolute Maximum Ratings

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs<sup>a</sup>, V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2V or  
30 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA  
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A & B Suffix) ..... -65 to 150°C  
(C Suffix) ..... -65 to 125°C

Power Dissipation<sup>b</sup>

14-Pin Plastic DIP<sup>c</sup> ..... 470 mW

14-Pin CerDIP<sup>d</sup> ..... 825 mW

10-Pin Metal Can<sup>e</sup> ..... 450 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C
- Derate 11 mW/°C above 75°C
- Derate 6 mW/°C above 75°C

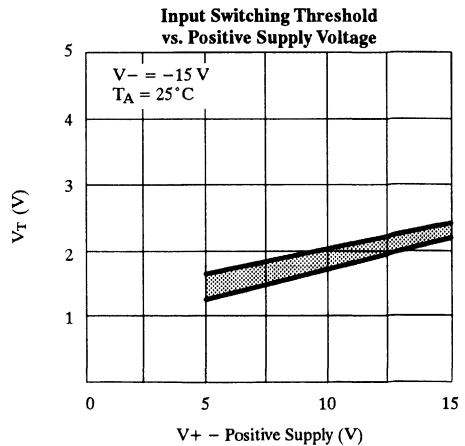
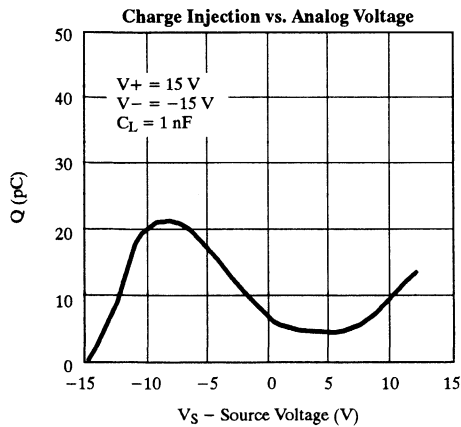
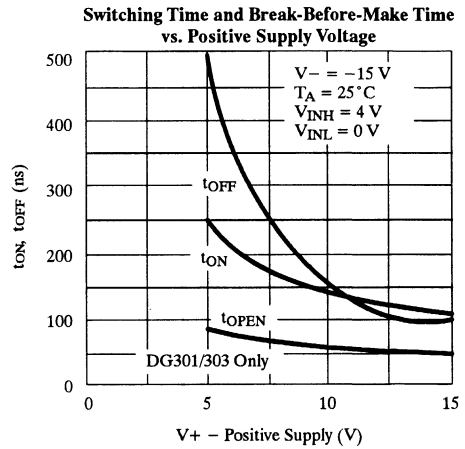
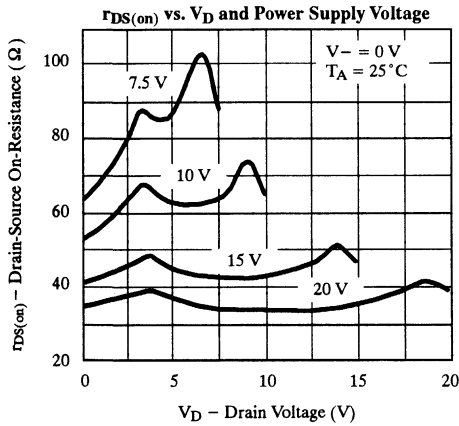
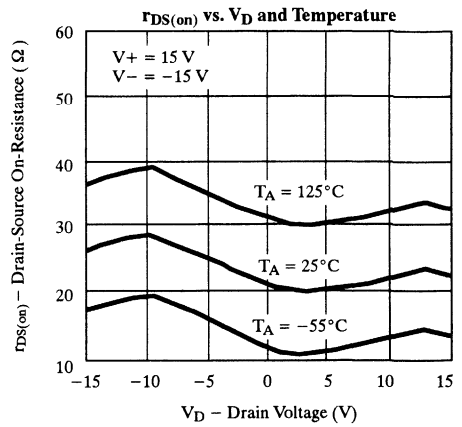
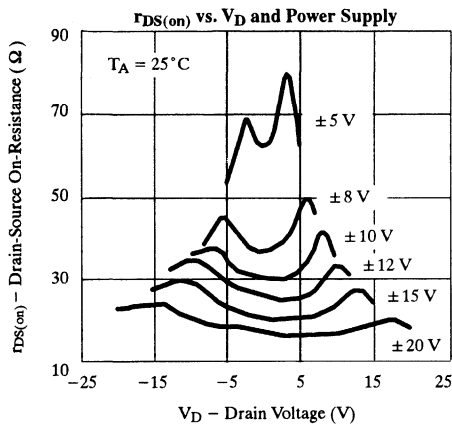
## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 0.8\text{ V}$ or $V_{IN} = 4\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C Suffix		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-15	15	-15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}, I_S = -10\text{ mA}$	Room Full	30		50 75		50 75	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}, V_D = \mp 14\text{ V}$	Room Hot	$\pm 0.1$	-1 -100	1 100	-5 -100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$		Room Hot	$\pm 0.1$	-1 -100	1 100	-5 -100	5 100	
Drain On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 14\text{ V}$	Room Hot	$\pm 0.1$	-1 -100	1 100	-5 -100	5 100	
<b>Digital Control</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Full	-0.001	-1 -1		-1		$\mu\text{A}$
		$V_{IN} = 15\text{ V}$	Room Full	0.001		1 1		1	
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Room Full	-0.001	-1 -1		-1		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	See Figure 2	Room	150		300			ns
Turn-Off Time	$t_{OFF}$		Room	130		250			
Break-Before-Make Time	$t_{OPEN}$	DG301A/303A Only See Figure 3	Room	50					
Charge Injection	Q	$C_L = 1\text{ nF}, R_{gen} = 0\ \Omega, V_{gen} = 0\text{ V}$ See Figure 4	Room	8					pC
Source-Off Capacitance	$C_{S(off)}$	$V_S, V_D = 0\text{ V}, f = 1\text{ MHz}$	Room	14					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	14					
Channel-On Capacitance	$C_{D(on)}$		Room	40					
Input Capacitance	$C_{in}$	$f = 1\text{ MHz}$	$V_{IN} = 0\text{ V}$	Room	6				
			$V_{IN} = 15\text{ V}$	Room	7				
Off-Isolation	OIRR	$V_{IN} = 0\text{ V}, R_L = 1\text{ k}\Omega$	Room	62					dB
Crosstalk (Channel-to-Channel)	XTALK	$V_S = 1\text{ V}_{rms}, f = 500\text{ kHz}$	Room	74					
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 4\text{ V}$ (One Input) All Others = 0 V	Room Full	0.23		0.5 1		1	mA
Negative Supply Current	$I_-$		Room Full	-0.001	-10 -100		-100		
Positive Supply Current	$I_+$	$V_{IN} = 0.8\text{ V}$ (All Inputs)	Room Full	0.001		10 100		100	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Full	-0.001	-10 -100		-100		

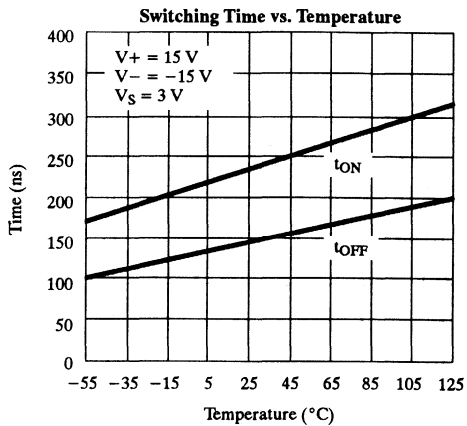
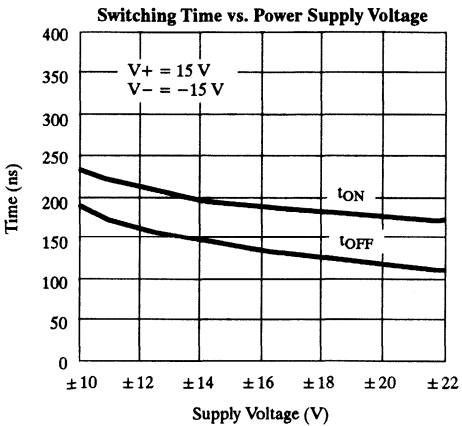
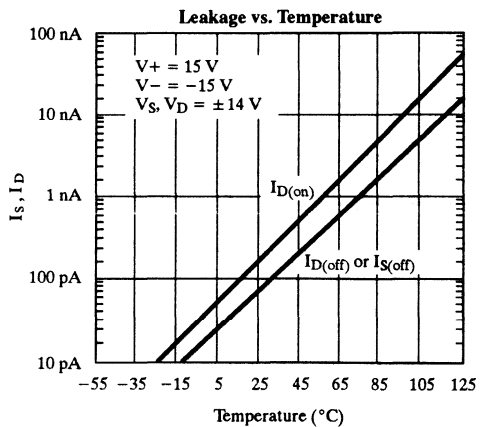
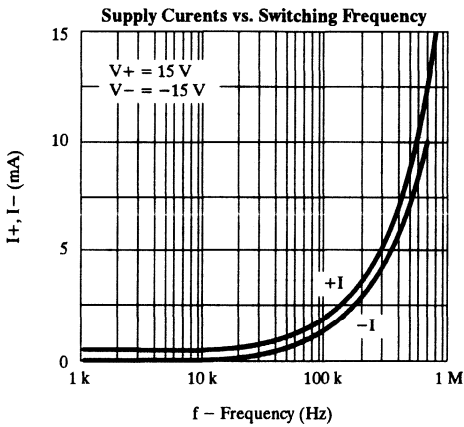
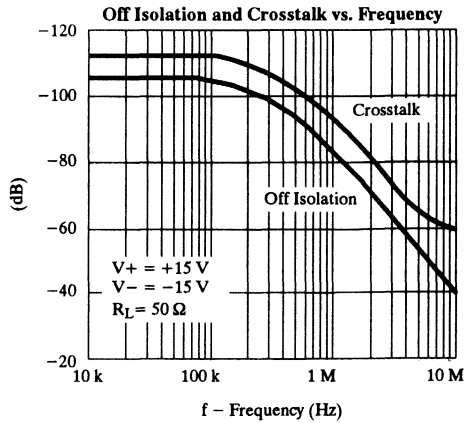
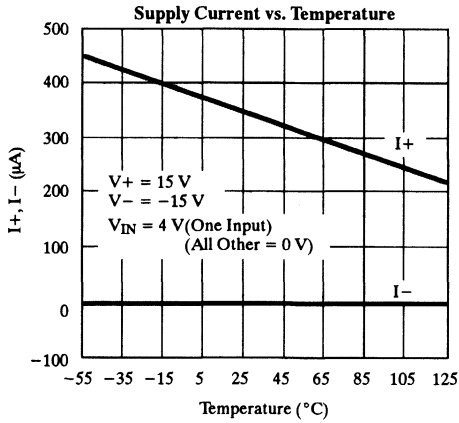
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

## Typical Characteristics



**Typical Characteristics (Cont'd)**



## Schematic Diagram (Typical Channel)

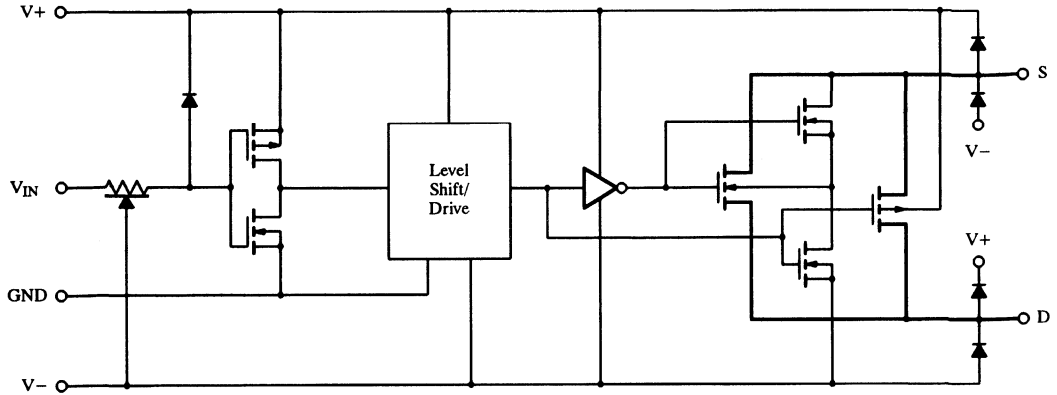
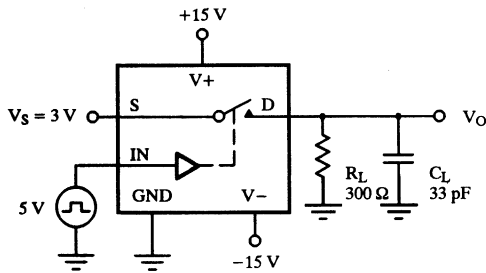


Figure 1.

## Test Circuits



$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

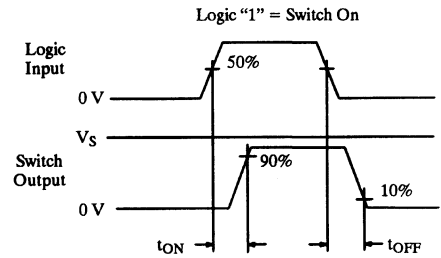
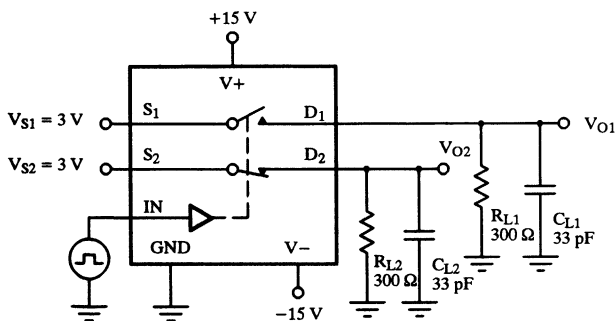


Figure 2. Switching Time



$C_L$  (includes fixture and stray capacitance)

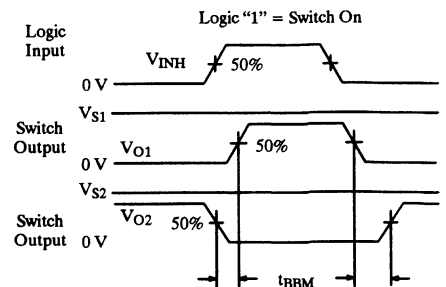


Figure 3. Break-Before-Make SPDT (DG301A, DG303A)



## Test Circuits (Cont'd)

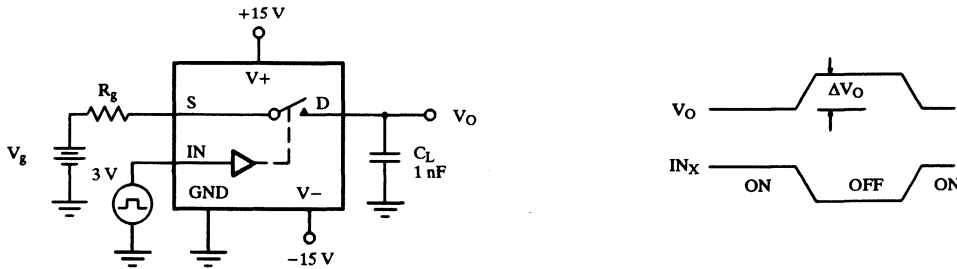


Figure 4. Charge Injection

## Application Hints<sup>a</sup>

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>g</sub> or V <sub>D</sub> Analog Voltage Range (V)
15	-15	0	4/0.8	-15 to 15
20	-20	0	4/0.8	-20 to 20
15	0	0	4/0.8	0 to 15

Note:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

1

## Applications

The DG300A series of analog switches will switch positive analog signals while using a single positive supply. This facilitates their use in applications where only one supply is available. The trade-offs of using single supplies are:

1) Increased  $r_{DS(on)}$ ; 2) slower switching speed. The analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 V. (See Input Switching Threshold vs. Positive Supply Voltage Curve.)

## Applications (Cont'd)

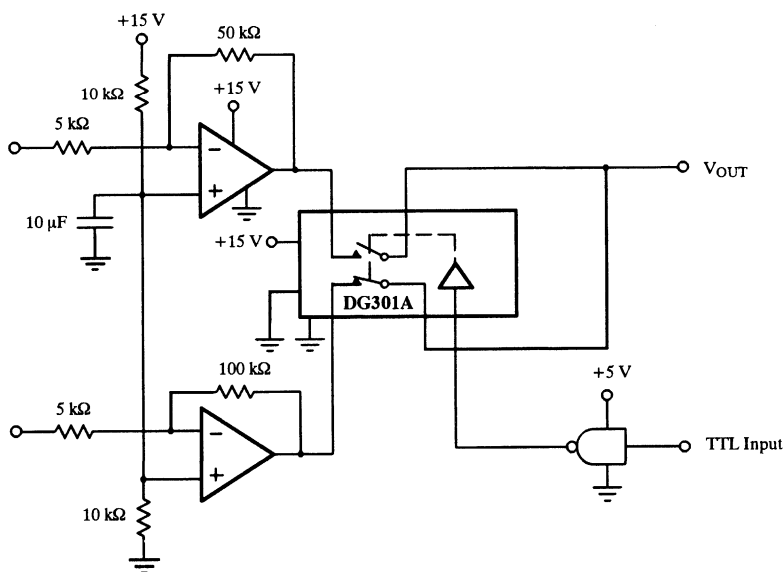


Figure 5. Single Supply Op Amp Switching

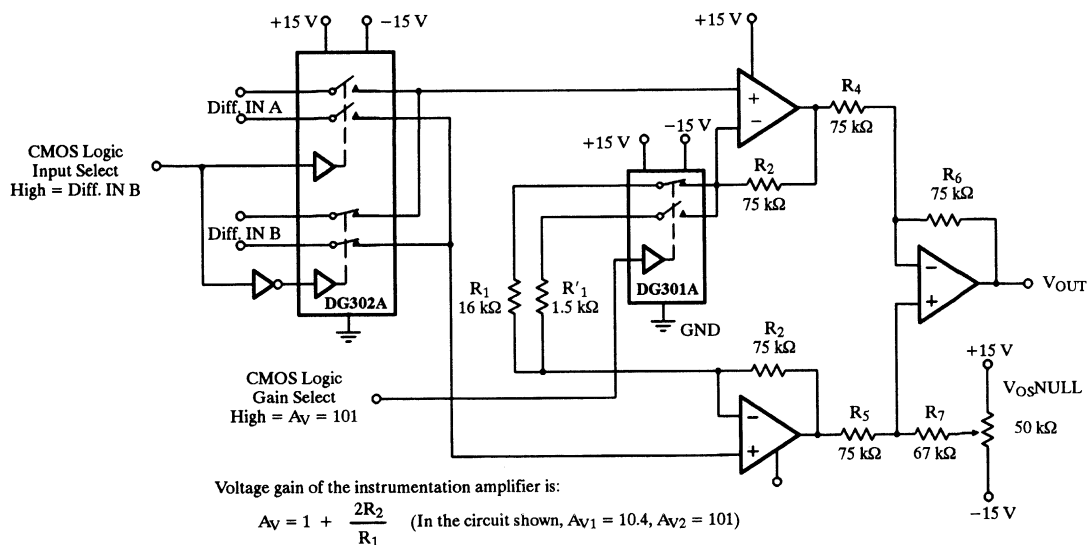


Figure 6. Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain

## CMOS Analog Switches

### Features

- $\pm 15\text{-V}$  Input Range
- Fast Switching— $t_{ON}$ : 110 ns
- Low  $r_{DS(on)}$ :  $30\ \Omega$
- Single Supply Operation
- CMOS Logic Levels
- Micropower: 30 nW

### Benefits

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Wide Dynamic Range
- Low Power Dissipation

### Applications

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

### Description

The DG304A through DG307A series of monolithic CMOS switches were designed for applications in communications, instrumentation and process control. This series is well suited for applications requiring fast switching and nearly flat on-resistance over the entire analog range.

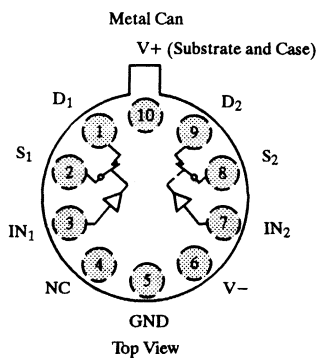
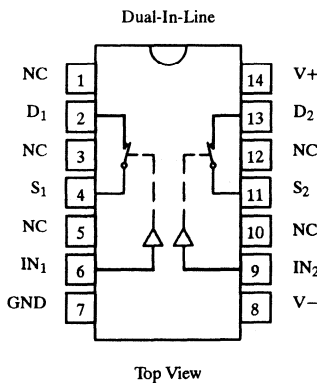
applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation (for positive switch voltages) is allowed by connecting the  $V^-$  rail to 0 V.

Designed on the Siliconix PLUS-40 CMOS process to achieve low power consumption and excellent on/off switch performance, these switches are ideal for battery powered

Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS input compatible.

### Functional Block Diagram and Pin Configuration

#### DG304A



#### Ordering Information – DG304A

Temp Range	Package	Part Number
-0 to 70°C	14-Pin Plastic DIP	DG304ACJ
		DG304AAK/883
-55 to 125°C	14-Pin CerDIP	JM38510/11605BCA
	10-Pin Can	JM38510/11605BIA
	14-Pin Sidebraz	JM38510/11605BCC

#### Truth Table

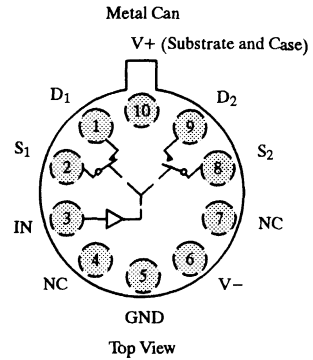
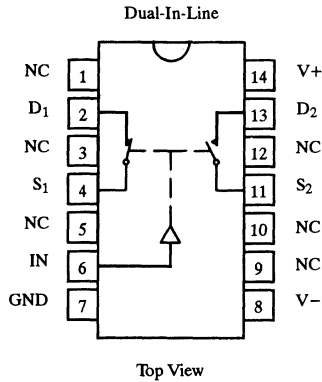
Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq 3.5\text{ V}$   
Logic "1"  $\geq 11\text{ V}$   
Switches Shown for Logic "1" Input

# DG304A/305A/306A/307A

## Functional Block Diagram and Pin Configuration (Cont'd)

### DG305A



#### Ordering Information – DG305A

Temp Range	Package	Part Number
-55 to 125°C	14-Pin CerDIP	JM38510/11605BCA
	10-Pin Can	DG305AAA
		JM38510/11606BIC
	14-Pin Sidebraze	JM38510/11606BCA

#### Truth Table

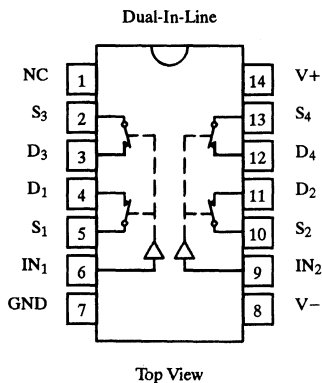
Logic	SW <sub>1</sub>	SW <sub>2</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V

Logic "1" ≥ 11 V

Switches Shown for Logic "1" Input

### DG306A



#### Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 3.5 V

Logic "1" ≥ 11 V

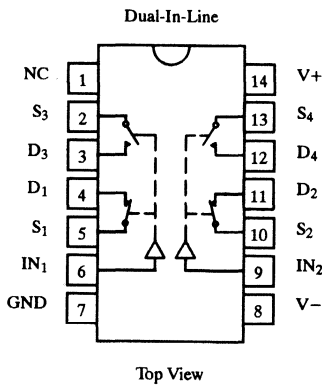
Switches Shown for Logic "1" Input

#### Ordering Information – 306A

Temp Range	Package	Part Number
-0 to 70°C	14-Pin Plastic DIP	DG306ACJ
		DG306AAK/883
-55 to 125°C	14-Pin CerDIP	JM38510/11607BCA
	14-Pin Sidebraze	JM38510/11607BCC

## Functional Block Diagram and Pin Configuration (Cont'd)

### DG307A



Four SPST Switches per Package

**Truth Table**

Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V  
Logic "1" ≥ 11 V

Switches Shown for Logic "1" Input

**Ordering Information – 307A**

Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG307ACJ
-25 to 85°C	14-Pin CerDIP	DG307ABK
		DG307AAK
		DG307AAK/883
		JM38510/11608BCA
-55 to 125°C	14-Pin Sidebraz	JM38510/11608BCC

## Absolute Maximum Ratings

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs<sup>a</sup>, V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2V or 30 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA  
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (AAA, AAK, ABK Suffix) ..... -65 to 150°C  
(ACJ Suffix) ..... -65 to 125°C

Power Dissipation<sup>b</sup>

14-Pin Plastic DIP<sup>c</sup> ..... 470 mW

14-Pin CerDIP<sup>d</sup> ..... 825 mW

10-Pin Metal Can<sup>e</sup> ..... 450 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 11 mW/°C above 75°C
- Derate 6.5 mW/°C above 25°C
- Derate 6 mW/°C above 75°C

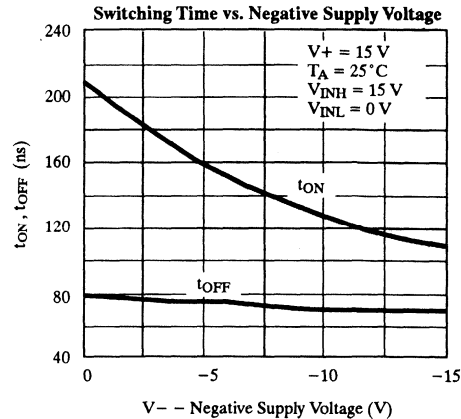
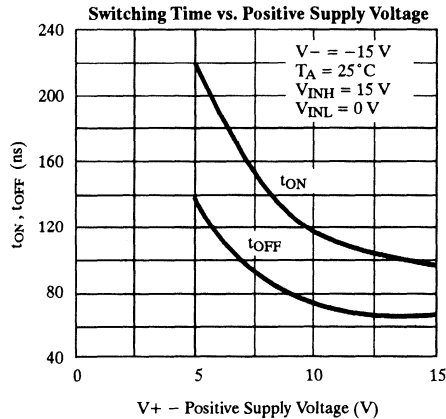
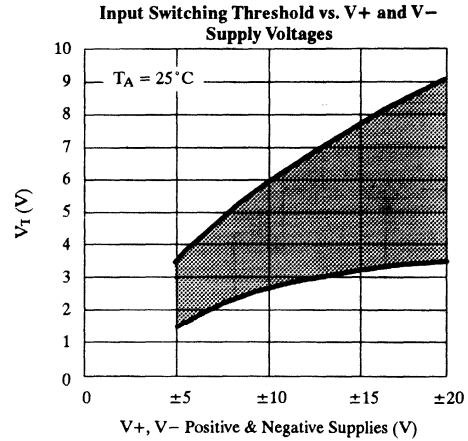
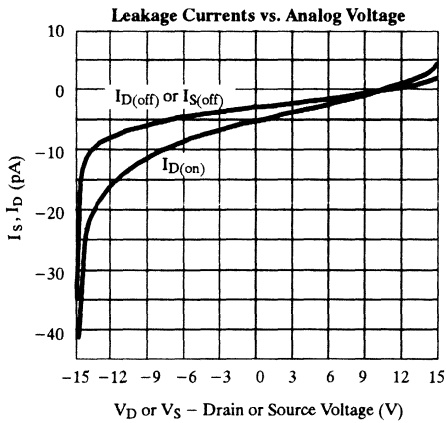
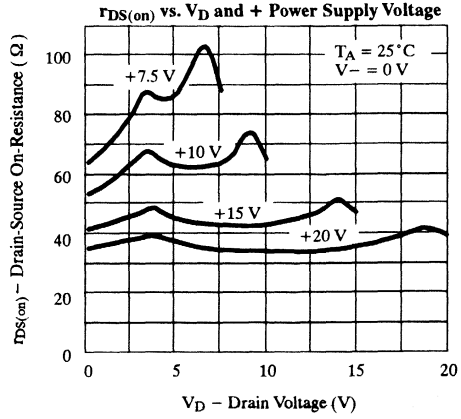
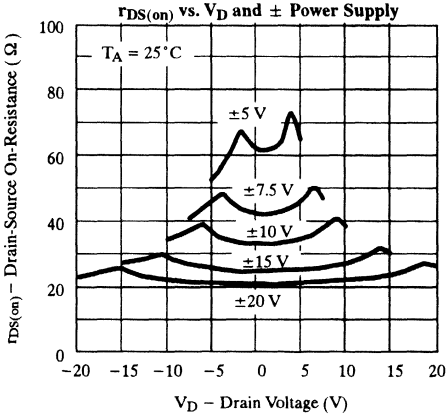
## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 3.5\text{ V or } 11\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C Suffix -25 to 85°C 0 to 70°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-15	15	-15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}, I_S = 10\text{ mA}$	Room Full	30		50 75		50 75	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}, V_D = \mp 14\text{ V}$	Room Full	$\pm 0.1$	-1 -100	1 100	-5 -100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_S = \pm 14\text{ V}, V_D = \mp 14\text{ V}$	Room Full	$\pm 0.1$	-1 -100	1 100	-5 -100	5 100	
Drain On Leakage Current	$I_{D(on)}$	$V_D = V_S = \pm 14\text{ V}$	Room Full	$\pm 0.1$	-2 -200	2 200	-5 -200	5 200	
<b>Digital Control</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Full	-0.001	-1 -1		-1		$\mu\text{A}$
		$V_{IN} = 15\text{ V}$	Room Full	0.001		1 1		1	
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Room Full	-0.001	-1 -1		-1		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	See Figure 2	Room	110		250			ns
Turn-Off Time	$t_{OFF}$		Room	70		150			
Break-Before-Make Time	$t_{OPEN}$	DG305A/307A ONLY See Figure 3	Room	50					
Charge Injection	Q	$C_L = 1\text{ nF}, R_{gen} = 0$ $V_{gen} = 0\text{ V}, \text{ See Figure 4}$	Room	30					pC
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}, V_S = 0\text{ V}$ $V_S, V_D = 0\text{ V}$	Room	14					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	14					
Channel-On Capacitance	$C_{D(on)}$		Room	40					
Input Capacitance	$C_{IN}$	$f = 1\text{ MHz}$	$V_{IN} = 0\text{ V}$	Room	6				
			$V_{IN} = 15\text{ V}$	Room	7				
Off-Isolation	OIRR	$V_{IN} = 0\text{ V}, R_L = 1\text{ k}\Omega$	Room	62					dB
Crosstalk (Channel-to-Channel)	X <sub>TALK</sub>	$V_S = 1\text{ V}_{rms}, f = 500\text{ kHz}$	Room	74					
<b>Power Supplies</b>									
Positive Supply Current	I <sup>+</sup>	$V_{IN} = 15\text{ V or } 0\text{ V (All Inputs)}$	Room Full	0.001		10 100		100	$\mu\text{A}$
Negative Supply Current	I <sup>-</sup>		Room Full	-0.001	-10 -100		-100		

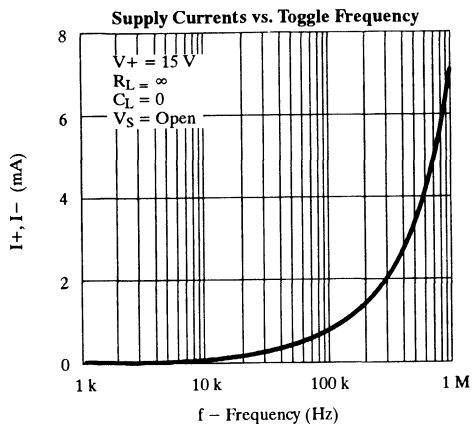
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**



## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

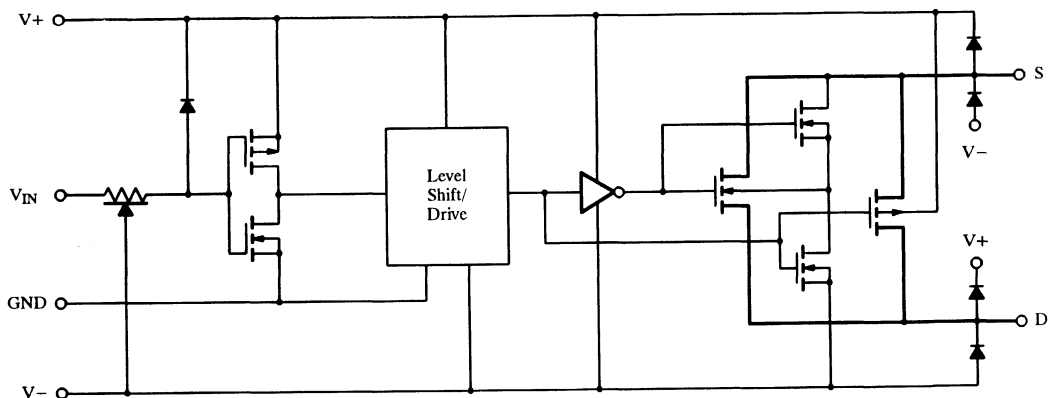


Figure 1.

## Test Circuits

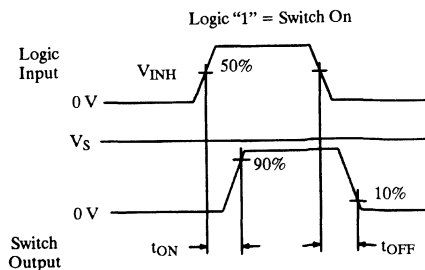
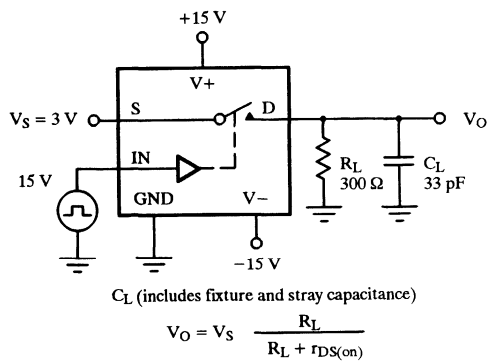
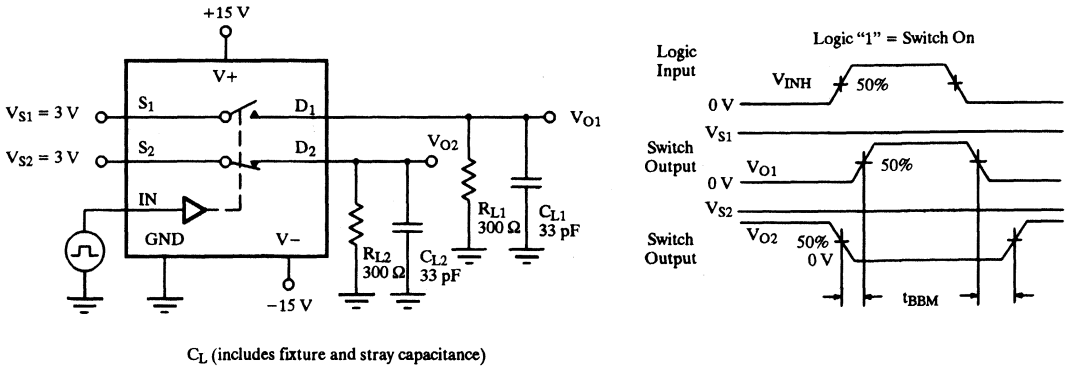


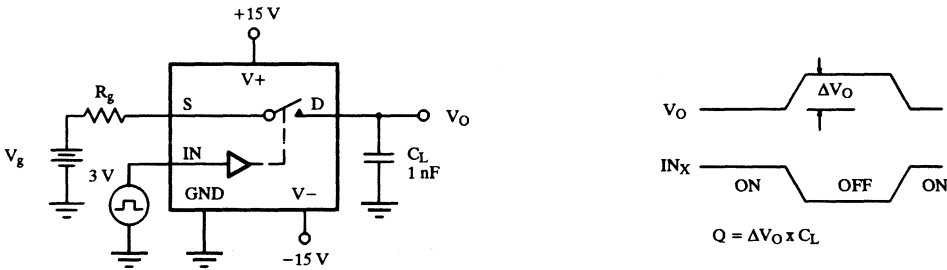
Figure 2. Switching Time



**Test Circuits (Cont'd)**



**Figure 3.** Break-Before-Make SPDT (DG305A, DG307A)



**Figure 4.** Charge Injection

**Application Hints<sup>a</sup>**

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15	-15	0	11/3.5	-15 to 15
20	-20	0	11/3.5	-20 to 20
15	0	0	11/3.5	0 to 15

Notes:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

## Applications

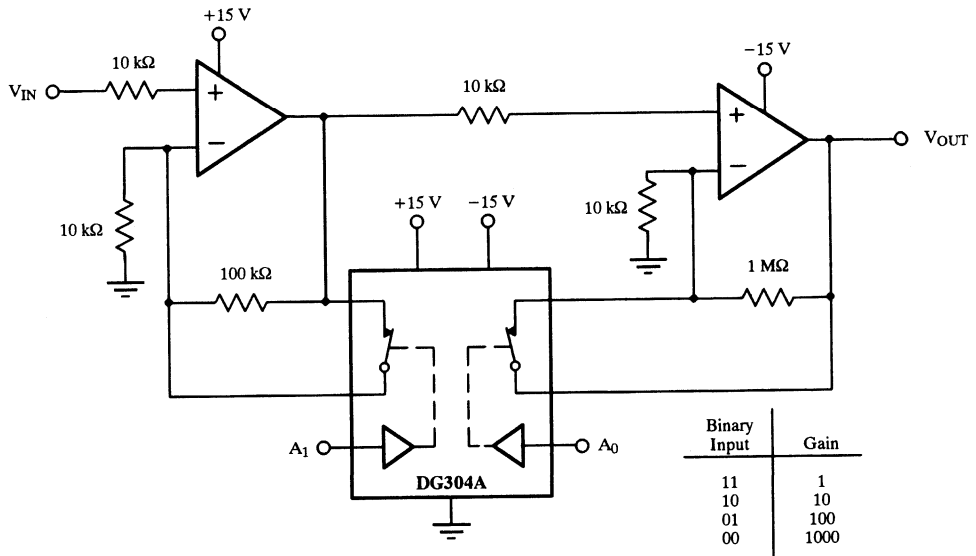


Figure 5. Low Power Binary to 10<sup>0</sup> Gain Low Frequency Amplifier

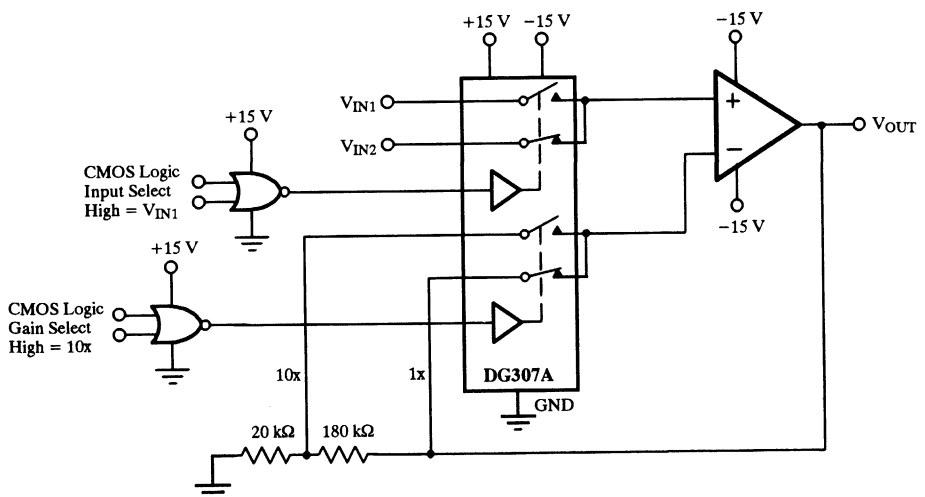


Figure 6. Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain

## Quad Monolithic SPST CMOS Analog Switches

### Features

- $\pm 15\text{-V}$  Analog Input Range
- Low On-Resistance:  $60\ \Omega$
- Fast Switching: 130 ns
- Low Power Dissipation: 30 nW
- CMOS Logic Compatible

### Benefits

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Wide Dynamic Range
- Single or Dual Supply Capability
- Static Protected Logic Inputs

### Applications

- Portable and Battery Powered Instrumentation
- Communication Systems
- Computer Peripherals
- High-Speed Multiplexing

## Description

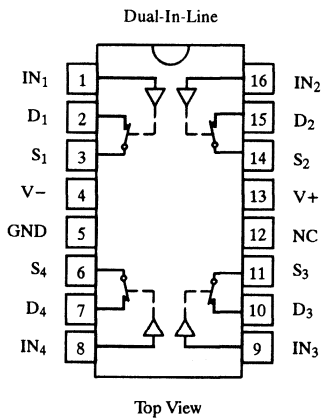
The DG308A and DG309 are quad single-pole single-throw analog switches designed for high speed switching applications in communications, instrumentation, and process control. This series is well suited for applications requiring a low on-resistance over the entire analog range.

Featuring low on-resistance ( $60\ \Omega$ ) and fast switching (130 ns), the DG308A is supplied in the “normally open”

configuration while DG309 is supplied “normally closed”. Input thresholds are high voltage CMOS compatible.

Designed with the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 44 V, each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. An epitaxial layer prevents latch up.

## Functional Block Diagram and Pin Configuration



Four SPST Switches per Package

Truth Table

Logic	DG308A	DG309
0	OFF	ON
1	ON	OFF

Logic “0”  $\leq 3.5\text{ V}$   
Logic “1”  $\geq 11\text{ V}$

Switches Shown for Logic “1” Input

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG308ACJ
		DG309CJ
-40 to 85°C	16-Pin Narrow SOIC	DG308ADY
		DG309DY
-55 to 125°C	16-Pin CerDIP	DG308AAK
		DG308AAK/883
		DG309AK/883

## Absolute Maximum Ratings

Voltages Referenced to V-	
V+	44 V
GND	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2V or 20 mA, whichever occurs first
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	20 mA
(Pulsed at 1 ms, 10% duty cycle max)	70 mA
Storage Temperature (AK Suffix)	-65 to 150°C
(CJ and DY Suffix)	-65 to 125°C

Power Dissipation <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	470 mW
16-Pin Narrow SOIC <sup>c</sup>	600 mW
16-Pin Cerdip <sup>d</sup>	900 mW

### Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 12 mW/°C above 75°C
- Derate 6.5 mW/°C above 25°C
- Derate 7.6 mW/°C above 75°C

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 3.5 V or 11 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		C, D Suffix		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = 1 mA	Room Full	60		100 150		100 125	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room Full	±0.1	-1 -100	1 100	-5 -100	5 100	nA
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = ±14 V, V <sub>S</sub> = ∓14 V	Room Full	±0.1	-1 -100	1 100	-5 -100	5 100	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = ±14 V	Room Full	±0.1	-1 -100	1 100	-5 -200	5 200	
<b>Digital Control</b>									
Input Current with Input Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 15 V	Full	0.001		1		1	μA
Input Current with Input Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Full	-0.001	-1		-1		
Input Capacitance	C <sub>IN</sub>		Room	8					pF
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	See Figure 2	Room	130		200		200	ns
Turn-Off Time	t <sub>OFF</sub>		Room	90		150		150	
Charge Injection	Q	C <sub>L</sub> = 0.01 μF, R <sub>gen</sub> = 0 Ω, V <sub>gen</sub> = 0 V	Room	-10					pC
Source-Off Capacitance	C <sub>S(off)</sub>	f = 140 kHz, V <sub>S</sub> , V <sub>D</sub> = 0 V	Room	11					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room	8					
Channel-On Capacitance	C <sub>D(on)</sub>		Room	27					
Off-Isolation <sup>f</sup>	OIRR	R <sub>L</sub> = 75 Ω, V <sub>S</sub> = 2 V <sub>p-p</sub> , f = 500 kHz	Room	78					dB

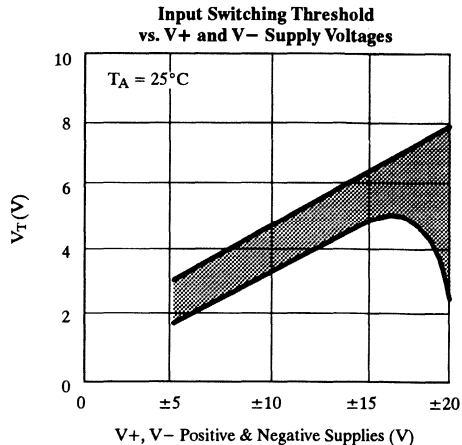
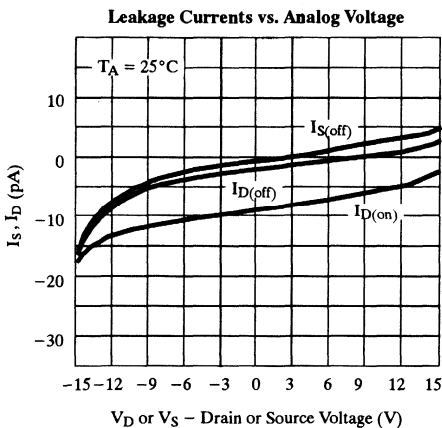
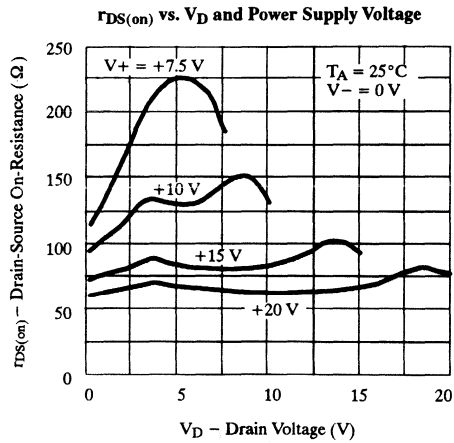
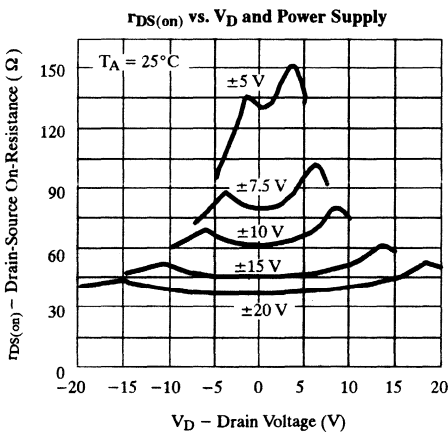
**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V+ = 15\text{ V}, V- = -15\text{ V}$ $V_{IN} = 3.5\text{ V or }11\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		C, D Suffix		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	All Channels On or Off $V_{IN} = 0\text{ V or }15\text{ V}$	Room Full	0.001		10		10	μA
Negative Supply Current	I-		Room Full	-0.001	-10		-100		

**Notes:**

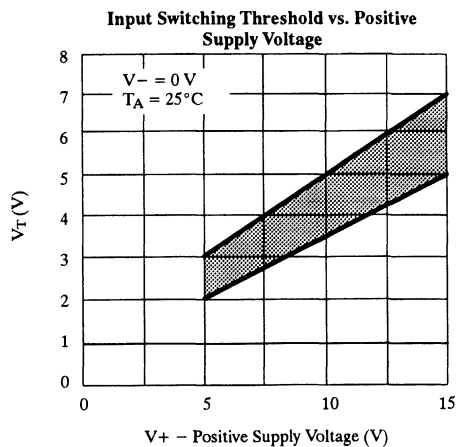
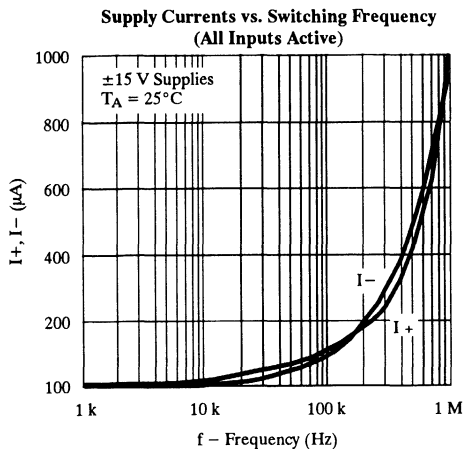
- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**



**1**

## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

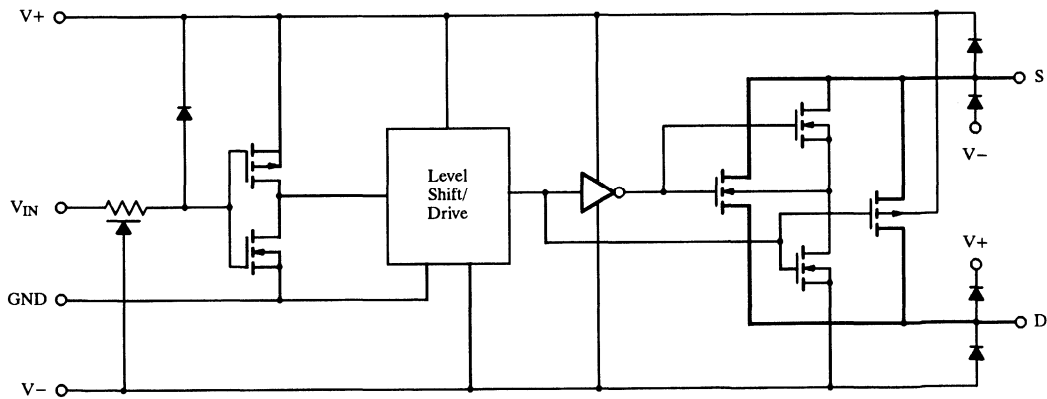
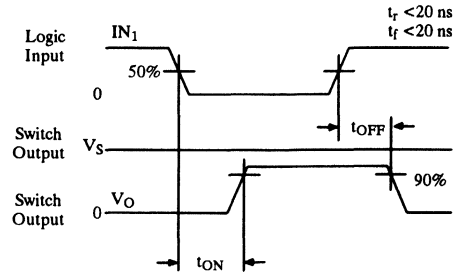
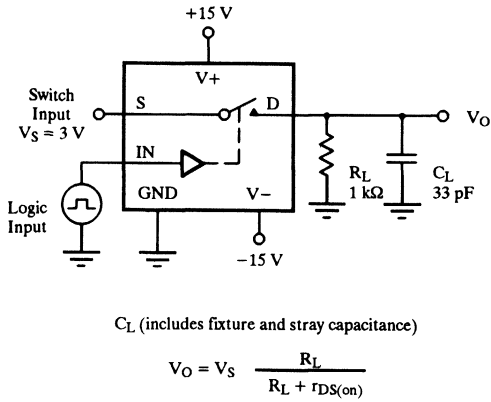


Figure 1.

**Test Circuits**



**Figure 2.** Switching Time

**Applications**

**Single Supply Operation**

The DG308A and DG309 will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) increased  $r_{DS(on)}$  and 2) slower switching

speed. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single supply operation are  $V+$  and  $0V$ .

## Improved Quad CMOS Analog Switches

### Features

- $\pm 22\text{-V}$  Supply Voltage Rating
- CMOS Compatible Logic
- Low On-Resistance— $r_{DS(on)}$ :  $45\ \Omega$
- Low Leakage— $I_{D(on)}$ :  $20\ \text{pA}$
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching— $t_{ON}$ :  $< 200\ \text{ns}$
- Low Glitching— $Q$ :  $1\ \text{pC}$

### Benefits

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG308A/309

### Applications

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

### Description

The DG308B/309B analog switches are highly improved versions of the industry-standard DG308A/309. These devices are fabricated in Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design

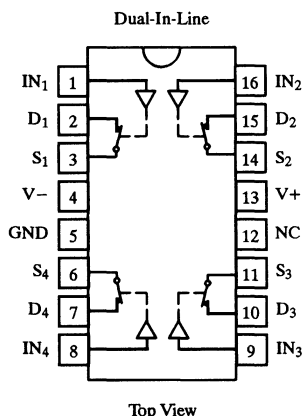
minimizes switching transients. The DG308B and DG309B can handle up to  $\pm 22\text{-V}$  input signals. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

The DG308B is a normally open switch and the DG309B is a normally closed switch. (See Truth Table.)

### Functional Block Diagram and Pin Configuration

#### DG308B



Truth Table

Logic	DG308B	DG309B
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 3.5\text{V}$   
Logic "1"  $\geq 11\text{V}$

Switches Shown for DG308B Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG308BDJ
		DG309BDJ
	16-Pin Narrow SOIC	DG308BDY
		DG309BDY
-55 to 125°C	16-Pin CerDIP	DG308BAK
		DG308BAK/883
		DG309BAK
		DG309BAK/883



**Absolute Maximum Ratings**

Voltages Referenced to V-

V+ .....	44 V
GND .....	25 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub> .....	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Current, Any Terminal .....	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max) .....	100 mA
Storage Temperature (AK, Suffix) .....	-65 to 150°C
(DJ, DY Suffix) .....	-65 to 125°C

Power Dissipation (Package)<sup>b</sup>

16-Pin Plastic DIP <sup>c</sup> .....	470 mW
16-Pin Narrow SOIC <sup>d</sup> .....	640 mW
16-Pin CerDIP <sup>e</sup> .....	900 mW

- Notes:
- Signals on S<sub>X</sub>, D<sub>X</sub>, or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads welded or soldered to PC Board.
  - Derate 6.5 mW/°C above 75°C
  - Derate 7.6 mW/°C above 75°C
  - Derate 12 mW/°C above 75°C

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 11 V, 3.5 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = 1 mA	Room	45		85		85	Ω
			Full				100		
r <sub>DS(on)</sub> Match	Δr <sub>DS(on)</sub>		Room	2					%
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room	±0.01	-0.5	0.5	-0.5	0.5	nA
			Full		-20	20	-5	5	
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = ±14 V, V <sub>S</sub> = ∓14 V	Room	±0.01	-0.5	0.5	-0.5	0.5	
			Full		-20	20	-5	5	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V	Room	±0.02	-0.5	0.5	-0.5	0.5	nA
			Full		-40	40	-10	10	
<b>Digital Control</b>									
Input Voltage High	V <sub>INH</sub>		Full		11		11		V
Input Voltage Low	V <sub>INL</sub>		Full			3.5		3.5	
Input Current	I <sub>INH</sub> or I <sub>INL</sub>	V <sub>INH</sub> or V <sub>INL</sub>	Full		-1	1	-1	1	μA
Input Capacitance	C <sub>IN</sub>		Room	5					pF
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	V <sub>S</sub> = 3 V, See Figure 2	Room			200		200	ns
Turn-Off Time	t <sub>OFF</sub>		Room			150		150	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>g</sub> = 0 V, R <sub>g</sub> = 0 Ω	Room	1					pC
Source-Off Capacitance	C <sub>S(off)</sub>	V <sub>S</sub> = 0 V, f = 1 MHz	Room	5					pF
Drain-Off Capacitance	C <sub>D(off)</sub>		Room	5					
Channel On Capacitance	C <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V, f = 1 MHz	Room	16					
Off Isolation	OIRR	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω V <sub>S</sub> = 1 V <sub>RMS</sub> , f = 100 kHz	Room	90					dB
Channel-to-Channel Crosstalk	X <sub>TALK</sub>		Room	95					

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 11\text{ V}, 3.5\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supply</b>									
Positive Supply Current	I+	$V_{IN} = 0\text{ or }15\text{ V}$	Room Full			1 5		1 5	$\mu\text{A}$
Negative Supply Current	I-		Room Full		-1 -5		-1 -5		
Power Supply Range for Continuous Operation	V <sub>OP</sub>		Full		±4	±22	±4	±22	V

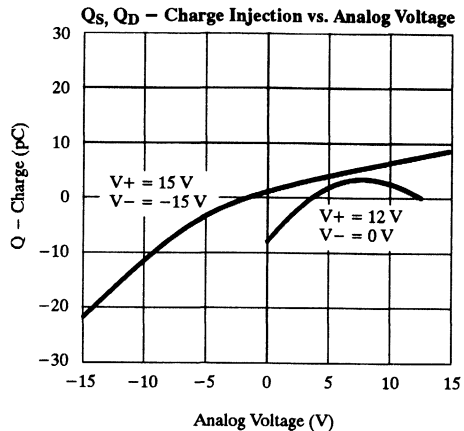
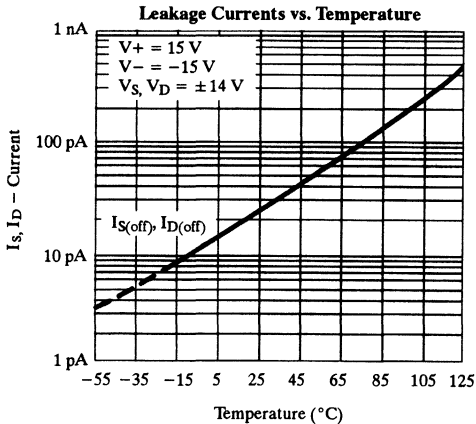
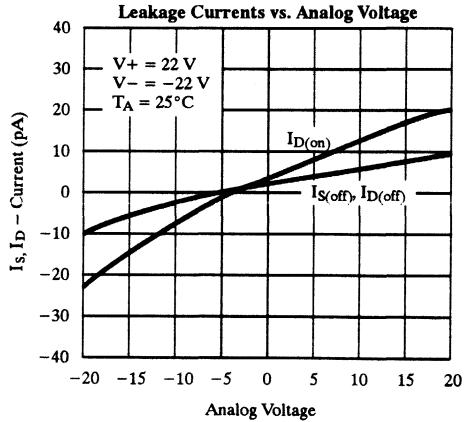
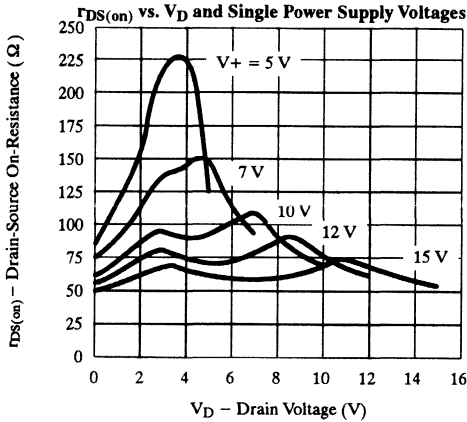
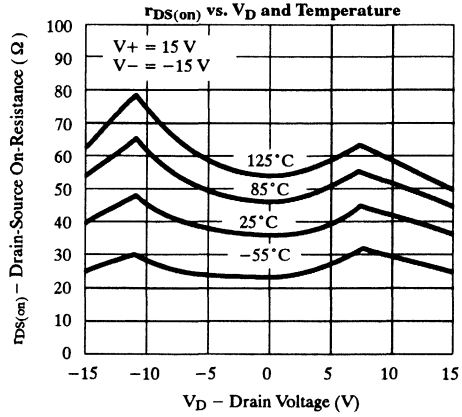
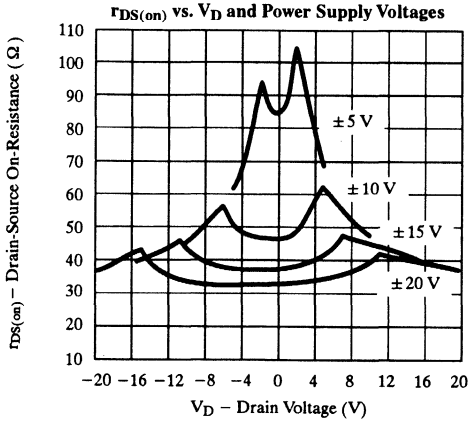
## Specifications<sup>a</sup> for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_{IN} = 11\text{ V}, 3.5\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		0	12	0	12	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	$V_D = 3\text{ V}, 8\text{ V}, I_S = 1\text{ mA}$	Room Full	90		160 200		160 200	$\Omega$
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	$V_S = 8\text{ V}, \text{ See Figure 2}$	Room			300		300	ns
Turn-Off Time	t <sub>OFF</sub>		Room			200		200	
Charge Injection	Q	$C_L = 1\text{ nF}, V_{\text{gen}} = 6\text{ V}, R_{\text{gen}} = 0\ \Omega$	Room	4					pC
<b>Power Supply</b>									
Positive Supply Current	I+	$V_{IN} = 0\text{ or }12\text{ V}$	Room Full			1 5		1 5	$\mu\text{A}$
Negative Supply Current	I-		Room Full		-1 -5		-1 -5		
Power Supply Range for Continuous Operation	V <sub>OP</sub>		Full		4	44	4	44	V

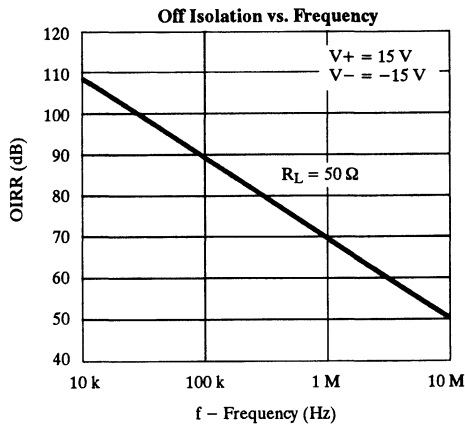
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**



## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

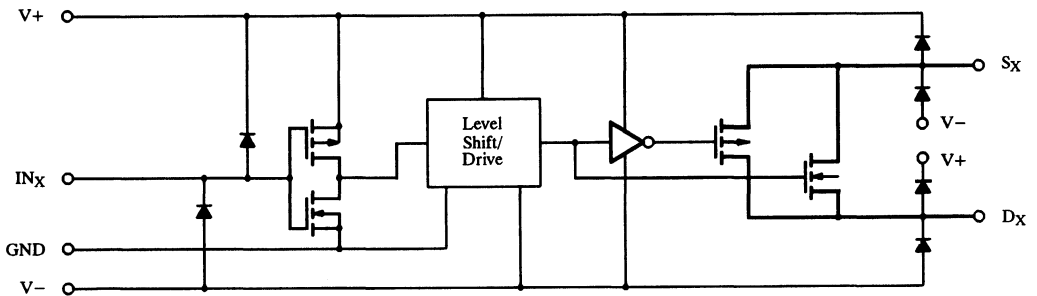


Figure 1.

## Test Circuits

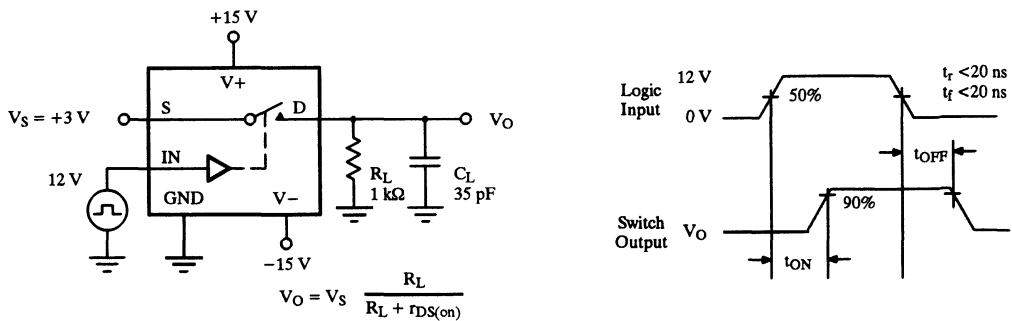
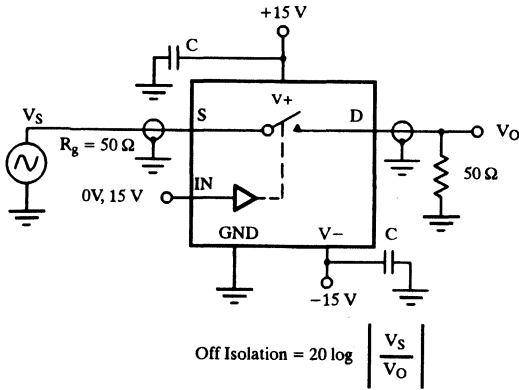
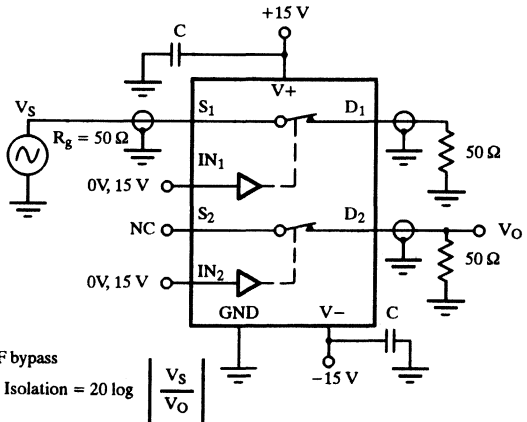


Figure 2. Switching Time

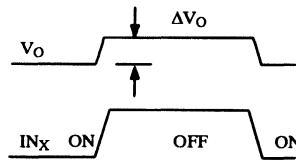
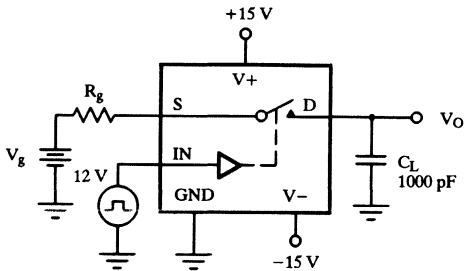
**Test Circuits (Cont'd)**



**Figure 3.** Off Isolation



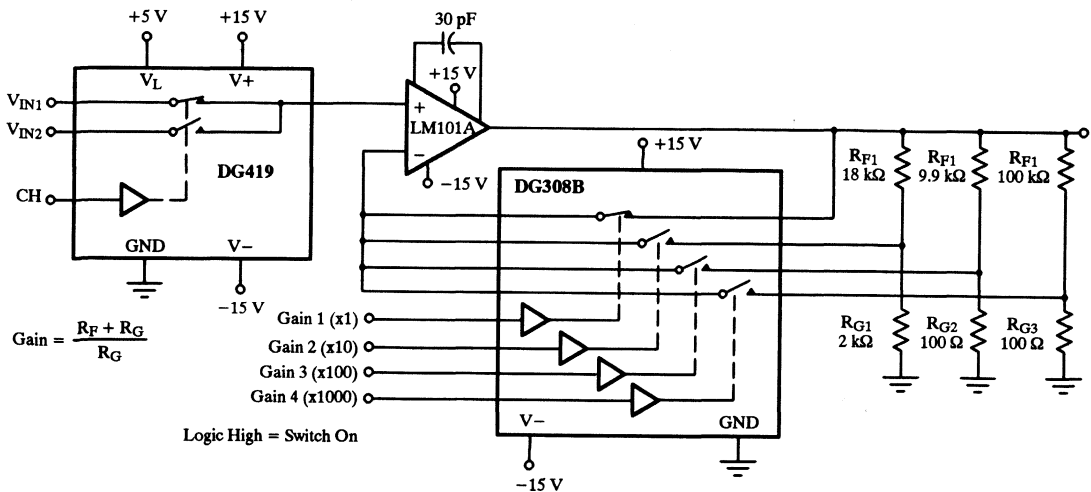
**Figure 4.** Channel-to-Channel Crosstalk



$\Delta V_O =$  measured voltage error due to charge injection  
The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

**Figure 5.** Charge Injection

**Applications**



**Figure 7.** A Precision Amplifier with Digitally Programmable Inputs and Gains

## Applications (Cont'd)

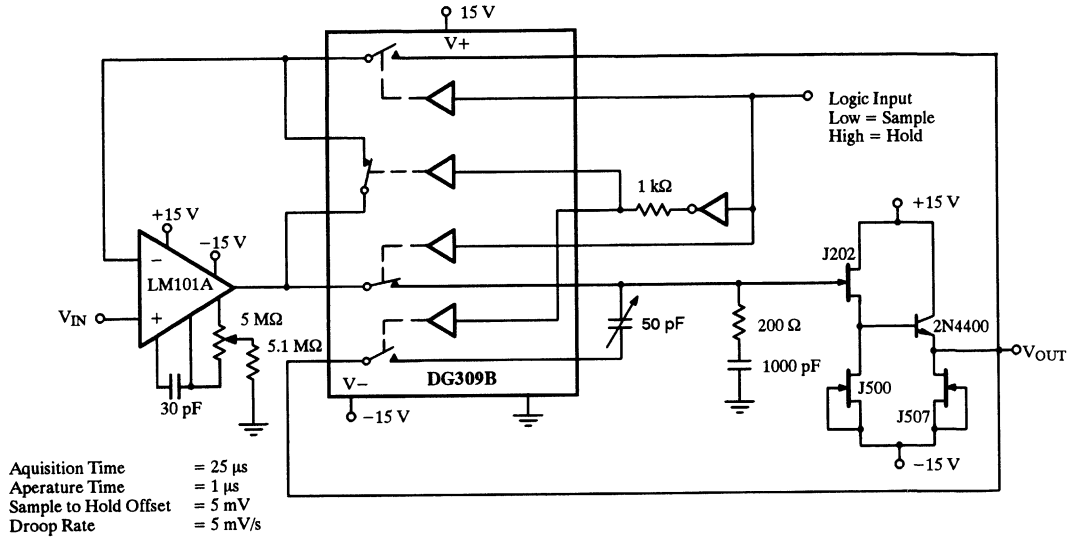
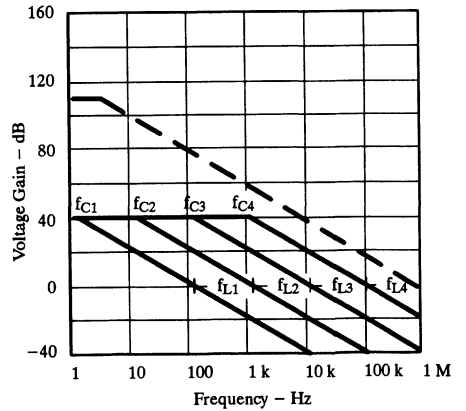
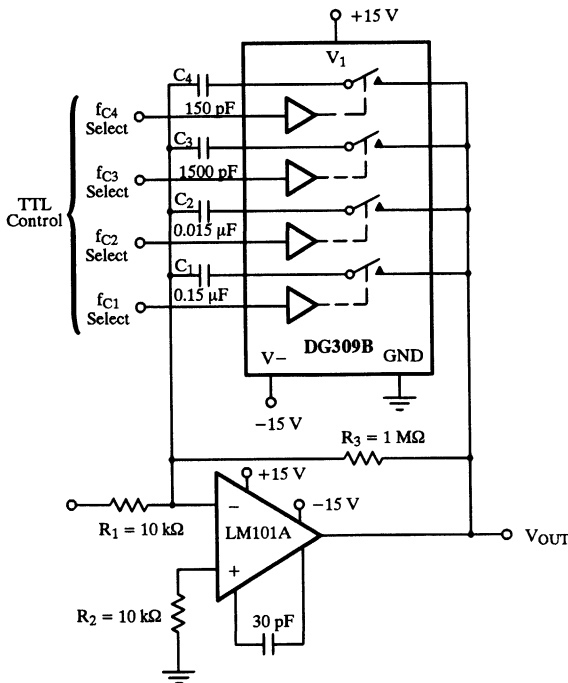


Figure 8. Sample-and-Hold



$$A_L \text{ (Voltage Gain Below Break Frequency)} = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (Break Frequency)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (Unity Gain Frequency)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{Max Attenuation} = \frac{r_{DS(on)}}{10 \text{ k}\Omega} \approx -40 \text{ dB}$$

Figure 9. Active Low Pass Filter with Digitally Selected Break Frequency

## CMOS Analog Switches

### Features

- $\pm 15\text{-V}$  Input Range
- Low  $r_{DS(on)}$ :  $30\ \Omega$
- Single Supply Operation
- Pin and Function Compatible with the JFET DG180 Family

### Benefits

- Full Rail-to-Rail Analog Signal Range
- Minimizes Signal Error
- Low Power Dissipation

### Applications

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

### Description

The DG381A–DG390A series of monolithic CMOS analog switches was designed for applications in instrumentation, communications, and process control. This series is suited for applications requiring fast switching and nearly flat on-resistance over the entire voltage range.

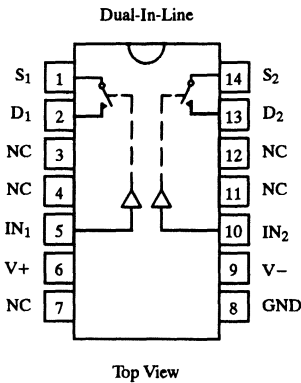
Designed on Siliconix' PLUS-40 CMOS process, these devices achieve low power consumption (3.5 mW typical) and excellent on/off switch performance. These switches

are ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation is allowed by connecting the  $V^-$  rail to 0 V.

Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS and quasi TTL logic compatible.

### Functional Block Diagram and Pin Configuration

#### DG381A



Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0"  $\leq 0.8\text{ V}$   
Logic "1"  $\geq 4\text{ V}$

Switches Shown for Logic "1" Input

#### Ordering Information – DG381A

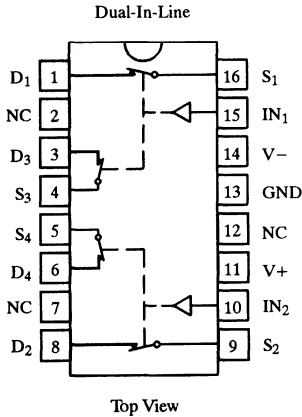
Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG381ACJ
-55 to 125°C	14-Pin CerDIP	DG381AAK/883

1

# DG381A/384A/387A/390A

## Functional Block Diagram and Pin Configuration (Cont'd)

### DG384A



Truth Table

Logic	Switch
0	OFF
1	ON

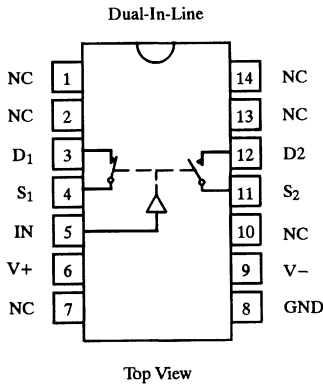
Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 4$  V

Switches Shown for Logic "1" Input

Ordering Information – DG384A

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG384ACJ
-55 to 125°C	16-Pin CerDIP	DG384AAK/883

### DG387A



Truth Table

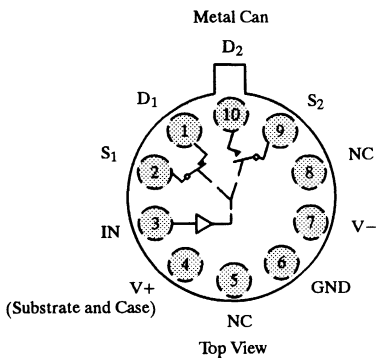
Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 4$  V

Switches Shown for Logic "1" Input

Ordering Information – DG387A

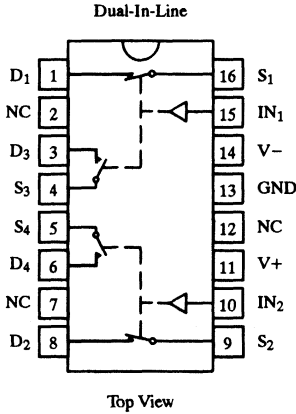
Temp Range	Package	Part Number
0 to 70°C	14-Pin Plastic DIP	DG387ACJ
-55 to 125°C	14-Pin CerDIP	DG387AAK/883
	10-Pin Metal Can	DG387AAA/883





## Functional Block Diagram and Pin Configuration (Cont'd)

### DG390A



Truth Table

Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 4 V

Switches Shown for Logic "1" Input

Ordering Information – DG390A

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG390ACJ
-25 to 85°C	16-Pin CerDIP	DG390ABK
		DG390AAK
		DG390AAK/883
-55 to 125°C		

## Absolute Maximum Ratings

Voltages Referenced to V-

V+	44 V
GND	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2V or 30 mA, whichever occurs first
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	30 mA
(Pulsed at 1 ms, 10% duty cycle max)	100 mA
Storage Temperature (AAA, AAK, ACK Suffix)	-65 to 150°C
(ACJ Suffix)	-65 to 125°C

Power Dissipation<sup>b</sup>

14-Pin Plastic DIP <sup>d</sup>	470 mW
14-Pin CerDIP <sup>c</sup>	825 mW
10-Pin Metal Can <sup>e</sup>	450 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 11 mW/°C above 75°C
- Derate 6.5 mW/°C above 25°C
- Derate 6 mW/°C above 75°C

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 0.8 V or 4 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C Suffix 0 to 70°C -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = -10 mA	Room Full	30		50 75		50 75	Ω
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room Hot	±0.1	-1 -100	1 100	-5 -100	5 100	nA
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>S</sub> = ±14 V, V <sub>D</sub> = ∓14 V	Room Hot	±0.1	-1 -100	1 100	-5 -100	5 100	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = ±14 V	Room Hot	±0.1	-11 -100	1 100	-5 -100	5 100	

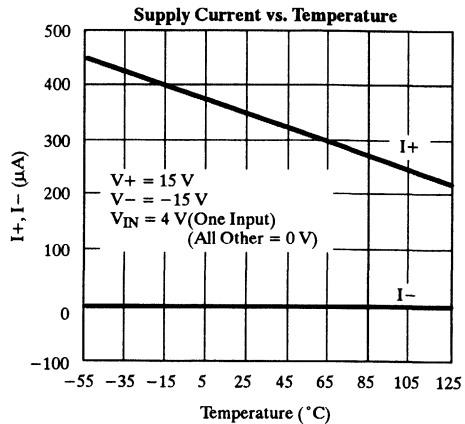
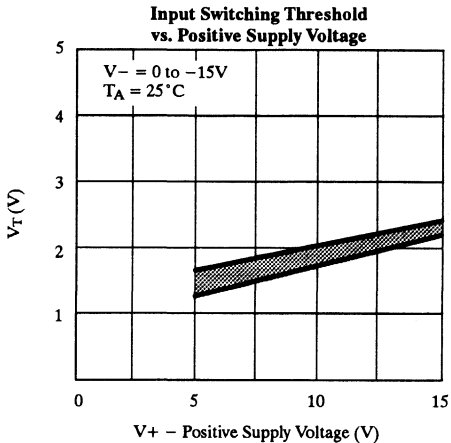
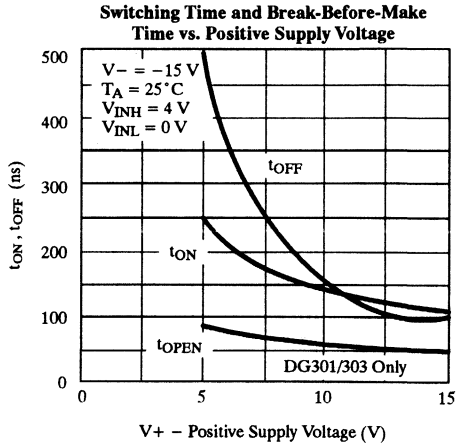
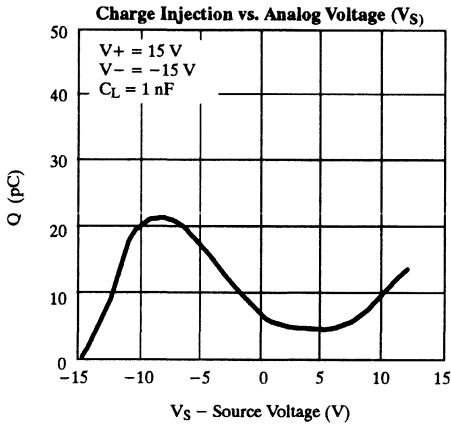
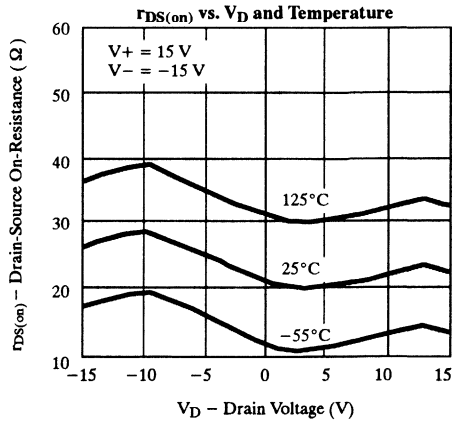
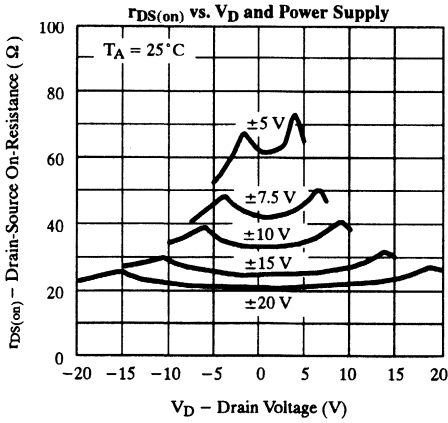
## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{IN} = 0.8\text{ V}$ or $4\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C Suffix 0 to 70°C -25 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Digital Control</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 5\text{ V}$	Room Full	-0.01	-1		-1		$\mu\text{A}$
		$V_{IN} = 15\text{ V}$	Room Full	0.001		1		1	
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Room Full	-0.01	-1		-1		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	See Figure 2	Room	150		300			ns
Turn-Off Time	$t_{OFF}$		Room	130		250			
Break-Before-Make Time	$t_{OPEN}$	See Figure 3	Room	50					
Charge Injection	Q	$C_L = 0.01\ \mu\text{F}$ , $R_{gen} = 0\ \Omega$ , $V_{gen} = 0\text{ V}$	Room	10					pC
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$ , $V_S$ , $V_D = 0\text{ V}$	Room	14					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	14					
Channel-On Capacitance	$C_{D(on)}$		Room	40					
Input Capacitance	$C_{IN}$	$f = 1\text{ MHz}$	$V_{IN} = 0\text{ V}$	Room	6				
			$V_{IN} = 15\text{ V}$	Room	7				
Off-Isolation	OIRR	$V_{IN} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$ $V_S = 1\text{ V}_{rms}$ , $f = 500\text{ kHz}$	Room	62					dB
Crosstalk (Channel-to-Channel)	XTALK		Room	74					
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_{IN} = 4\text{ V}$ (One Input) (All Others = 0)	Room Full	0.23		0.5 1.0		1	mA
Negative Supply Current	I-		Room Full	-0.01	-10		-100		
Positive Supply Current	I+	$V_{IN} = 0.8\text{ V}$ (All Inputs)	Room Full	0.001		10 100		100	$\mu\text{A}$
Negative Supply Current	I-		Room Full	-0.01	-10		-100		

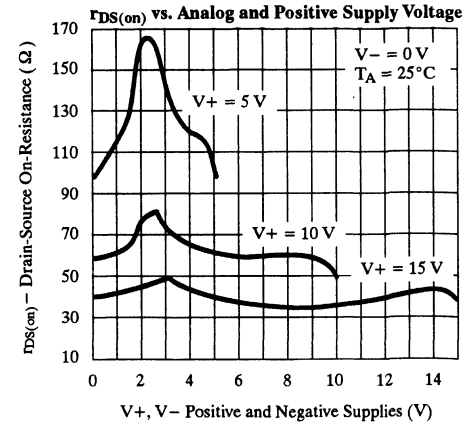
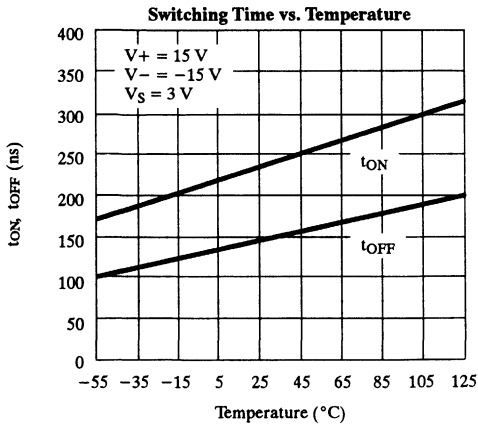
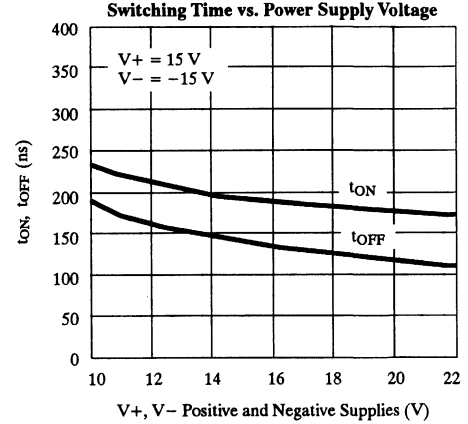
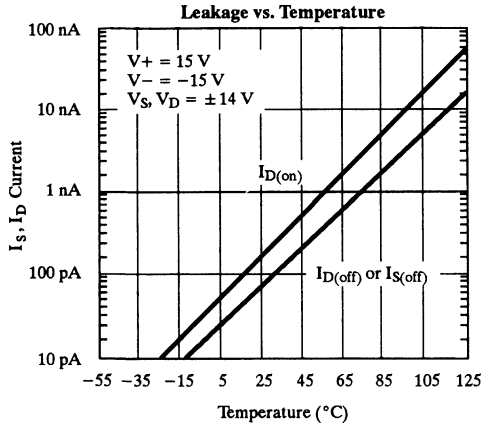
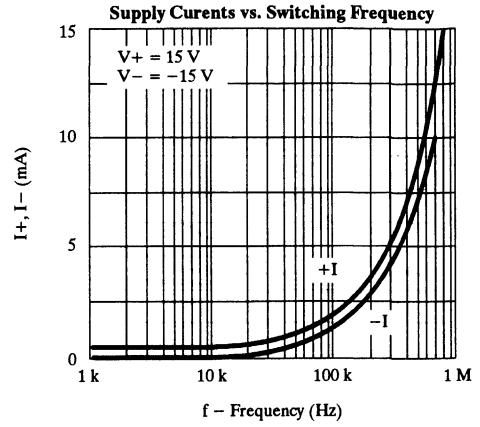
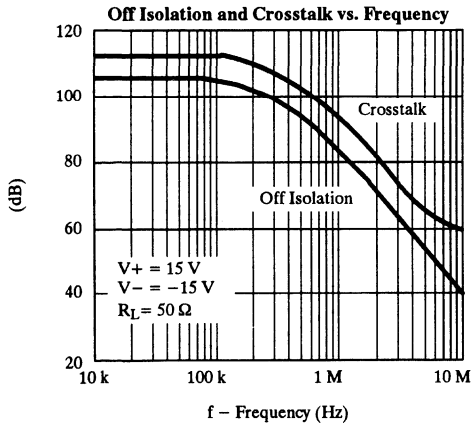
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**



## Typical Characteristic (Cont'd)



## Schematic Diagram (Typical Channel)

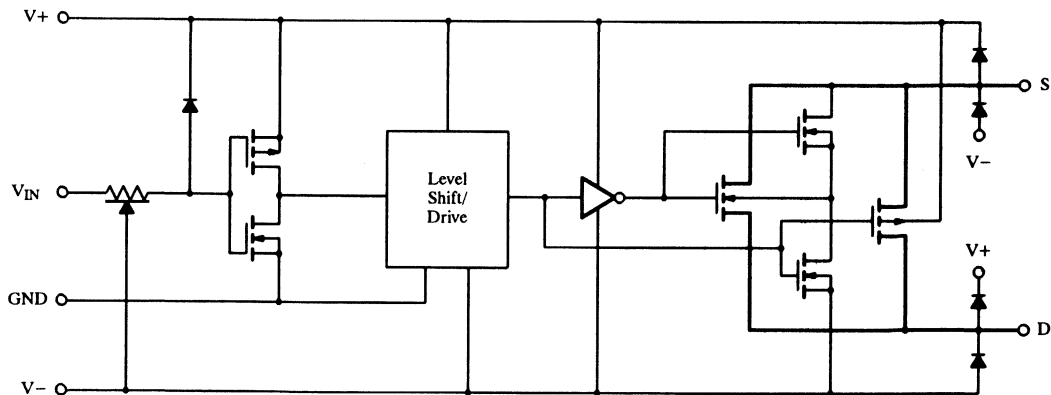


Figure 1.

## Test Circuits

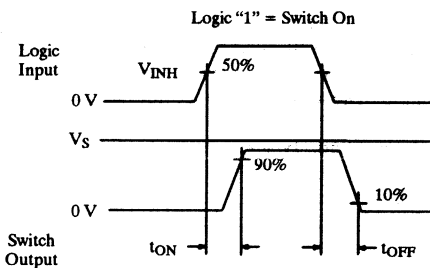
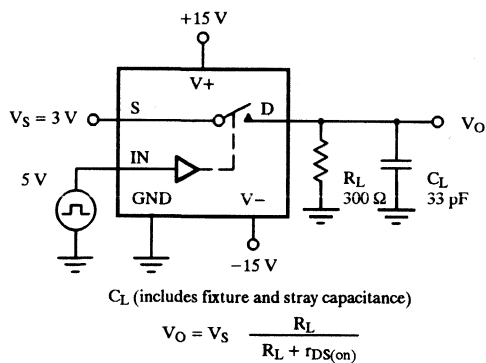
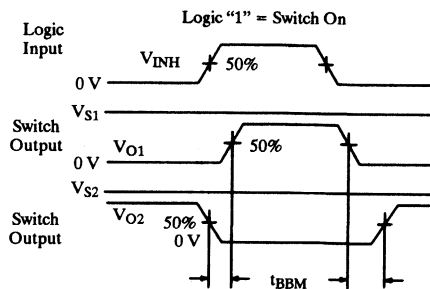
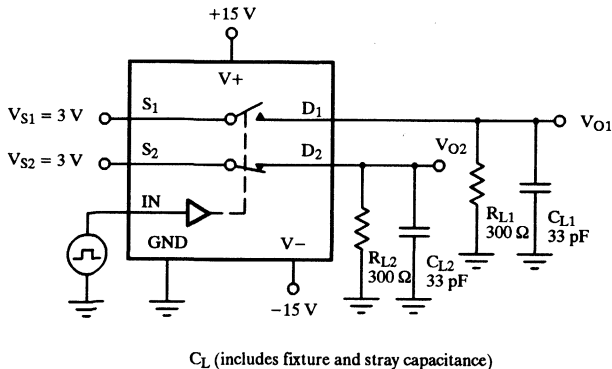


Figure 2. Switching Time



$C_L$  (includes fixture and stray capacitance)

Figure 3. Break-Before-Make SPDT (DG301A, DG303A)

## Test Circuits (Cont'd)

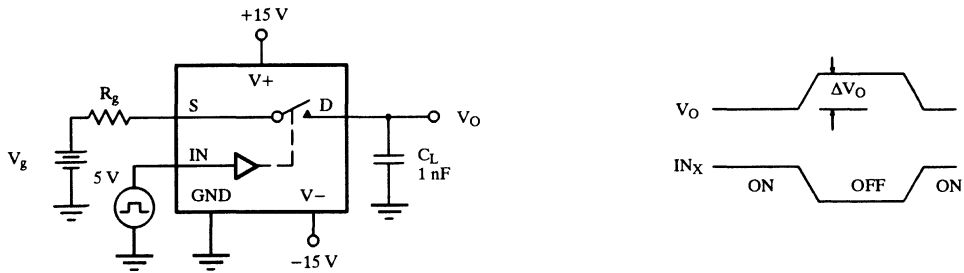


Figure 4. Charge Injection

## Applications

The DG381A series of analog switches will switch positive analog signals while using a single positive supply. This allows their use in applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) increased  $r_{DS(on)}$ , 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied (see Typical Characteristics). The analog voltage should not go above or below the supply voltages which in single operation are  $V+$  and 0 V.

In the integrator of Figure 4,  $R_D$  controls the discharge rate of the capacitor so that the pulsed or continuous current ratings are not exceeded. During reset  $SW_1$  is closed and  $SW_2$  is open. Opening  $SW_2$  with  $SW_1$  also open will hold the integrator output at its present value.

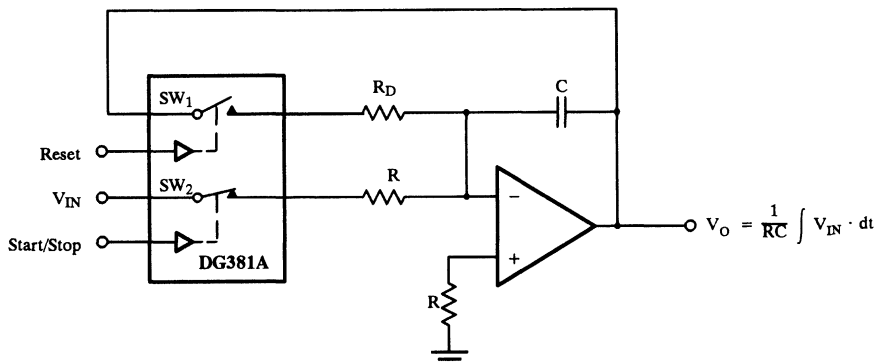


Figure 5. Integrator with Reset and Start/Stop

## Low-Power, High-Speed CMOS Analog Switches

### Features

- 44-V Supply Max Rating
- $\pm 15\text{-V}$  Analog Signal Range
- On-Resistance— $r_{DS(on)}$ : 20  $\Omega$
- Low Leakage— $I_{D(on)}$ : 40 pA
- Fast Switching— $t_{ON}$ : 100 ns
- Ultra Low Power Requirements— $P_D$ : 0.35  $\mu\text{W}$
- TTL, CMOS Compatible
- Single Supply Capability

### Benefits

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

### Applications

- Audio and Video Switching
- Sample-and-Hold Circuits
- Battery Operation
- Test Equipment
- Hi-Rel Systems
- PBX, PABX

### Description

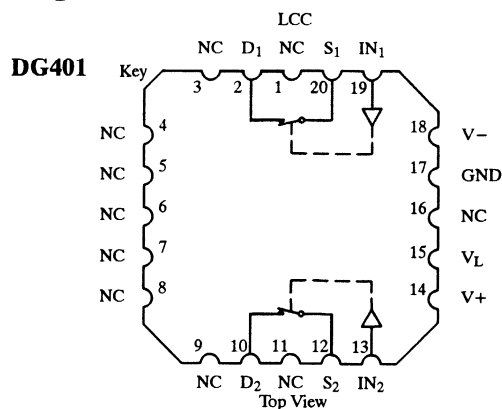
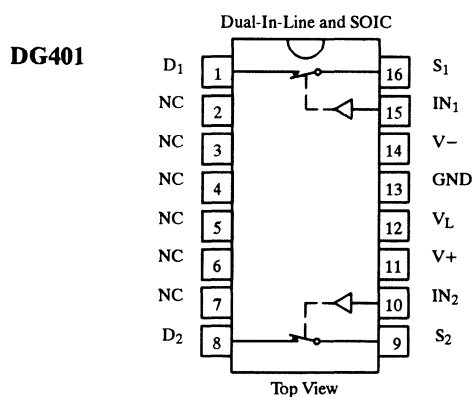
The DG401/403/405 monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (0.35  $\mu\text{W}$ , typ) with high speed ( $t_{ON}$ : 100 ns, typ), the DG401 series is ideally suited for portable and battery powered industrial and military applications.

Built on the Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full  $\pm 15\text{-V}$  analog range, rivaling JFET performance without the inherent dynamic range limitations.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams.

### Functional Block Diagrams and Pin Configurations



#### Ordering Information – DG401

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG401DJ
		DG401AK
-55 to 125°C	16-Pin CerDIP	DG401AK/883
		LCC-20

#### Two SPST Switches per Package

#### Truth Table

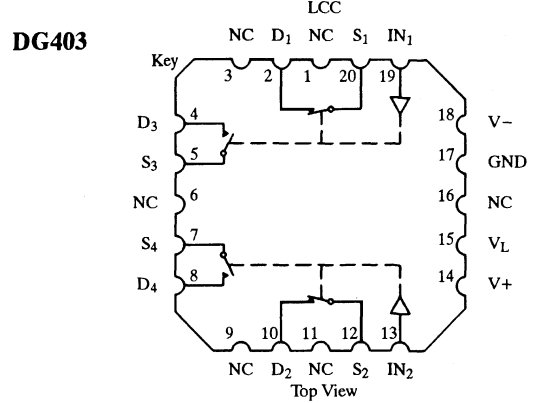
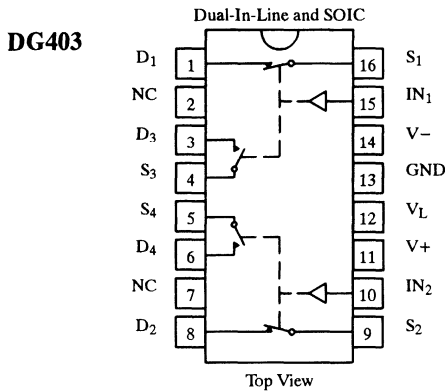
Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq 0.8\text{ V}$   
Logic "1"  $\geq 2.4\text{ V}$

Switches Shown for Logic "1" Input

**1**

## Functional Block Diagrams and Pin Configurations (Cont'd)



### Ordering Information - DG403

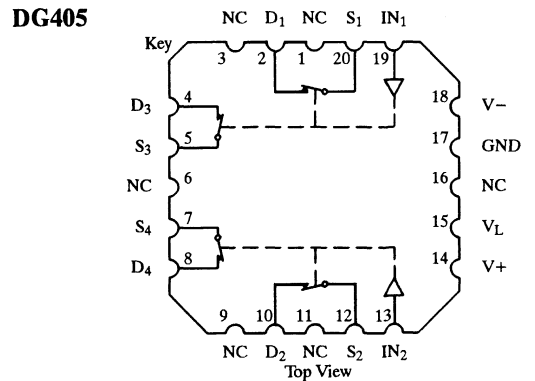
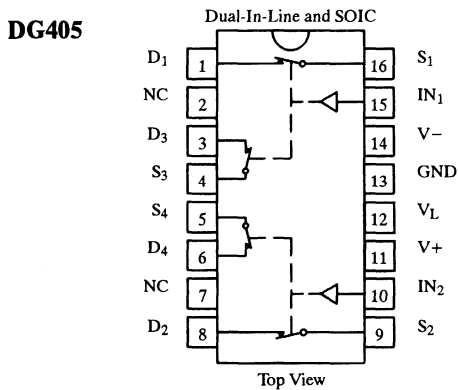
Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG403DJ
	16-Pin Narrow SOIC	DG403DY
-55 to 125°C	16-Pin CerDIP	DG403AK
		DG403AK/883
	LCC-20	DG403AZ/883

### Two SPDT Switches per Package

Truth Table		
Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input



### Ordering Information - DG405

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG405DJ
	16-Pin Narrow SOIC	DG405DY
-55 to 125°C	16-Pin CerDIP	DG405AK
		DG405AK/883
	LCC-20	DG405AZ/883

### Two DPST Switches per Package

Truth Table	
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input



**Absolute Maximum Ratings**

V+ to V-	44 V
GND to V-	25 V
V <sub>L</sub>	(GND - 0.3 V) to (V+) + 0.3 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>	(V-) - 2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous	30 mA
Current, S or D (Pulsed 1 ms 10% duty)	100 mA
Storage Temperature (AK, AZ Suffix)	-65 to 150°C
(DJ, DY Suffix)	-65 to 125°C
Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	450 mW
16-Pin CerDIP <sup>d</sup>	900 mW
16-Pin SOIC <sup>e</sup>	600 mW
LCC-20 <sup>f</sup>	900 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C
- Derate 12 mW/°C above 75°C
- Derate 7.6 mW/°C above 75°C
- Derate 13 mW/°C above 75°C

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>L</sub> = 5 V, V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±10 V V+ = 13.5 V, V- = -13.5 V	Room Full	20		35 45		45 55	Ω
Δ Drain-Source On-Resistance	Δr <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±5 V, 0 V V+ = 16.5 V, V- = -16.5 V	Room Full	3		3 5		3 5	
Switch Off Leakage Current	I <sub>S(off)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ±15.5 V	Room Hot	-0.01	-0.25 -20	0.25 20	-0.5 -5	0.5 5	nA
	I <sub>D(off)</sub>		Room Hot	-0.01	-0.25 -20	0.25 20	-0.5 -5	0.5 5	
Channel On Leakage Current	I <sub>D(on)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>S</sub> = V <sub>D</sub> = ±15.5 V	Room Hot	-0.04	-0.4 -40	0.4 40	-1 -10	1 10	
<b>Digital Control</b>									
Input Current V <sub>IN</sub> Low	I <sub>IL</sub>	V <sub>IN</sub> under test = 0.8 V All Other = 2.4 V	Full	0.005	-1	1	-1	1	μA
Input Current V <sub>IN</sub> High	I <sub>IH</sub>	V <sub>IN</sub> under test = 2.4 V All Other = 0.8 V	Full	0.005	-1	1	-1	1	
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF See Figure 2	Room	100		150		150	ns
Turn-Off Time	t <sub>OFF</sub>		Room	60		100		100	
Break-Before-Make Time Delay (DG403)	t <sub>D</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF	Room	12	5		5		
Charge Injection	Q	C <sub>L</sub> = 10,000 pF V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	Room	60					pC
Off Isolation Reject Ratio	OIRR	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	Room	72					dB
Channel-to-Channel Crosstalk	X <sub>TALK</sub>		Room	90					



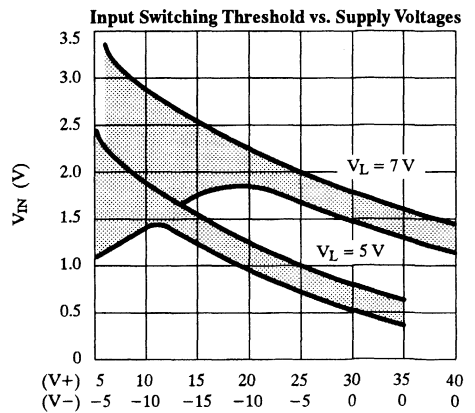
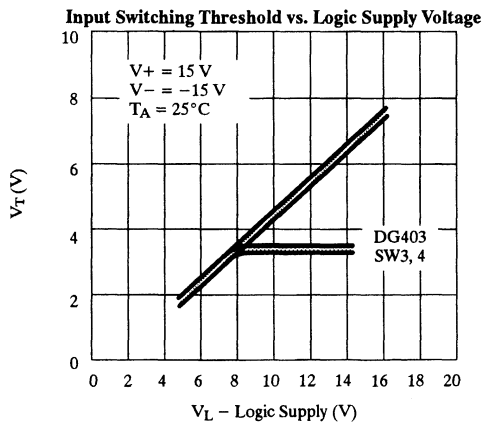
## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Dynamic Characteristics (Cont'd)</b>									
Source Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}, V_S = 0\text{ V}$	Room	12					pF
Drain Off Capacitance	$C_{D(off)}$		Room	12					
Channel On Capacitance	$C_D, C_{S(on)}$		Room	39					
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room Full	0.01		1 5		1 5	μA
Negative Supply Current	$I_-$		Room Full	-0.01	-1 -5		-1 -5		
Logic Supply Current	$I_L$		Room Full	0.01		1 5		1 5	
Ground Current	$I_{GND}$		Room Full	-0.01	-1 -5		-1 -5		

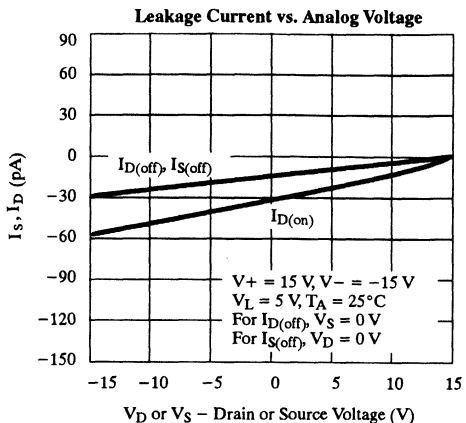
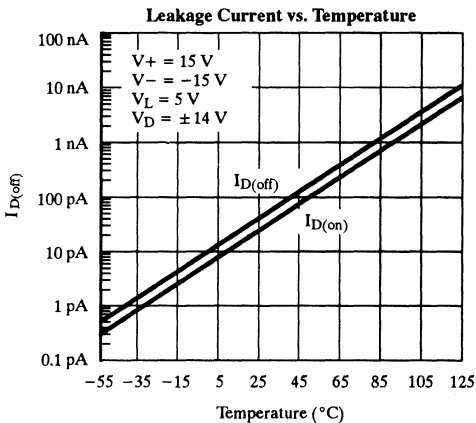
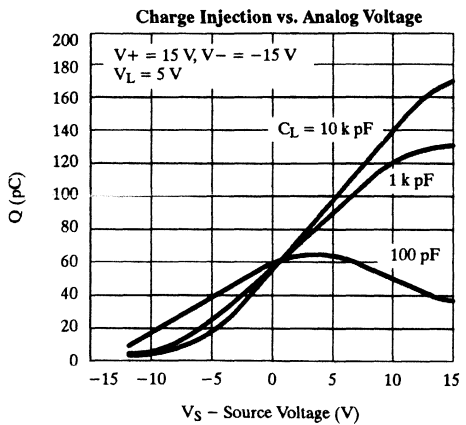
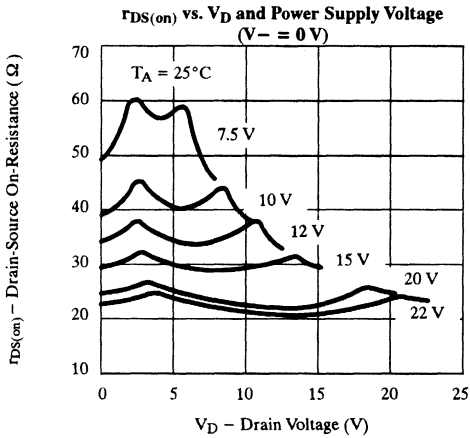
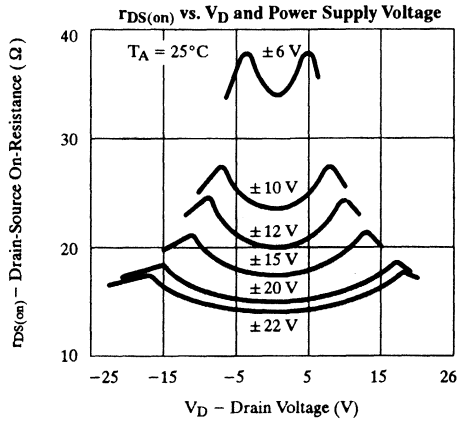
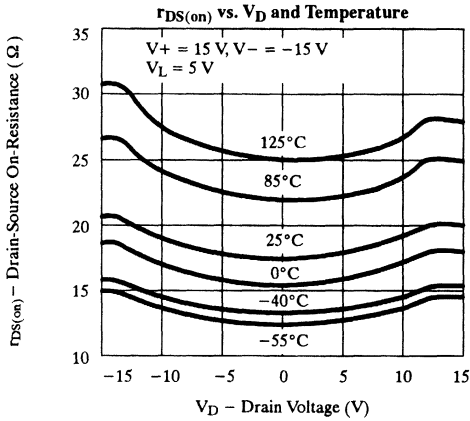
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
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- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

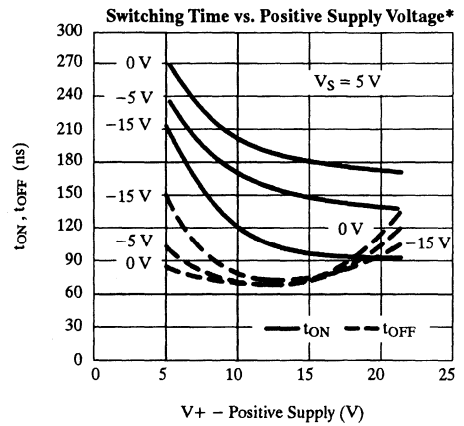
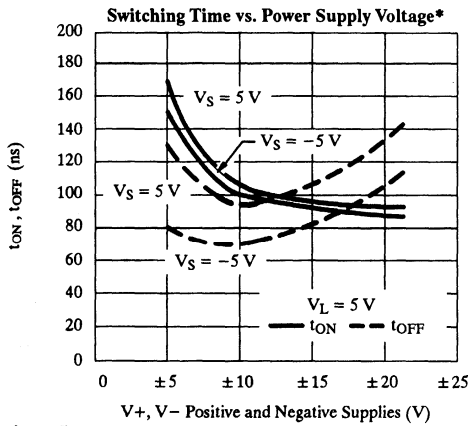
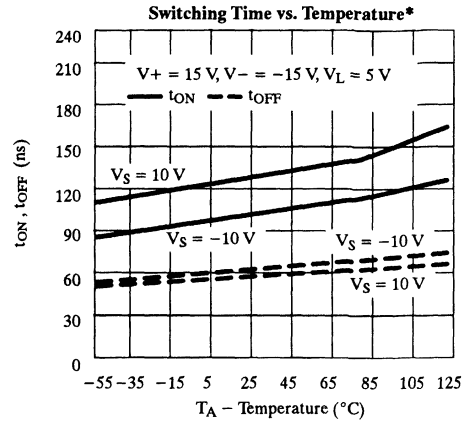
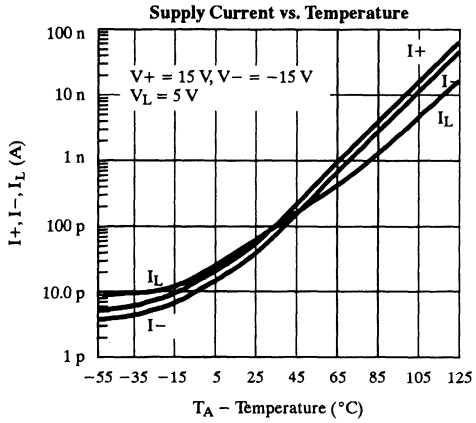
## Typical Characteristics



**Typical Characteristics (Cont'd)**



## Typical Characteristics (Cont'd)



\*Refer to Figure 2 for test conditions.

## Schematic Diagram (Typical Channel)

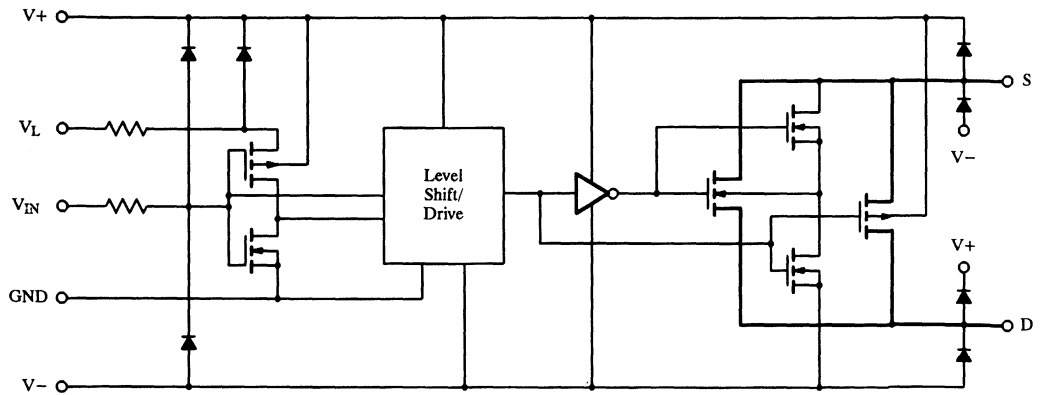
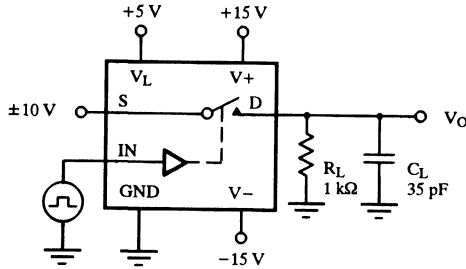


Figure 1.

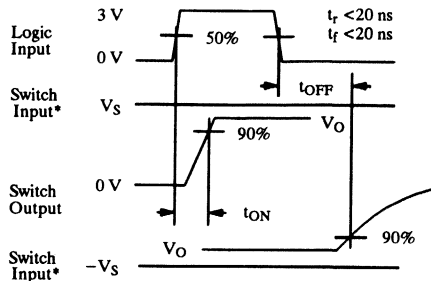
**Test Circuits**

$V_O$  is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



$C_L$  (includes fixture and stray capacitance)

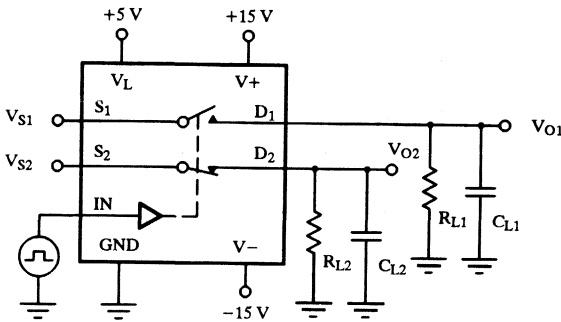
$$V_O = V_S \frac{R_L}{R_L + \tau_{DS(on)}}$$



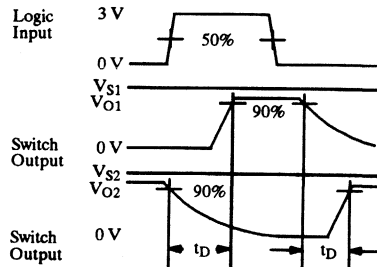
\* $V_S = 10\text{ V}$  for  $t_{ON}$ ,  $V_S = -10\text{ V}$  for  $t_{OFF}$

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

**Figure 2. Switching Time**

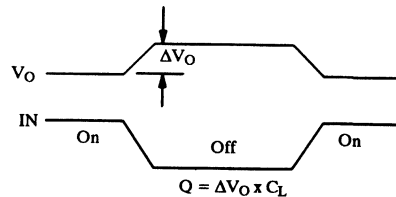
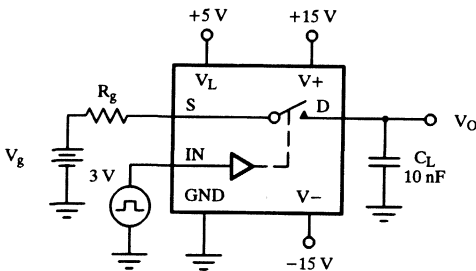


$C_L$  (includes fixture and stray capacitance)



**Figure 3. Break-Before-Make**

**1**



**Figure 4. Charge Injection**

## Test Circuits (Cont'd)

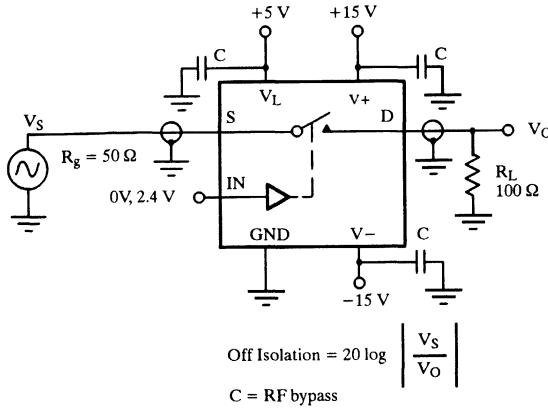


Figure 5. Off Isolation

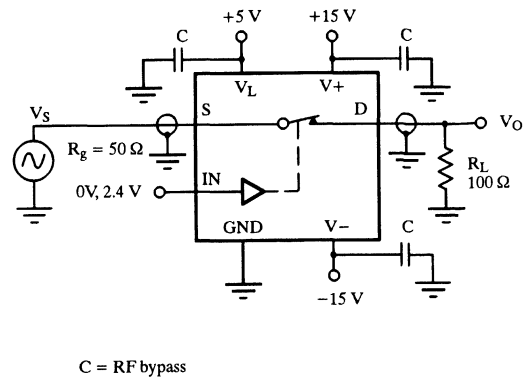


Figure 6. Insertion Loss

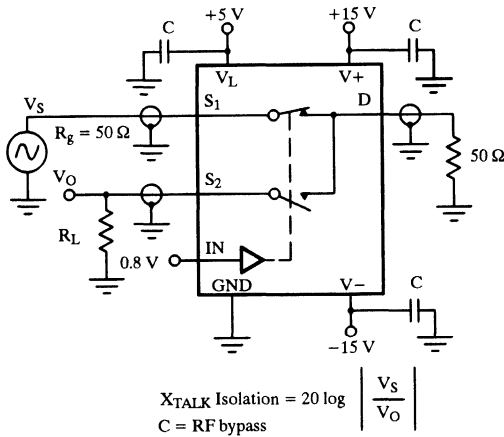


Figure 7. Crosstalk

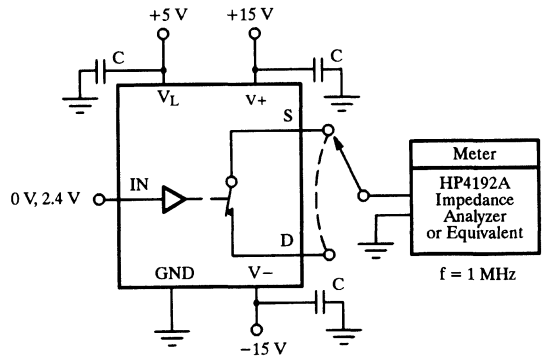


Figure 8. Capacitances

## Applications

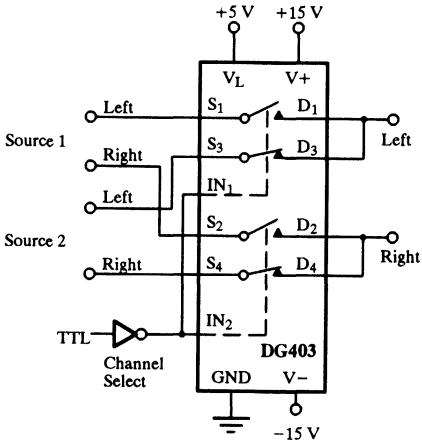
### Stereo Source Selector:

A single logic signal controls the status of all four switches of the device, simplifying stereo source switching. The low on-resistance (<35 Ω) minimizes total harmonic distortion.

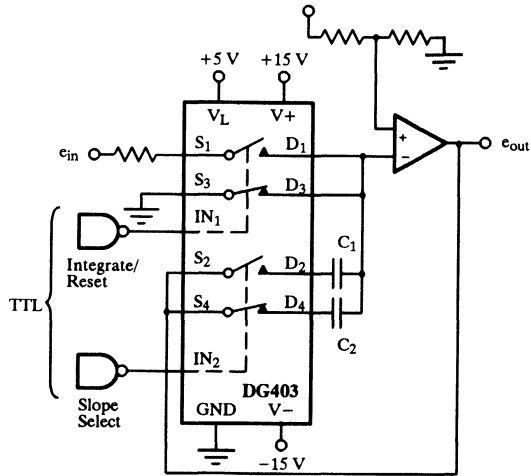
### Dual Slope Integrators:

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C<sub>1</sub> or C<sub>2</sub>. Another one selects e<sub>in</sub> or discharges the capacitor in preparation for the next integration cycle.

**Applications (Cont'd)**



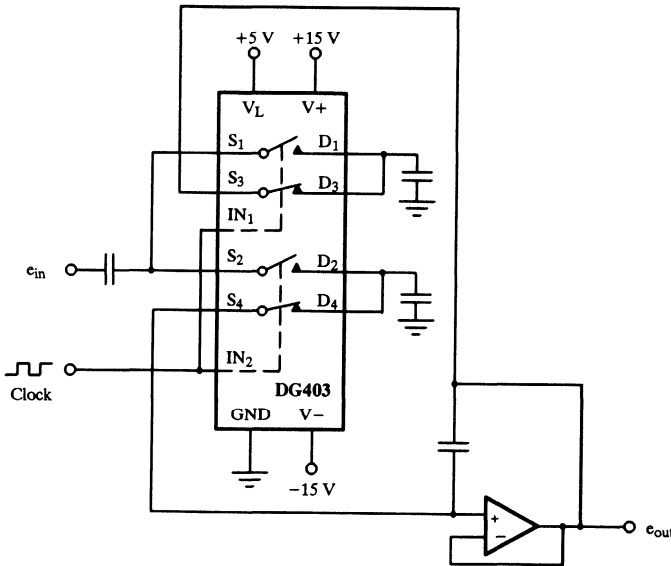
**Figure 9.** Stereo Source Selector



**Figure 10.** Dual Slope Integrator

**Band-Pass Switched Capacitor Filter:**

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.



**Figure 11.** Band-Pass Switched Capacitor Filter





## Precision Monolithic Quad SPST CMOS Analog Switches

### Features

- 44-V Supply Max Rating
- $\pm 15\text{-V}$  Analog Signal Range
- On-Resistance— $r_{DS(on)}$ : 25  $\Omega$
- Fast Switching— $t_{ON}$ : 110 ns
- Ultra Low Power— $P_D$ : 0.35  $\mu\text{W}$
- TTL, CMOS Compatible
- Single Supply Capability

### Benefits

- Widest Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

### Applications

- Precision Automatic Test Equipment
- Precision Data Acquisition
- Communication Systems
- Battery Powered Systems
- Computer Peripherals

### Description

The DG411 series of monolithic quad analog switches was designed to provide high speed, low error switching of precision analog signals. Combining low power (0.35  $\mu\text{W}$ ) with high speed ( $t_{ON}$ : 110 ns), the DG411 family is ideally suited for portable and battery powered industrial and military applications.

To achieve high-voltage ratings and superior switching performance, the DG411 series was built on Siliconix's high

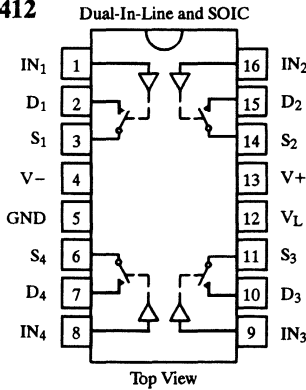
voltage silicon gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages up to the supply levels when off.

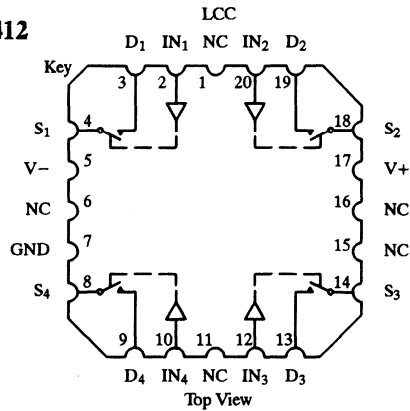
The DG411 and DG412 respond to opposite control logic as shown in the Truth Table. The DG413 has two normally open and two normally closed switches.

### Functional Block Diagram and Pin Configuration

DG411/412



DG411/412



Ordering Information – DG411/412

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG411DJ
		DG412DJ
-40 to 85°C	16-Pin Narrow SOIC	DG411DY
		DG412DY
-55 to 125°C	16-Pin CerDIP	DG411AK, DG411AK/883, 5962-9073101MEA
		DG412AK, DG412AK/883, 5962-9073102MEA
	LCC-20	DG411AZ/883, 5962-9073101M2A
		DG412AZ/883, 5962-9073102M2A

Truth Table

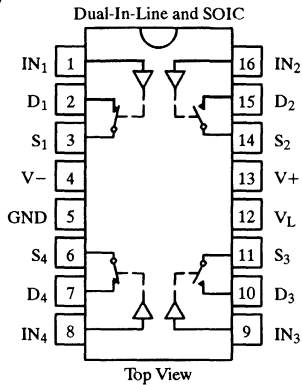
Logic	DG411	DG412
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8\text{ V}$   
Logic "1"  $\geq 2.4\text{ V}$

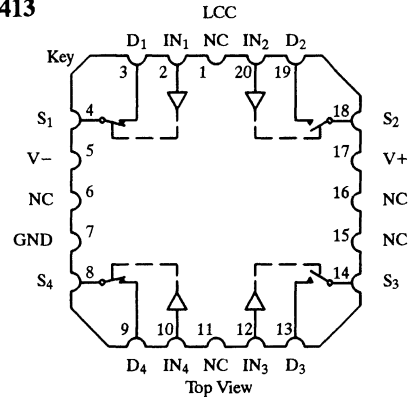
Switches Shown for DG411 Logic "1" Input



## DG413



## DG413



### Ordering Information – DG413

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG413DJ
	16-Pin Narrow SOIC	DG413DY
-55 to 125°C	16-Pin CerDIP	DG413AK, DG413AK/883, 5962-9073103MEA
	LCC-20	DG413AZ/883, 5962-9073103M2A

### Truth Table

Logic	SW <sub>1</sub> , SW <sub>4</sub>	SW <sub>2</sub> , SW <sub>3</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V

Switches Shown for DG411 Logic "1" Input

## Absolute Maximum Ratings

V+ to V-	44 V
GND to V-	25 V
V <sub>L</sub>	(GND -0.3 V) (V+) +0.3 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Current, S or D (Pulsed 1 ms, 10% Duty Cycle)	100 mA
Storage Temperature (AK, AZ Suffix)	-65 to 150°C
(DJ, DY Suffix)	-65 to 125°C
Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	470 mW

16-Pin Narrow SOIC <sup>d</sup>	600 mW
16-Pin CerDIP <sup>e</sup>	900 mW
LCC-20 <sup>e</sup>	900 mW

### Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 25°C
- Derate 7.6 mW/°C above 75°C
- Derate 12 mW/°C above 75°C

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-15	15	-15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_+ = 13.5\text{ V}, V_- = -13.5\text{ V}$ $I_S = -10\text{ mA}, V_D = \pm 8.5\text{ V}$	Room Full	25		35 45		35 45	$\Omega$
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}, V_S = \mp 15.5\text{ V}$	Room Full	$\pm 0.1$	-0.25 -20	0.25 20	-0.25 -5	0.25 5	nA
	$I_{D(off)}$		Room Full	$\pm 0.1$	-0.25 -20	0.25 20	-0.25 -5	0.25 5	
Channel On Leakage Current	$I_{D(on)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_S = V_D = \pm 15.5\text{ V}$	Room Full	$\pm 0.1$	-0.4 -40	0.4 40	-0.4 -10	0.4 10	
<b>Digital Control</b>									
Input Current, $V_{IN}$ Low	$I_{IL}$	$V_{IN}$ Under Test = 0.8 V	Full	0.005	-0.5	0.5	-0.5	0.5	$\mu\text{A}$
Input Current, $V_{IN}$ High	$I_{IH}$	$V_{IN}$ Under Test = 2.4 V	Full	0.005	-0.5	0.5	-0.5	0.5	
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$ See Figure 2	Room Full	110		175 240		175 220	ns
Turn-Off Time	$t_{OFF}$		Room Full	100		145 160		145 160	
Break-Before-Make Time Delay	$t_D$	DG413 Only, $V_S = 10\text{ V}$ $R_L = 300\ \Omega, C_L = 35\text{ pF}$	Room	25					
Charge Injection	Q	$V_g = 0\text{ V}, R_g = 0\ \Omega, C_L = 10\text{ nF}$	Room	5					pC
Off Isolation <sup>e</sup>	OIRR	$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room	68					dB
Channel-to-Channel Crosstalk <sup>e</sup>	$X_{TALK}$		Room	85					
Source Off Capacitance <sup>e</sup>	$C_{S(off)}$	f = 1 MHz	Room	9					pF
Drain Off Capacitance <sup>e</sup>	$C_{D(off)}$		Room	9					
Channel On Capacitance <sup>e</sup>	$C_{D(on)}$		Room	35					
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room Full	0.0001		1 5		1 5	$\mu\text{A}$
Negative Supply Current	I-		Room Full	-0.0001	-1 -5		-1 -5		
Logic Supply Current	$I_L$		Room Full	0.0001		1 5		1 5	
Ground Current	$I_{GND}$		Room Full	-0.0001	-1 -5		-1 -5		

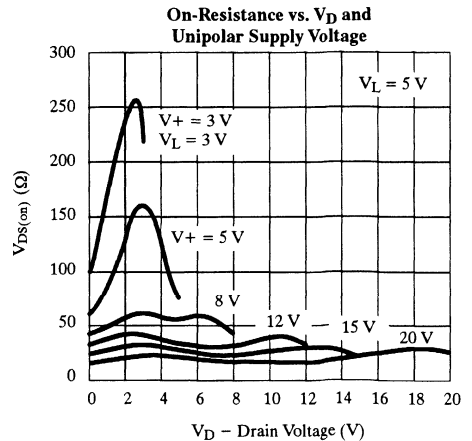
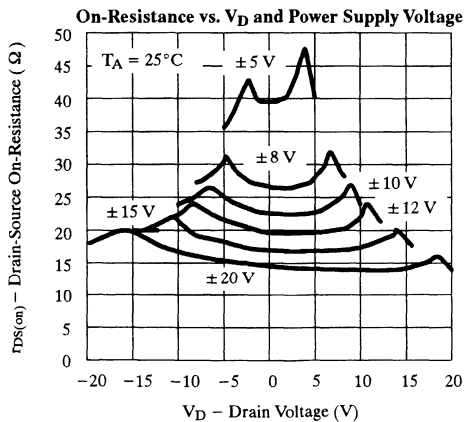
## Specifications<sup>a</sup> for Unipolar Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full			12		12	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_+ = 10.8\text{ V}, I_S = -10\text{ mA}$ $V_D = 3\text{ V}, 8\text{ V}$	Room Full	40		80 100		80 100	$\Omega$
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ $V_S = 8\text{ V}$ , See Figure 2	Room Hot	175		250 400		250 315	ns
Turn-Off Time	$t_{OFF}$		Room Hot	95		125 140		125 140	
Break-Before-Make Time Delay	$t_D$	DG413 Only $V_S = 8\text{ V}, R_L = 300\ \Omega, C_L = 35\text{ pF}$	Room	25					
Charge Injection	Q	$V_g = 6\text{ V}, R_g = 0\ \Omega, C_L = 10\text{ nF}$	Room	25					pC
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_+ = 13.5, V_{IN} = 0\text{ or }5\text{ V}$	Room Hot	0.0001		1 5		1 5	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Hot	-0.0001		-1 -5		-1 -5	
Logic Supply Current	$I_L$		Room Hot	0.0001		1 5		1 5	
Ground Current	$I_{GND}$		Room Hot	-0.0001		-1 -5		-1 -5	

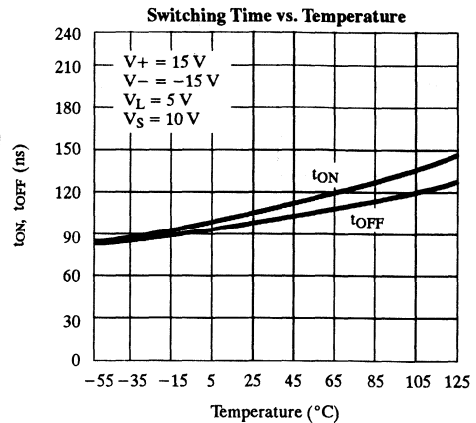
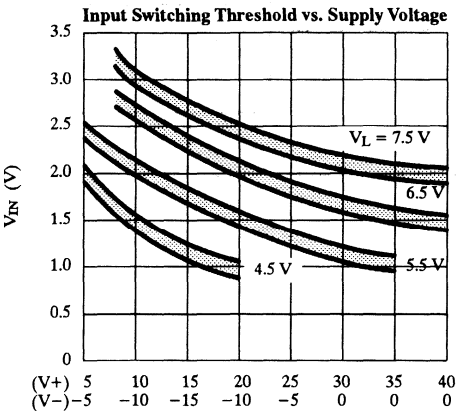
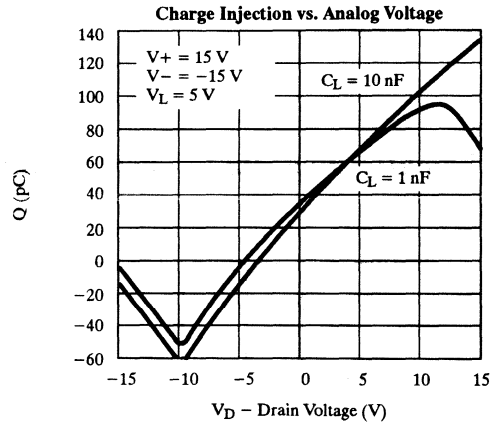
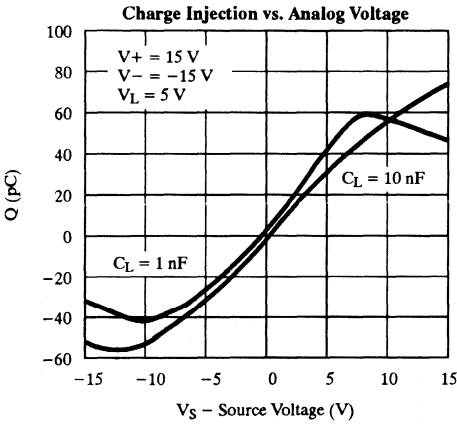
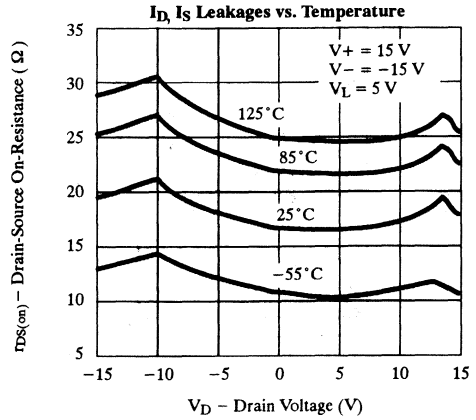
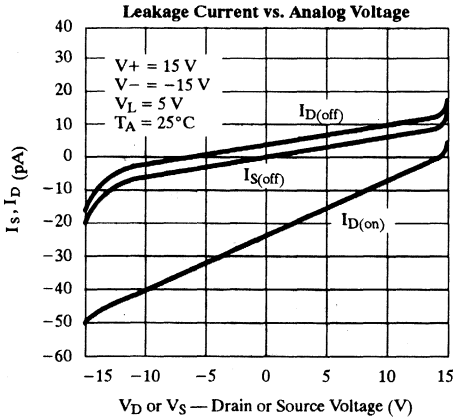
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

## Typical Characteristics

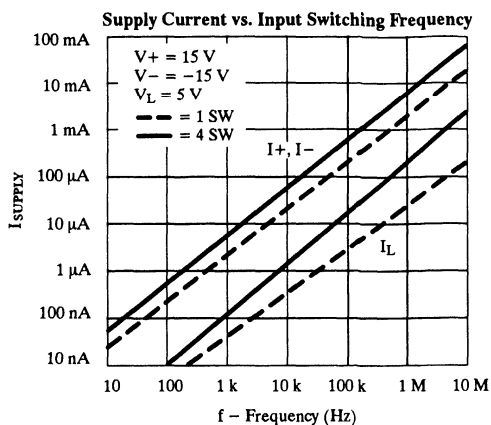
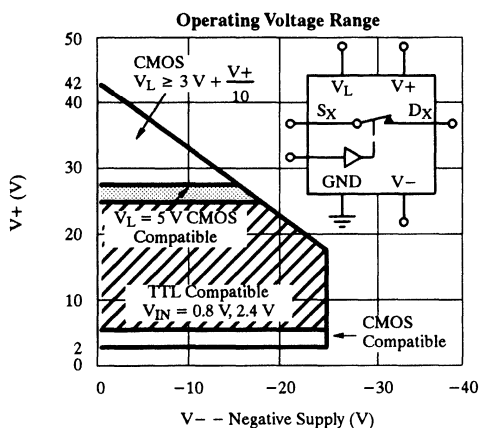


**Typical Characteristics (Cont'd)**



**1**

## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

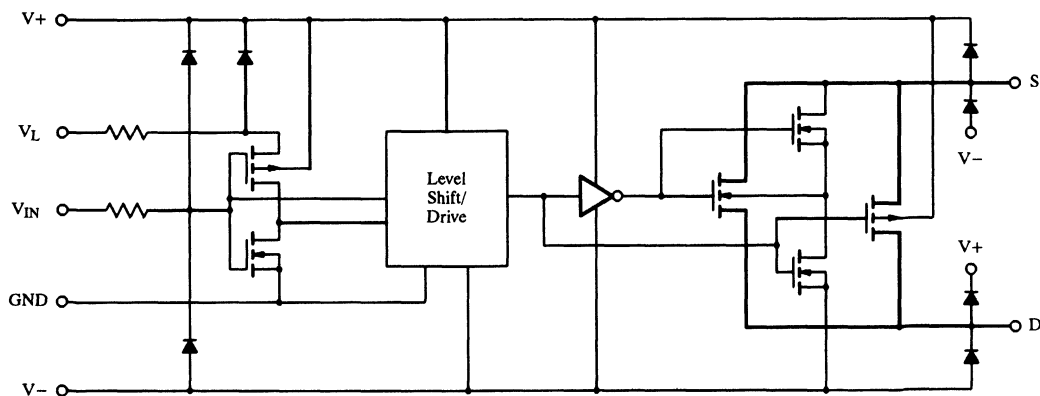
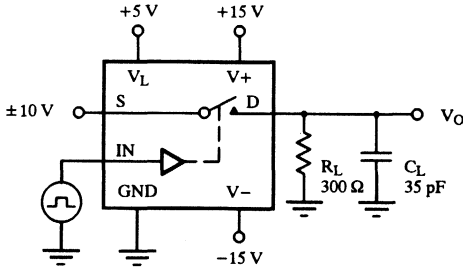


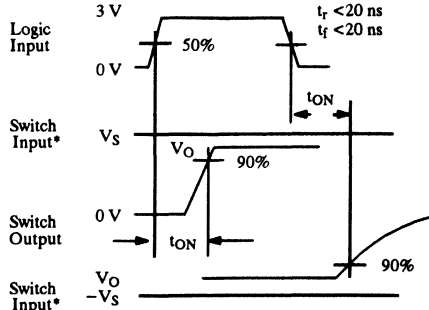
Figure 1.

**Test Circuits**



$C_L$  (includes fixture and stray capacitance)

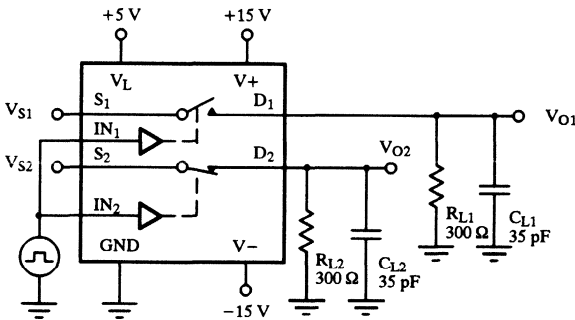
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



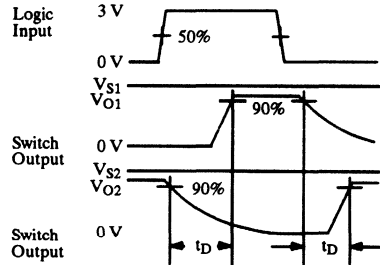
\* $V_S = 10\text{ V}$  for  $t_{ON}$ ,  $V_S = -10\text{ V}$  for  $t_{OFF}$

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

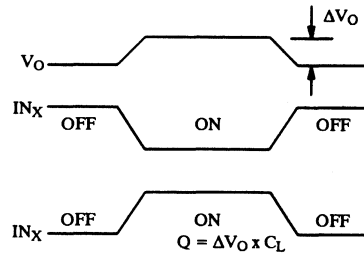
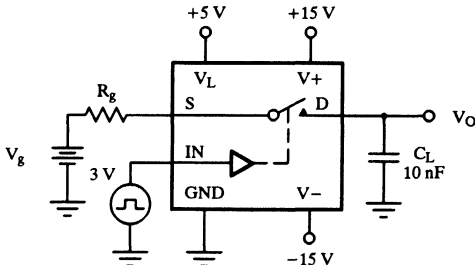
**Figure 2. Switching Time**



$C_L$  (includes fixture and stray capacitance)



**Figure 3. Break-Before-Make (DG413)**



$IN_X$  dependent on switch configuration Input polarity determined by sense of switch.

**Figure 4. Charge Injection**

## Test Circuits (Cont'd)

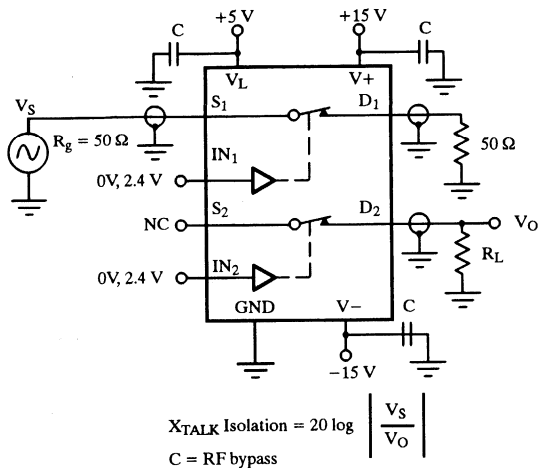


Figure 5. Crosstalk

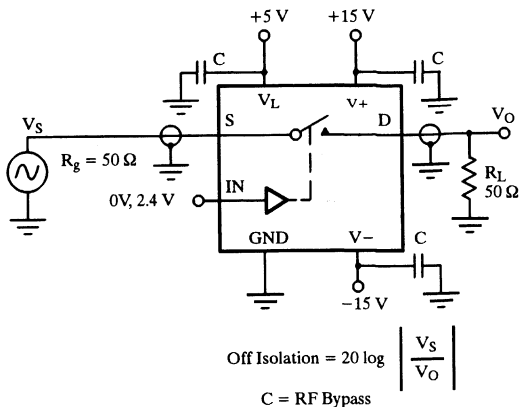


Figure 6. Off Isolation

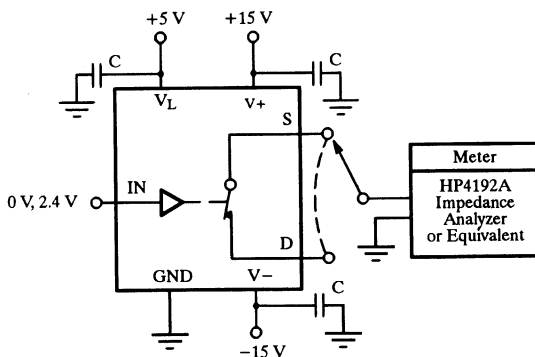


Figure 7. Source/Drain Capacitances

## Applications

### Single Supply Operation:

The DG411/412/413 can be operated with unipolar supplies from 5 V to 44 V. These devices are characterized and tested for unipolar supply operation at 12 V to facilitate the majority of applications. In single supply operation, V+ is

tied to V<sub>L</sub> and V- is tied to 0 V. See Input Switching Threshold vs. Supply Voltage curve for V<sub>L</sub> versus input threshold requirements.



## Applications (Cont'd)

### Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 8, where the inputs to the summing amplifier have some noise filtering, it is necessary to have

shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

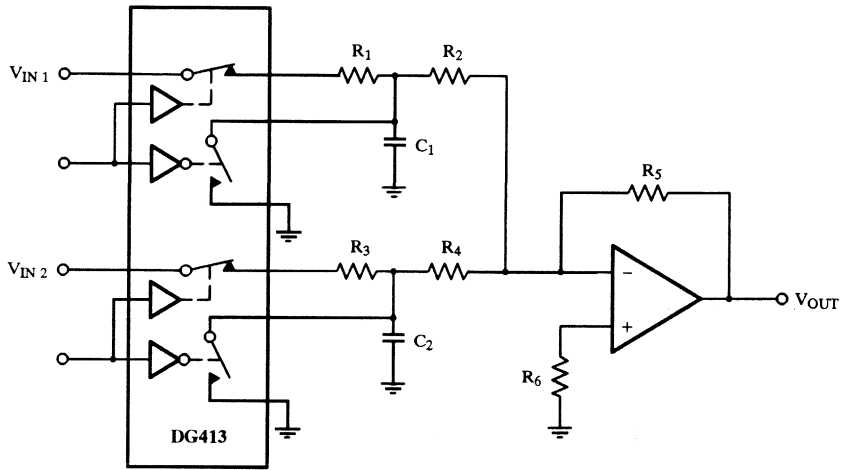


Figure 8. Summing Amplifier

## Precision CMOS Analog Switches

### Features

- $\pm 15\text{-V}$  Analog Signal Range
- On-Resistance— $r_{DS(on)}$ : 20  $\Omega$
- Fast Switching Action— $t_{ON}$ : 100 ns
- Ultra Low Power Requirements— $P_D$ : 35 nW
- TTL and CMOS Compatible
- MiniDIP and SOIC Packaging
- 44-V Supply Max Rating

### Benefits

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing
- Reduced Board Space
- Improved Reliability

### Applications

- Precision Test Equipment
- Precision Instrumentation
- Battery Powered Systems
- Sample-and-Hold Circuits
- Military Radios
- Guidance and Control Systems
- Hard Disk Drives

### Description

The DG417/418/419 monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power, low leakages, high speed, low on-resistance and small physical size, the DG417 series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

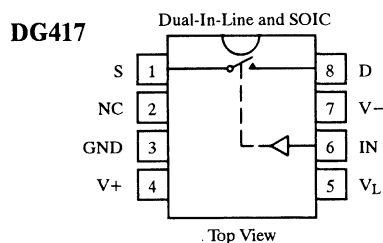
To achieve high-voltage ratings and superior switching performance, the DG417 series is built on Siliconix's high

voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419, which is an SPDT configuration. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG417 and DG418 respond to opposite control logic levels as shown in the Truth Table.

### Functional Block Diagram and Pin Configuration



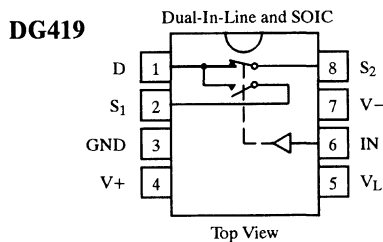
Truth Table — DG417/418

Logic	DG417	DG418
0	ON	OFF
1	OFF	ON

Logic "0" =  $\leq 0.8\text{ V}$ , Logic "1" =  $\geq 2.4\text{ V}$   
Switch Shown for DG417 Logic "1" Input

Ordering Information — DG417/418

Temp Range	Package	Part Number
-40 to 85°C	8-Pin Plastic MiniDIP	DG417DJ
		DG418DJ
	8-Pin Narrow SOIC	DG417DY
		DG418DY
-55 to 125°C	8-Pin CerDIP	DG417AK, DG417AK/883
		DG418AK, DG418AK/883



Truth Table — DG419

Logic	SW <sub>1</sub>	SW <sub>2</sub>
0	ON	OFF
1	OFF	ON

Logic "0" =  $\leq 0.8\text{ V}$ , Logic "1" =  $\geq 2.4\text{ V}$   
Switches Shown for DG419 Logic "1" Input

Ordering Information — DG419

Temp Range	Package	Part Number
-40 to 85°C	8-Pin Plastic MiniDIP	DG419DJ
	8-Pin Narrow SOIC	DG419DY
-55 to 125°C	8-Pin CerDIP	DG419AK, DG419AK/883

## Absolute Maximum Ratings

Voltages Referenced to V-	
V+	44 V
GND	25 V
V <sub>L</sub>	(GND - 0.3 V) to (V+) + 0.3 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>	(V-) - 2 V to (V+) + 2 V or 30 mA, whichever occurs first
Current, (Any Terminal) Continuous	30 mA
Current (S or D) Pulsed 1 ms, 10% duty cycle	100 mA
Storage Temperature (AK Suffix)	-65 to 150°C
(DJ, DY Suffix)	-65 to 125°C

Power Dissipation (Package) <sup>b</sup>	
8-Pin Plastic MiniDIP <sup>c</sup>	400 mW
8-Pin Narrow SOIC <sup>d</sup>	400 mW
8-Pin CerDIP <sup>e</sup>	600 mW

- Notes:
- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads welded or soldered to PC Board.
  - Derate 6 mW/°C above 75°C
  - Derate 6.5 mW/°C above 25°C
  - Derate 12 mW/°C above 75°C

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified  V+ = 15 V, V- = -15 V V <sub>L</sub> = 5 V, V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>		Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
						Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>			Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±12.5 V V+ = 13.5 V, V- = -13.5 V		Room Full	20		35 45		35 45	Ω
Switch Off Leakage Current	I <sub>S(off)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ±15.5 V	DG417	Room Full	-0.1	-0.25 -20	0.25 20	-0.25 -5	0.25 5	nA
	I <sub>D(off)</sub>		DG418	Room Full	-0.1	-0.25 -20	0.25 20	-0.25 -5	0.25 5	
Channel On Leakage Current	I <sub>D(on)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>S</sub> = V <sub>D</sub> = ±15.5 V	DG417	Room Full	-0.4	-0.4 -40	0.4 40	-0.4 -10	0.4 10	nA
			DG418	Room Full	-0.4	-0.4 -40	0.4 40	-0.4 -10	0.4 10	
			DG419	Room Full	-0.4	-0.75 -60	0.75 60	-0.75 -12	0.75 12	
<b>Digital Control</b>										
Input Current, V <sub>IN</sub> Low	I <sub>IL</sub>			Full	0.005	-0.5	0.5	-0.5	0.5	μA
Input Current, V <sub>IN</sub> High	I <sub>IH</sub>			Full	0.005	-0.5	0.5	-0.5	0.5	μA
<b>Dynamic Characteristics</b>										
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S</sub> = ±10 V	DG417 DG418	Room Full	100		175 250		175 250	ns
Turn-Off Time	t <sub>OFF</sub>	See Switching Time Test Circuit	DG417 DG418	Room Full	60		145 210		145 210	
Transition Time	t <sub>TRANS</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S1</sub> = ±10 V, V <sub>S2</sub> = ∓10 V	DG419	Room Full			175 250		175 250	
Break-Before-Make Time Delay	t <sub>D</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S1</sub> = V <sub>S2</sub> = ±10 V	DG419	Room	13	5		5		
Charge Injection	Q	C <sub>L</sub> = 10 nF, V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω		Room	60					pC
Source Off Capacitance	C <sub>S(off)</sub>			Room	8					pF
Drain Off Capacitance	C <sub>D(off)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V	DG417 DG418	Room	8					
Channel On Capacitance	C <sub>D(on)</sub>		DG417 DG418	Room	30					
			DG419	Room	35					

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room Full	0.001		1 5		1 5	$\mu\text{A}$
Negative Supply Current	I-		Room Full	-0.001	-1 -5		-1 -5		
Logic Supply Current	I <sub>L</sub>		Room Full	0.001		1 5		1 5	
Ground Current	I <sub>GND</sub>		Room Full	-0.0001	-1 -5		-1 -5		

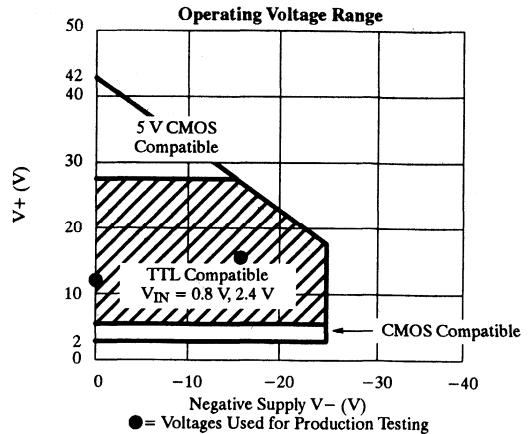
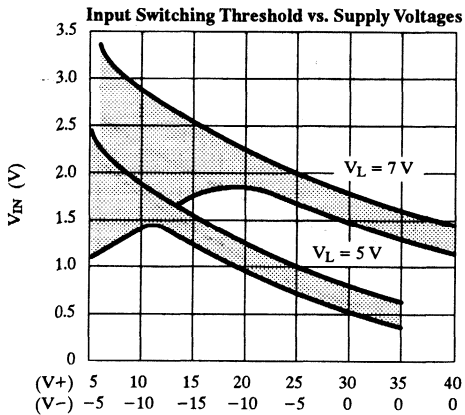
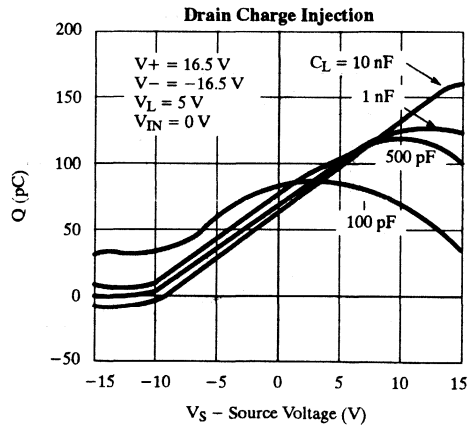
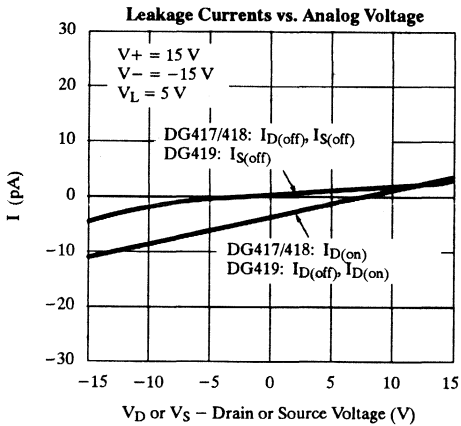
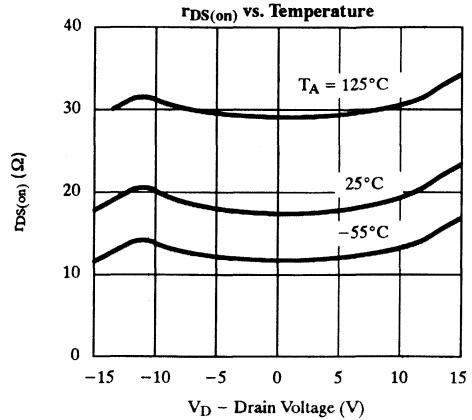
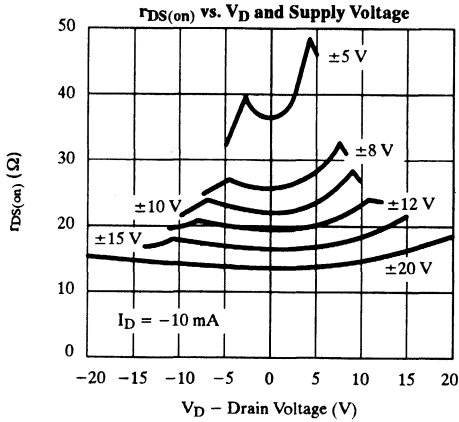
## Specifications<sup>a</sup> for Unipolar Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		0	12	0	12	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = 3.8 V, V <sub>+</sub> = 10.8 V	Room	40					$\Omega$
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 300 $\Omega$ , C <sub>L</sub> = 35 pF, V <sub>S</sub> = 8 V See Switching Time Test Circuit	Room	110					ns
Turn-Off Time	t <sub>OFF</sub>		Room	40					
Break-Before-Make Time Delay	t <sub>D</sub>	R <sub>L</sub> = 300 $\Omega$ , C <sub>L</sub> = 35 pF	DG419	Room	60				
Charge Injection	Q	C <sub>L</sub> = 10 nF, V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 $\Omega$	Room	5					pC
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_+ = 13.2\text{ V}, V_L = 5.25\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room	0.001					$\mu\text{A}$
Negative Supply Current	I-		Room	-0.001					
Logic Supply Current	I <sub>L</sub>		Room	0.001					
Ground Current	I <sub>GND</sub>		Room	-0.001					

### Notes:

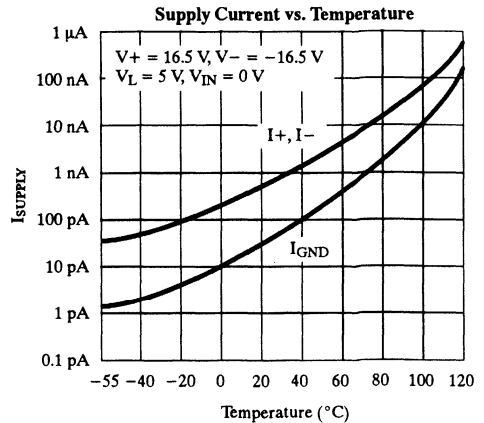
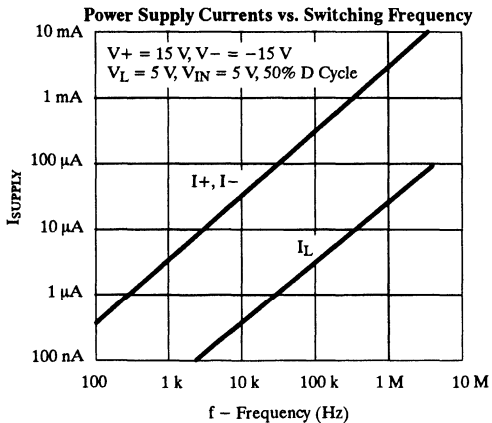
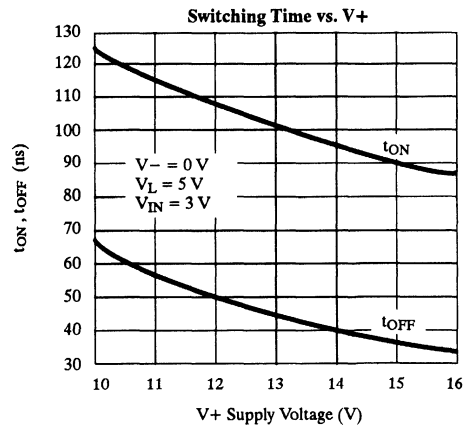
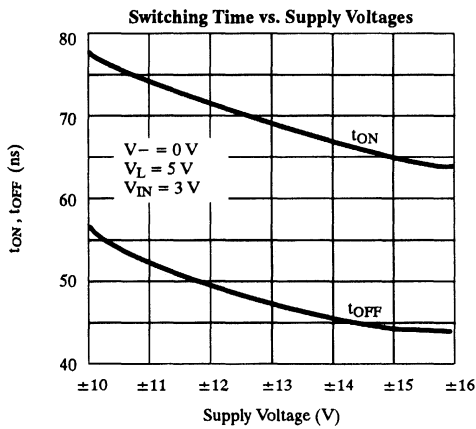
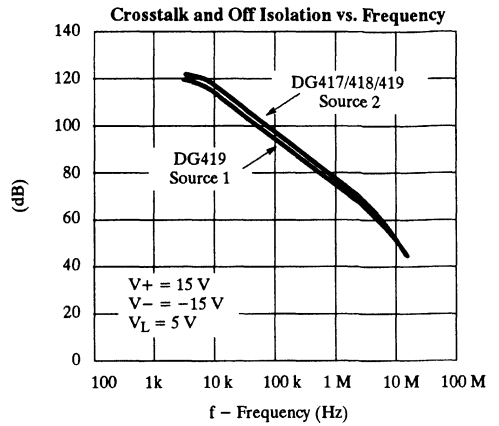
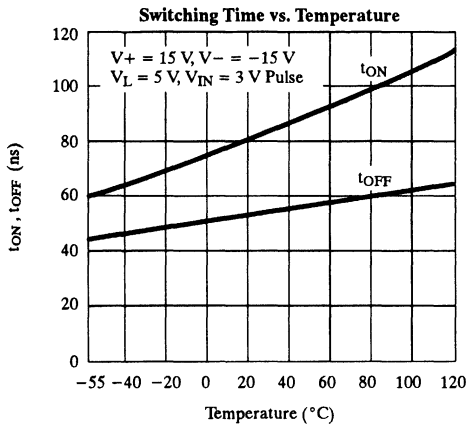
- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

## Typical Characteristics



1

## Typical Characteristics (Cont'd)



**Schematic Diagram (Typical Channel)**

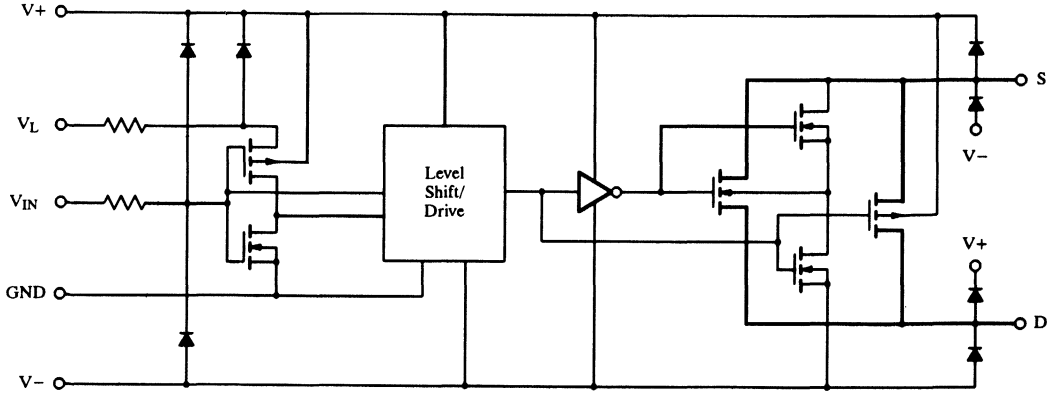
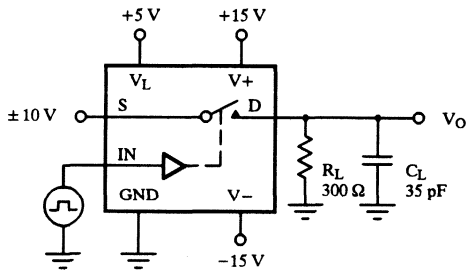


Figure 1.

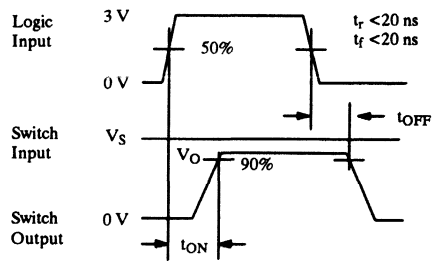
**Test Circuits**

$V_O$  is the steady state output with the switch on.



$C_L$  (includes fixture and stray capacitance)

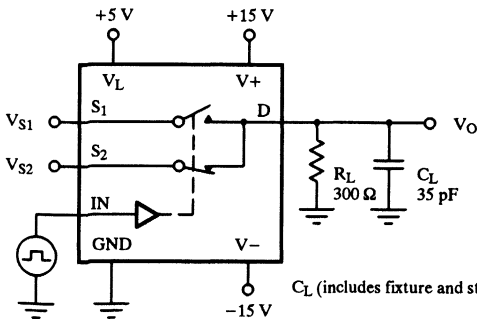
$$V_O = V_S \frac{R_L}{R_L + \tau DS(on)}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 2. Switching Time (DG417/418)

1



$C_L$  (includes fixture and stray capacitance)

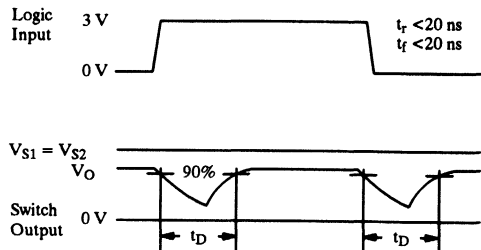
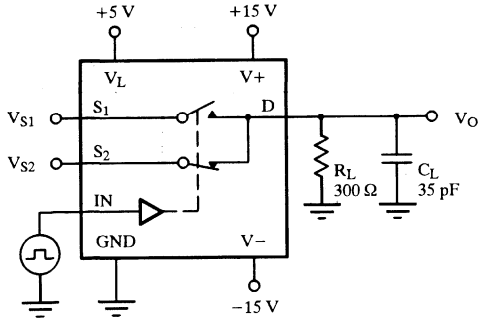


Figure 3. Break-Before-Make (DG419)

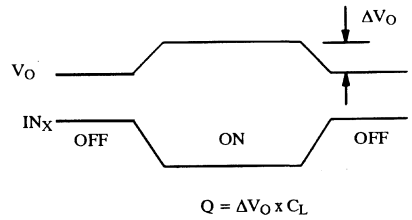
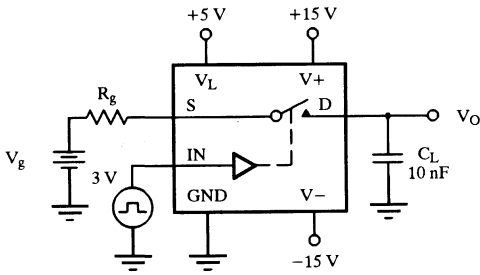
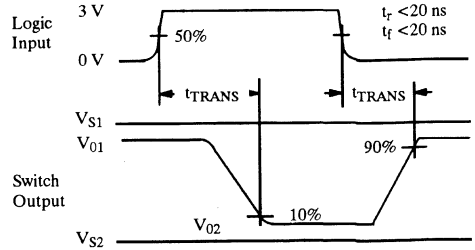
## Test Circuits (Cont'd)



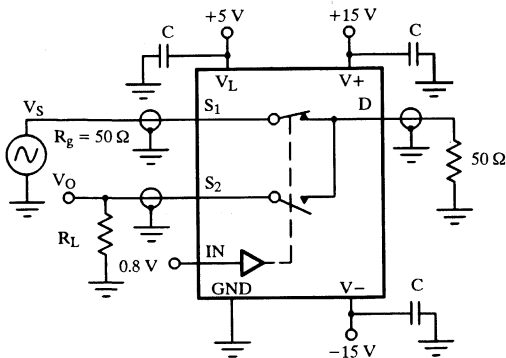
$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + t_{DS(on)}}$$

**Figure 4.** Transition Time (DG419)



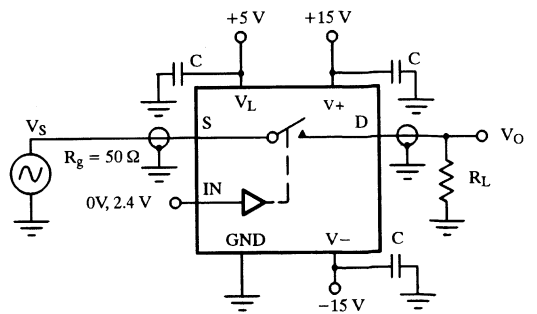
**Figure 5.** Charge Injection



$$X_{TALK} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

$C = \text{RF bypass}$

**Figure 6.** Crosstalk (DG419)

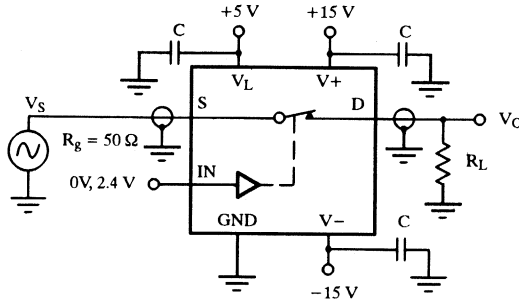


$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

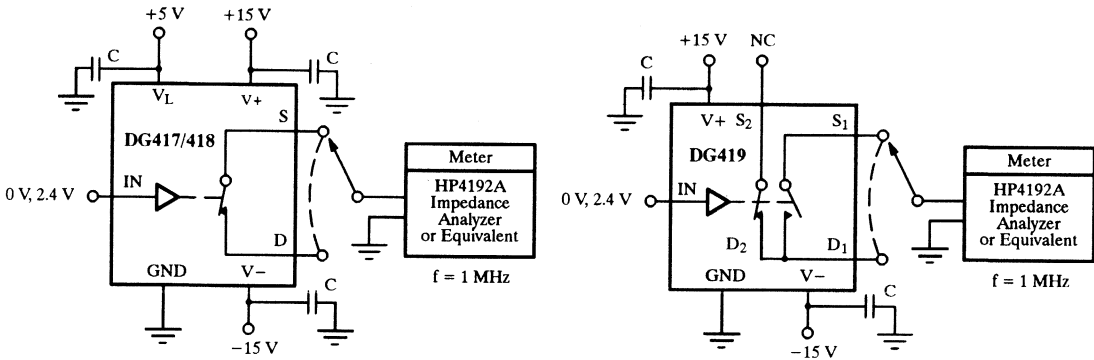
**Figure 7.** Off Isolation



**Test Circuits (Cont'd)**



**Figure 8.** Insertion Loss



**Figure 9.** Source/Drain Capacitances

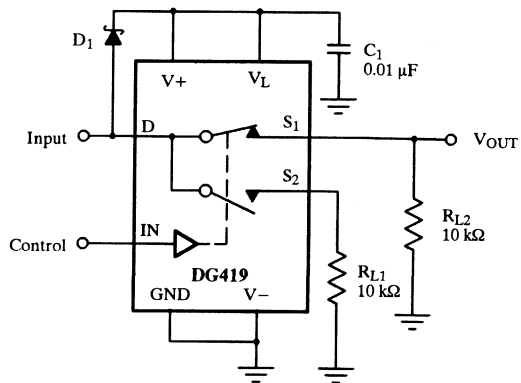
**Applications**

**Switched Signal Powers Analog Switch**

The analog switch in Figure 10 derives power from its input signal, provided the input signal amplitude exceeds 4 V and its frequency exceeds 1 kHz.

This circuit is useful when signals have to be routed to either of two remote loads. Only three conductors are required: one for the signal to be switched, one for the control signal and a common return.

A positive input pulse turns on the clamping diode  $D_1$  and charges  $C_1$ . The charge stored on  $C_1$  is used to power the chip; operation is satisfactory because the switch requires less than  $1 \mu A$  of stand-by supply current. Loading of the signal source is imperceptible. The DG419's on-resistance is a low  $100 \Omega$  for a 5-V input signal.



**Figure 10.** Switched Signal Powers Remote SPDT Analog Switch

## Applications (Cont'd)

### Micropower UPS Transfer Switch

When  $V_{CC}$  drops to 3.3 V, the DG417 changes states, closing  $SW_1$  and connecting the backup cell, as shown in Figure 11.  $D_1$  prevents current from leaking back towards the rest of the circuit. Current consumption by the CMOS analog switch is around 100 pA; this ensures that most of the power available is applied to the memory, where it is

really needed. In the stand-by mode, hundreds of  $\mu A$  are sufficient to retain memory data.

When the 5-V supply comes back up, the resistor divider senses the presence of at least 3.5 V, and causes a new change of state in the analog switch, restoring normal operation.

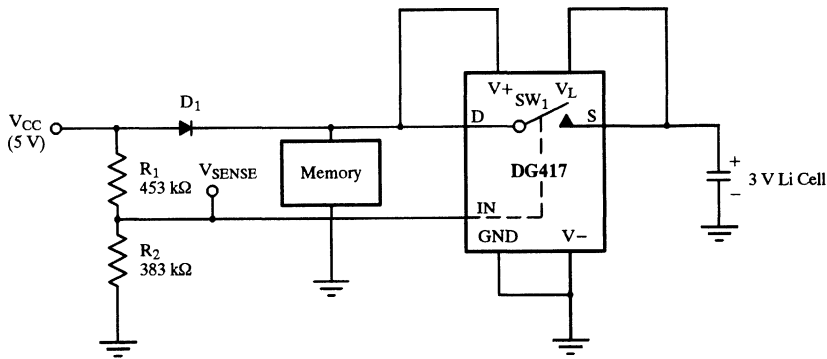


Figure 11. Micropower UPS Circuit

### Programmable Gain Amplifier

The DG419, as shown in Figure 12, allows accurate gain selection in a small package. Switching into virtual ground reduces distortion caused by  $r_{DS(on)}$  variation as a function of analog signal amplitude.

### GaAs FET Driver

The DG419, as shown in Figure 13 may be used as a GaAs FET driver. It translates a TTL control signal into  $-8-V, 0-V$  level outputs to drive the gate.

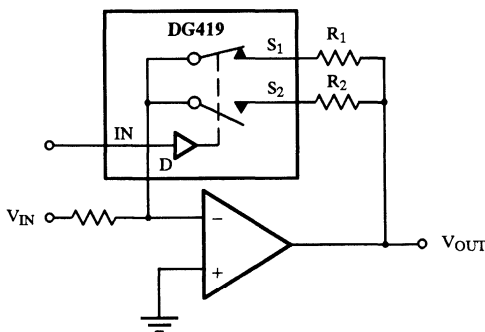


Figure 12. Programmable Gain Amplifier

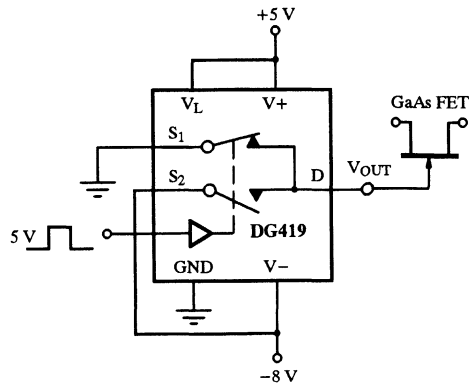


Figure 13. GaAs FET Driver

# Low-Power, High-Speed, Latchable CMOS Analog Switches

## Features

- Latched Control Inputs
- Rail-to-Rail Analog Input Range
- On-Resistance: 25 Ω
- Fast Switching Action— $t_{ON}$ : 170 ns
- Micropower Requirements— $P_D$ : 35 nW
- TTL and CMOS Logic Compatible
- Low Leakage: 40 pA

## Benefits

- $\mu P$  Compatible
- Wide Dynamic Range
- Reduced Component Count
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Battery-Compatible Operation

## Applications

- Data Bus Switching
- Sample-and-Hold Circuits
- Programmable Filters
- $\mu P$  Controlled Analog Systems
- Portable Instruments
- Telecommunication Systems

## Description

The DG421/423/425 are monolithic analog switches featuring latchable logic inputs to simplify interfacing with microprocessors. This series combines fast switching speed ( $t_{ON}$ : 170 ns, typ), and low on-resistance ( $r_{DS(on)}$ : 25 Ω, typ) making it ideally suited for battery powered industrial and military applications that require microprocessor compatible analog switches.

The DG421 has two normally open switches (SPST). The DG423 has two single-pole, double-throw (SPDT) pairs. The DG425 has two normally open pairs (DPST).

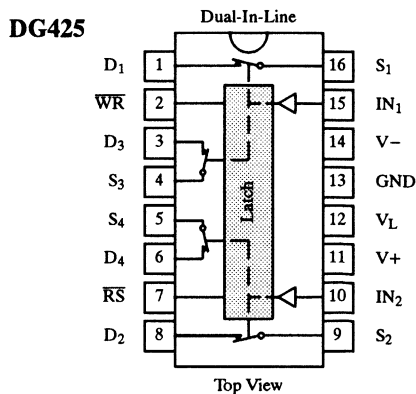
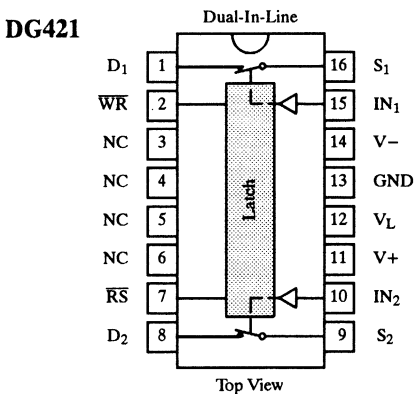
To achieve high-voltage ratings and superior switching

performance, the DG421 series is built on Siliconix's high voltage silicon gate CMOS process. Break-before-make is guaranteed for the DG423. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on and blocks input voltages up to the supply rail voltages when off.

The input data latches become transparent when  $\overline{WR}$  is set low. When  $\overline{WR}$  goes high the latches store the logic control data. A low on  $\overline{RS}$  resets all switches to their default state (all inputs low).

## Functional Block Diagram and Pin Configuration



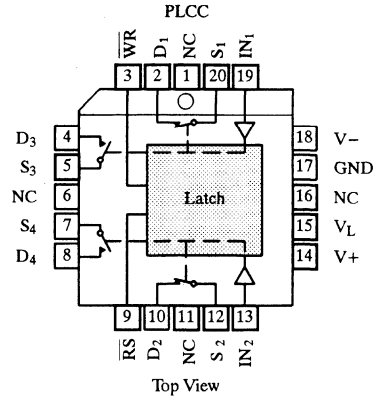
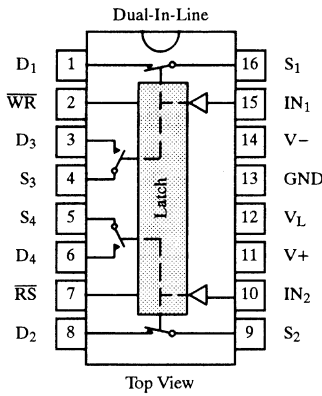
Truth Table – DG421/DG425

$\overline{WR}$	$\overline{RS}$	$IN_x$	Switch
0	1	0	OFF
		1	ON

Logic "0"  $\leq 0.8 V$   
Logic "1"  $\geq 2.4 V$   
Switches Shown for Logic "1" Input

## Functional Block Diagram and Pin Configuration

**DG423**



Truth Table – DG423

WR	RS	IN <sub>X</sub>	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	1	0	OFF	ON
		1	ON	OFF

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

Ordering Information – DG421/423/425

Temp Range	Package	Part Number
-40 to 85°	16-Pin Plastic DIP	DG421DJ
		DG423DJ
		DG425DJ
	20-Pin PLCC	DG423DN

Latch Operation Truth Table

IN <sub>X</sub>	RS	WR	Latch/Switch X
X	1	0	Transparent latch operation
X	1		Control data latched-in, switches on or off as selected by last IN <sub>X</sub>
X	0	X	All latches reset, switches on or off as when IN <sub>X</sub> = 0, WR = 0, RS = 1
X		X	

## Absolute Maximum Ratings

Voltages Referenced to V-

V+	44 V
GND	25 V
V <sub>L</sub>	(GND - 0.3 V) to (V+ + 0.3 V)
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>	V- minus 2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	40 mA
Current, S or D (Pulsed 1 ms, 10% duty)	100 mA
Storage Temperature	-65 to 125°C

Power Dissipation (Package)<sup>b</sup>

16-Pin Plastic DIP <sup>c</sup>	470 mW
20-Pin PLCC <sup>d</sup>	800 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C
- Derate 10 mW/°C above 75°C

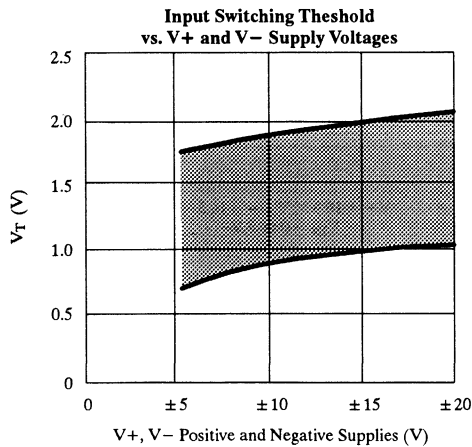
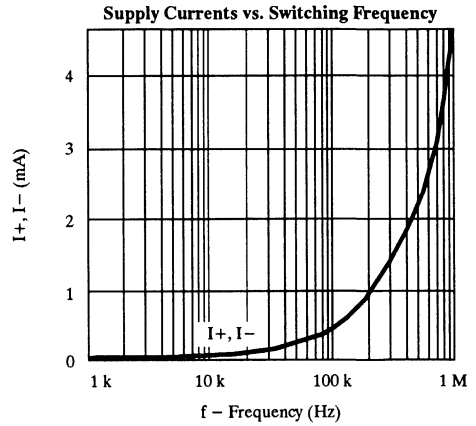
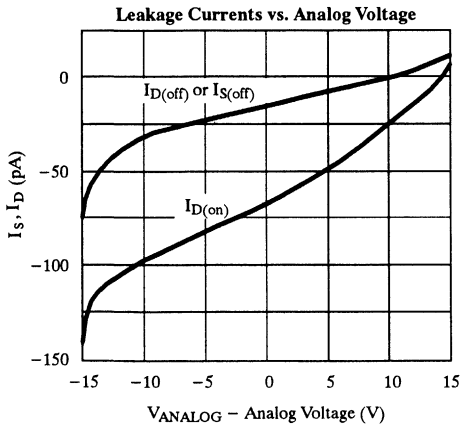
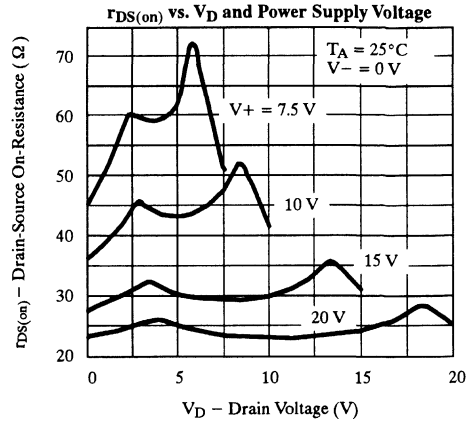
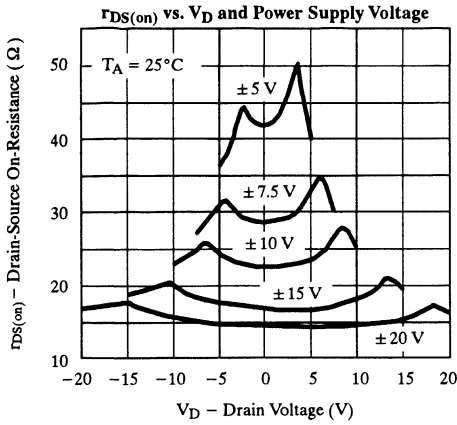
**Specifications**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^e$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$		Full	-15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = \pm 8.5\text{ V}$ $V_+ = 13.5\text{ V}, V_- = -13.5\text{ V}$	Room Full		25	35 45	$\Omega$
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_D = \mp 15.5\text{ V}, V_S = \pm 15.5\text{ V}$	Room Full	-0.25 -5	$\pm 0.01$	0.25 5	nA
	$I_{D(off)}$		Room Full	-0.25 -5	$\pm 0.01$	0.25 5	
Channel On Leakage Current	$I_{D(on)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$	Room Full	-0.4 -10	$\pm 0.04$	0.4 10	
<b>Digital Control</b>							
Input Current with $V_{IN}$ Low	$I_{IL}$	$V_{IN}$ under test = 0.8 V, all other = 2.4 V	Full	-0.5	0.005	0.5	$\mu\text{A}$
Input Current with $V_{IN}$ High	$I_{IH}$	$V_{IN}$ under test = 2.4 V, all other = 0.8 V	Full	-0.5	0.005	0.5	
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ See Figure 2	Room Full		170	250 300	ns
Turn-Off Time	$t_{OFF}$		Room Full		140	200 200	
Latch Timing	$t_{WW}$	$R_I = 300\ \Omega, C_I = 35\text{ pF}$ $V_S = \pm 10\text{ V}$	Room Full	200 200			
	$t_{DW}$		Room Full	100 100			
	$t_{WD}$		Room Full	60 100			
Break-Before-Make Time Delay	$t_D$	DG423 Only, $R_L = 300\ \Omega, C_L = 35\text{ pF}$ , See Figure 3	Room	5	25		
Charge Injection <sup>d</sup>	Q	$C_L = 10\text{ nF}, V_{gen} = 0\text{ V}, R_{gen} = 0\ \Omega$ , See Figure 4	Room		60		pC
Off Isolation Reject Ratio	OIRR	$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room		65		dB
Crosstalk (Channel-to-Channel)	$X_{TALK}$	Between Any Two Channels $R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room		76		
Source Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}$	Full		9		pF
Drain Off Capacitance	$C_{D(off)}$		Full		9		
Channel On Capacitance	$C_{D(on)}$		Full		35		
<b>Power Supply</b>							
Positive Supply Current	$I_+$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room Full		0.0001	1 5	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Full	-1 -5	-0.0001		
Logic Supply Current	$I_L$		Room Full		0.0001	1 5	
Ground Current	$I_{GND}$		Room Full	-1 -5	-0.0001		

Notes:

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

## Typical Characteristics



**Schematic Diagram (Typical Channel)**

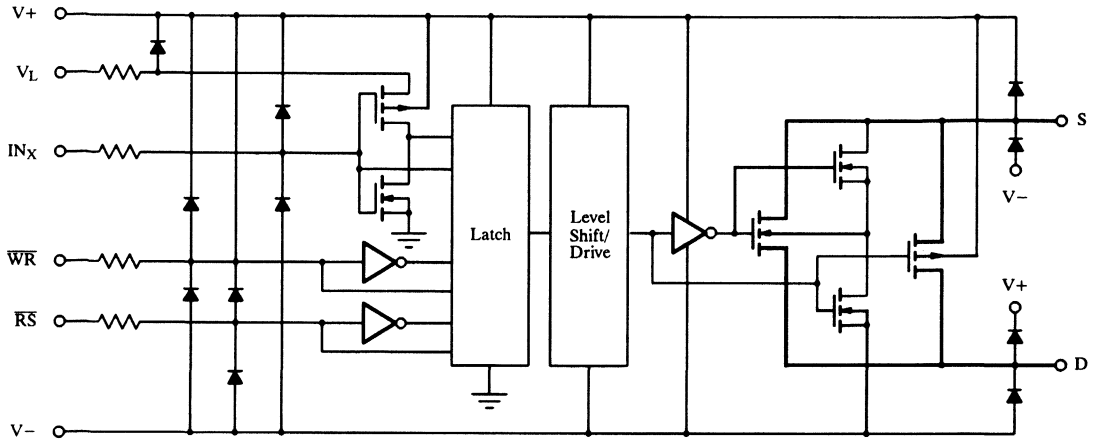
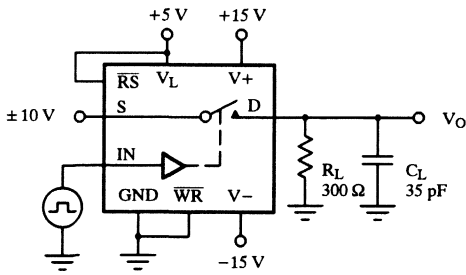


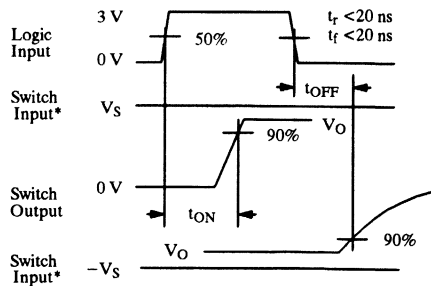
Figure 1.

**Test Circuits**



$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



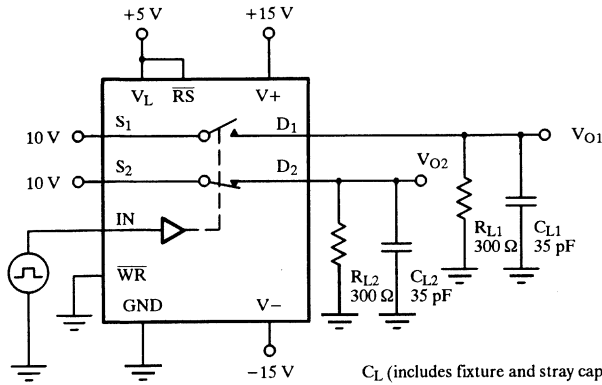
\* $V_S = 10$  V for  $t_{ON}$ ,  $V_S = -10$  V for  $t_{OFF}$

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

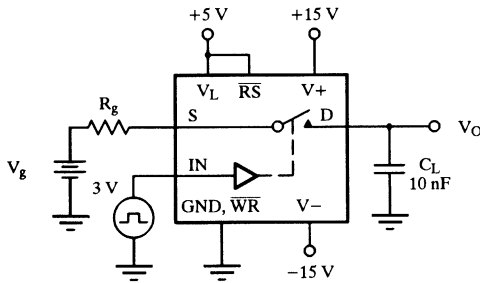
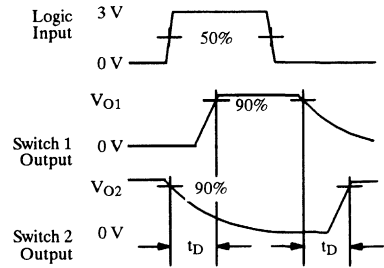
**1**

Figure 2. Switching Time

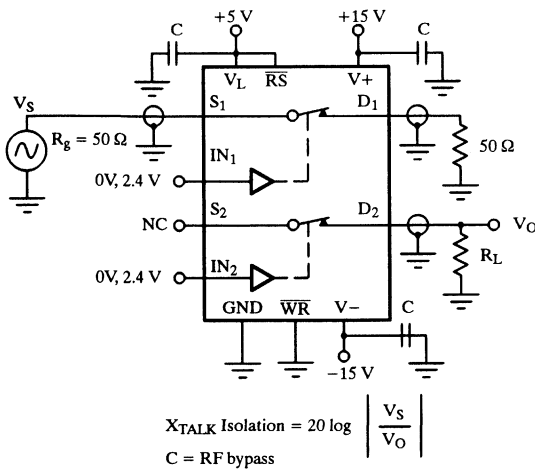
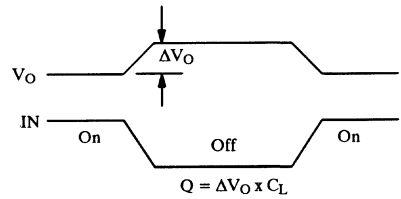
## Test Circuits (Cont'd)



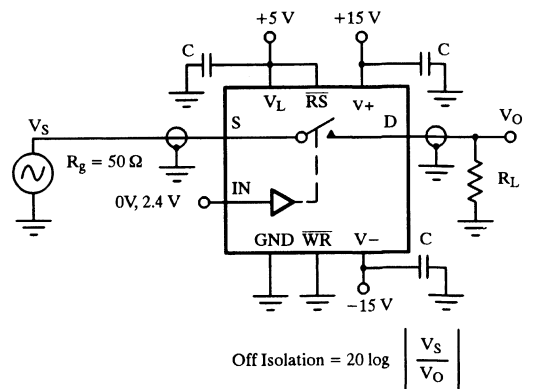
**Figure 3.** Break-Before-Make



**Figure 4.** Charge Injection



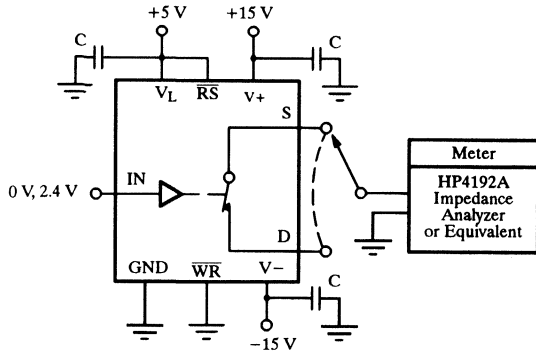
**Figure 5.** Crosstalk



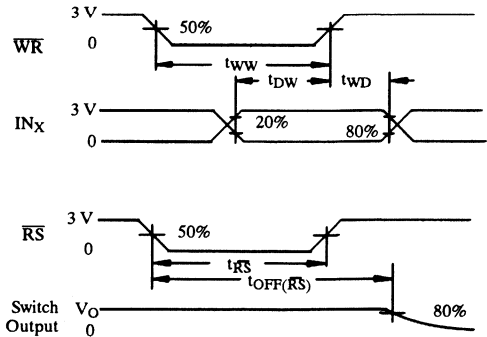
**Figure 6.** Off Isolation



**Test Circuits (Cont'd)**



**Figure 7.** Source/Drain Capacitances

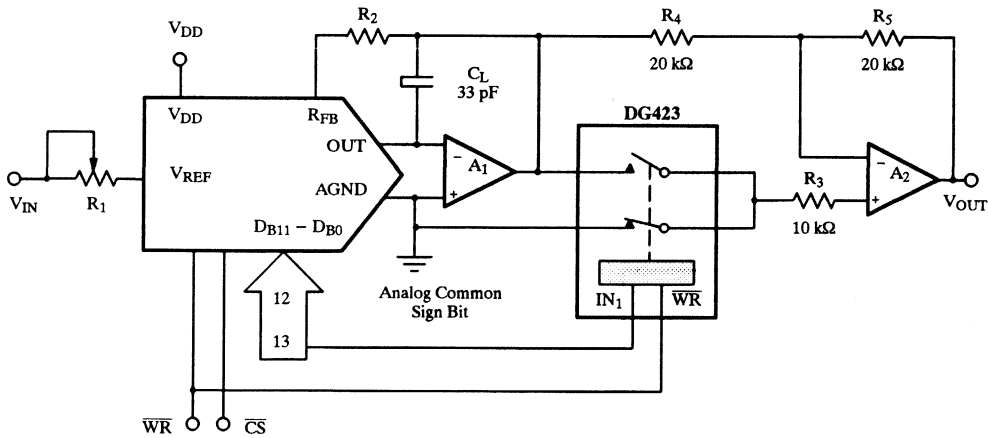


**Figure 8.** Latch Timing

**Applications**

Figure 9 shows a circuit configured to increase the effective resolution of the 12-bit DAC to 13 bits. The circuit operates

with a sign plus magnitude code. A sign bit of "0" connects R<sub>3</sub> to GND, giving 12-bit resolution per quadrant.



**12-Bit Plus Sign Magnitude Code Table**

Sign Bit	Digital Input			Analog Output (V <sub>OUT</sub> )
	MSB	LSB	LSB	
0	1111	1111	1111	$+(4095/4096)V_{IN}$
0	0000	0000	0000	0 Volts
1	0000	0000	0000	0 Volts
1	1111	1111	1111	$+(4095/4096)V_{IN}$

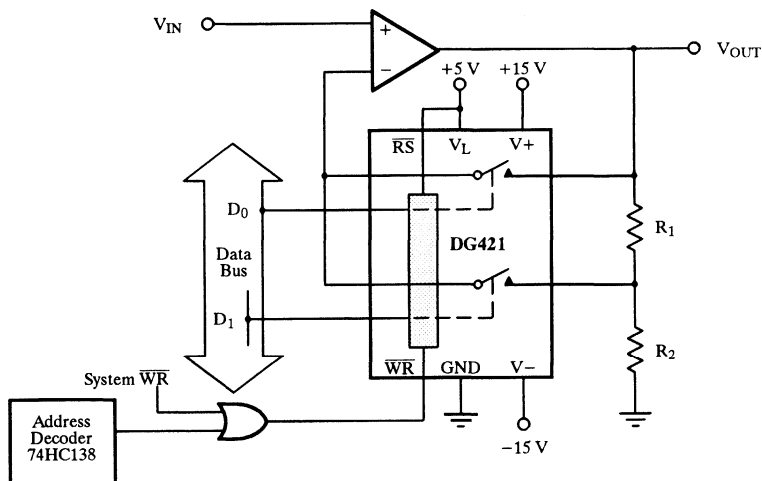
**Figure 9.** 12-Bit Plus Sign Magnitude D/A Converter

## Applications

When switch  $S_1$  of Figure 10 is closed, the op amp is placed in the familiar unity-gain non-inverting configuration. When switch  $S_2$  is closed and  $S_1$  is open the gain is given by:

$$A_V = 1 + \frac{R_1}{R_2}$$

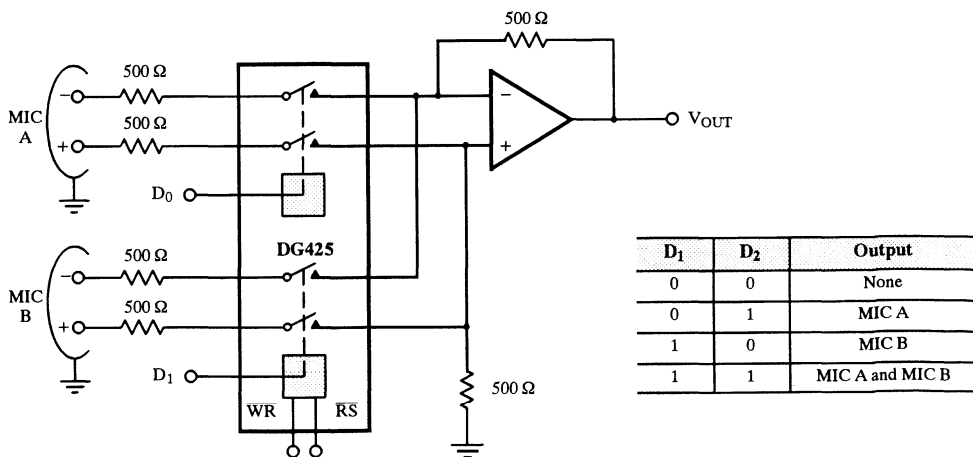
The microprocessor system  $\overline{WR}$  must gate the decoder output to ensure proper timing.



**Figure 10.** Bus-Controlled Precision Gain-Ranging Circuit

Figure 11 shows a balanced-line microphone input stage that provides selection or summing between two balanced-line microphones and also performs differential-to-single-ended conversion. Either MIC A or MIC B can be selected, and neither and/or both may be

summed at the output. This configuration uses “virtual ground” switching, a method which minimizes distortion resulting from the analog switch on-resistance modulation. The actual voltage swings experienced by the analog switch barely exceed 1 V for a 15-V full-scale range input.



**Figure 11.** Bus-Controlled Selector for Balanced-Line Microphones



## Ordering Information and Truth Table

Ordering Information		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG441DJ
		DG442DJ
	16-Pin Narrow SOIC	DG441DY
		DG442DY
-55 to 125°C	16-Pin CerDIP	DG441AK
		DG441AK/883
		5962-9204101MEA
		DG442AK
		DG442AK/883
		5962-9204102MEA
	LCC-20	5962-9204101M2A
		5962-9204102M2A

Truth Table		
Logic	DG441	DG442
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V  
Switches Shown for DG441 Logic "1" Input

## Absolute Maximum Ratings

V+ to V-	44 V
GND to V-	25 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle)	100 mA
Storage Temperature (AK Suffix)	-65 to 150°C
(DJ, DY Suffix)	-65 to 125°C
Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	450 mW
16-Pin CerDIP <sup>d</sup>	900 mW
16-Pin Narrow Body SOIC <sup>d</sup>	900 mW
LCC-20 <sup>d</sup>	1200 mW

### Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C
- Derate 12 mW/°C above 25°C

## Specifications<sup>a</sup> for Dual Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>†</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
					<b>Analog Switch</b>				
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±8.5 V V+ = 13.5 V, V- = -13.5 V	Room Full	50		85 100		85 100	Ω
Switch Off Leakage Current	I <sub>S(off)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ∓15.5 V	Room Full	±0.01	-0.5 -20	0.5 20	-0.5 -5	0.5 5	nA
	I <sub>D(off)</sub>		Room Full	±0.01	-0.5 -20	0.5 20	-0.5 -5	0.5 5	
Channel On Leakage Current	I <sub>D(on)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>S</sub> = V <sub>D</sub> = ±15.5 V	Room Full	±0.08	-0.5 -40	0.5 40	-0.5 -10	0.5 10	

**Specifications<sup>a</sup> for Dual Supplies (Cont'd)**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Digital Control</b>									
Input Current $V_{IN}$ Low	$I_{IL}$	$V_{IN}$ under test = 0.8 V All Other = 2.4 V	Full	-0.01	-500	500	-500	500	nA
Input Current $V_{IN}$ High	$I_{IH}$	$V_{IN}$ under test = 2.4 V All Other = 0.8 V	Full	0.01	-500	500	-500	500	
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$ , See Figure 2	Room	150		250		250	ns
Turn-Off Time	DG441 $t_{OFF}$		Room	90		120		120	
	DG442 $t_{OFF}$		Room	110		210		210	
Charge Injection <sup>e</sup>	Q	$C_L = 1\text{ nF}, V_S = 0\text{ V}$ $V_{gen} = 0\text{ V}, R_{gen} = 0\text{ }\Omega$	Room	-1					pC
Off Isolation <sup>e</sup>	OIRR	$R_L = 50\text{ }\Omega, C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	Room	60					dB
Crosstalk <sup>e</sup> (Channel-to-Channel)	X <sub>TALK</sub>		Room	100					
Source Off Capacitance <sup>e</sup>	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	4					pF
Drain Off Capacitance <sup>e</sup>	$C_{D(off)}$		Room	4					
Channel On Capacitance <sup>e</sup>	$C_{D(on)}$		$V_{ANALOG} = 0\text{ V}$	Room	16				
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Full	15		100		100	$\mu\text{A}$
Negative Supply Current	$I_-$		Room	-0.0001	-1		-1		
			Full		-5		-5		
Ground Current	$I_{GND}$	Full	-15	-100		-100			

**Specifications<sup>a</sup> for Single Supply**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = 3\text{ V}, 8\text{ V}$ $V_+ = 10.8\text{ V}$	Room Full	100		160 200		160 200	$\Omega$
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ $V_S = 8\text{ V}$ , See Figure 2	Room	300		450		450	ns
Turn-Off Time	$t_{OFF}$		Room	60		200		200	
Charge Injection	Q	$C_L = 1\text{ nF}$ $V_{gen} = 6\text{ V}, R_{gen} = 0\text{ }\Omega$	Room	2					pC

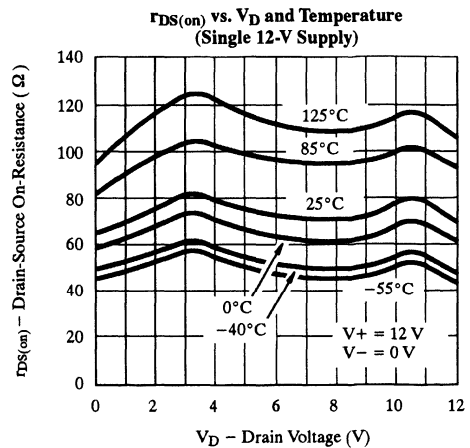
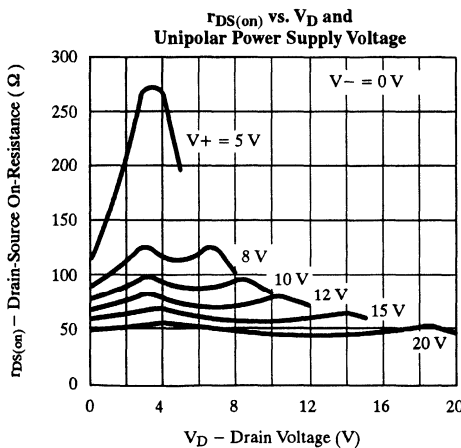
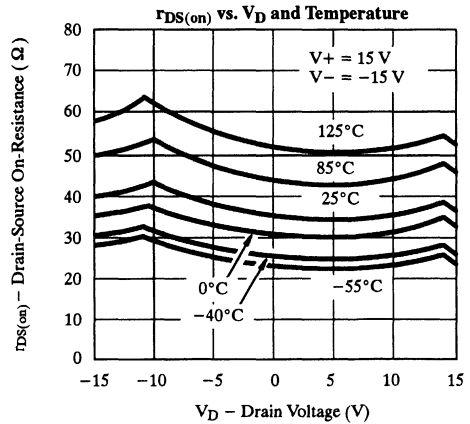
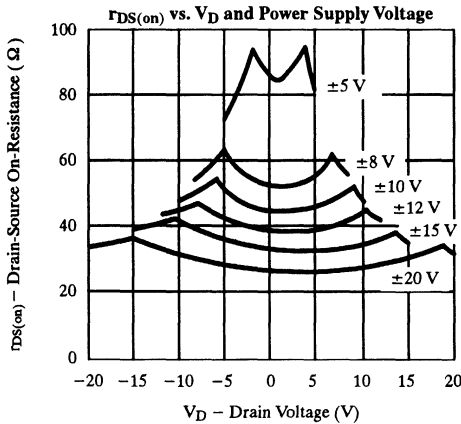
## Specifications<sup>a</sup> for Single Supply<sup>a</sup> (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Full	15		100		100	μA
Negative Supply Current	I-		Room Full	-0.0001	-1	-100	-1	-100	
Ground Current	I <sub>GND</sub>		Full	-15	-100		-100		

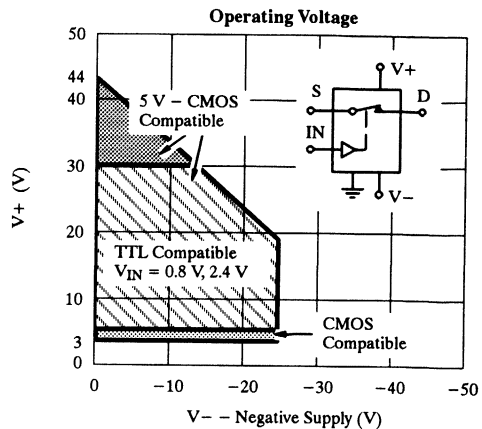
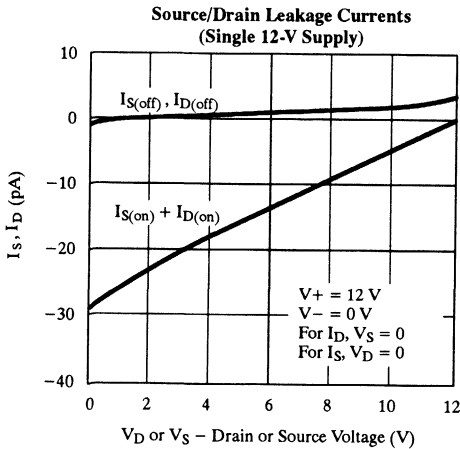
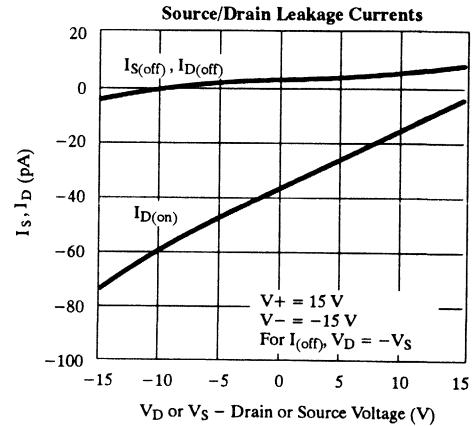
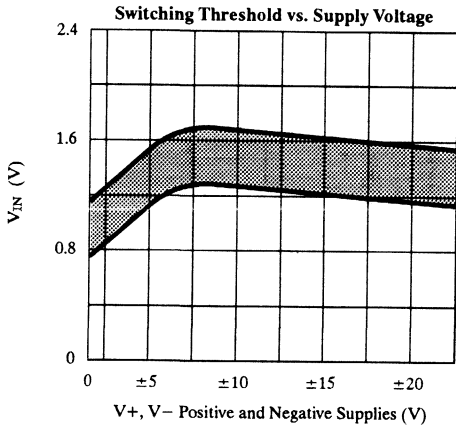
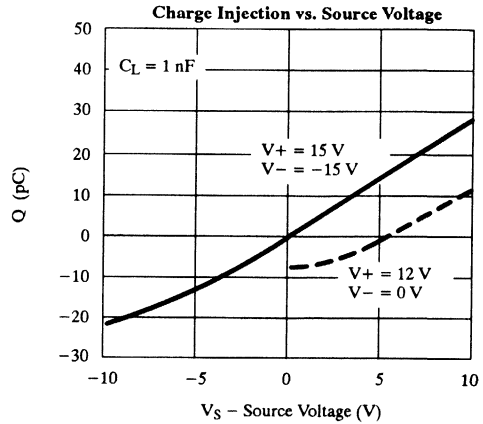
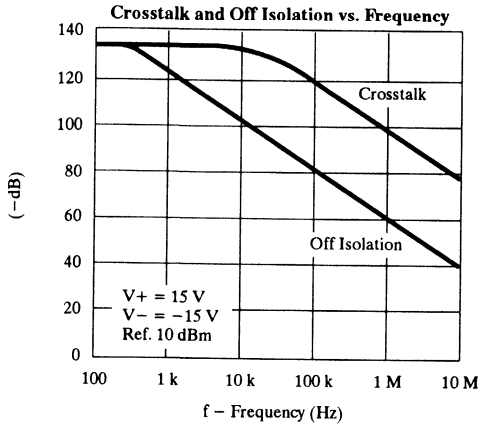
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

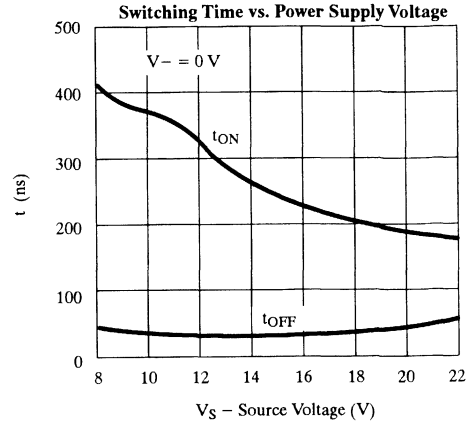
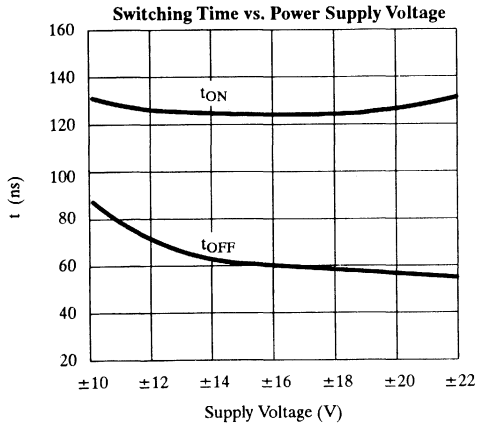
## Typical Characteristics



**Typical Characteristics (Cont'd)**



## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

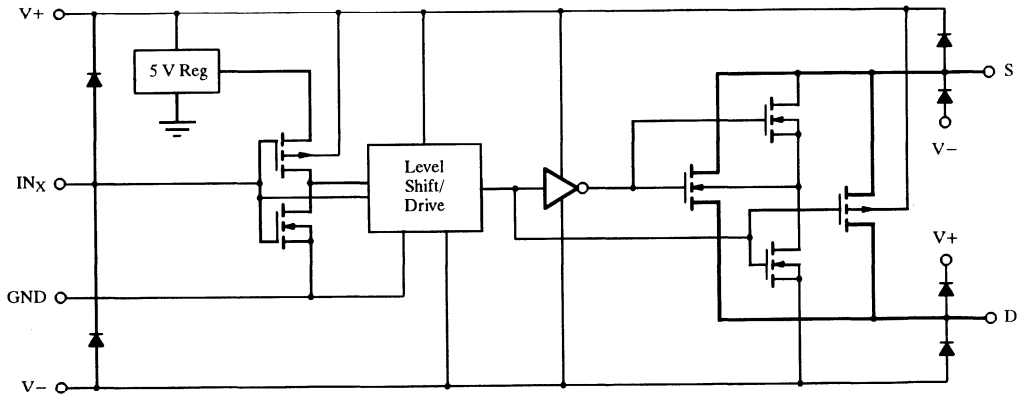
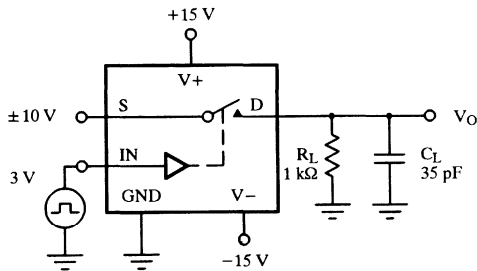
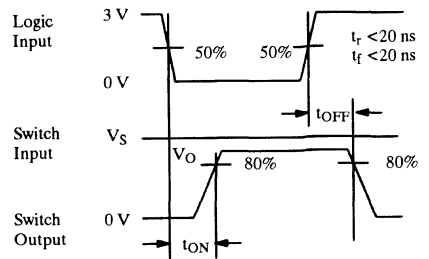


Figure 1.

## Test Circuits



$C_L$  (includes fixture and stray capacitance)

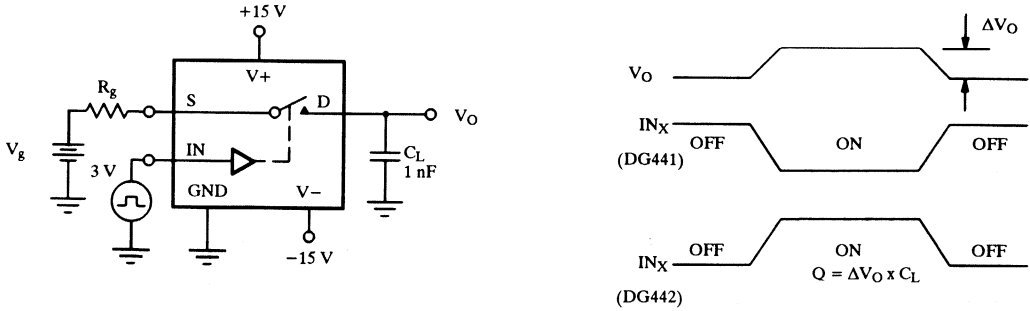


Note: Logic input waveform is inverted for DG442.

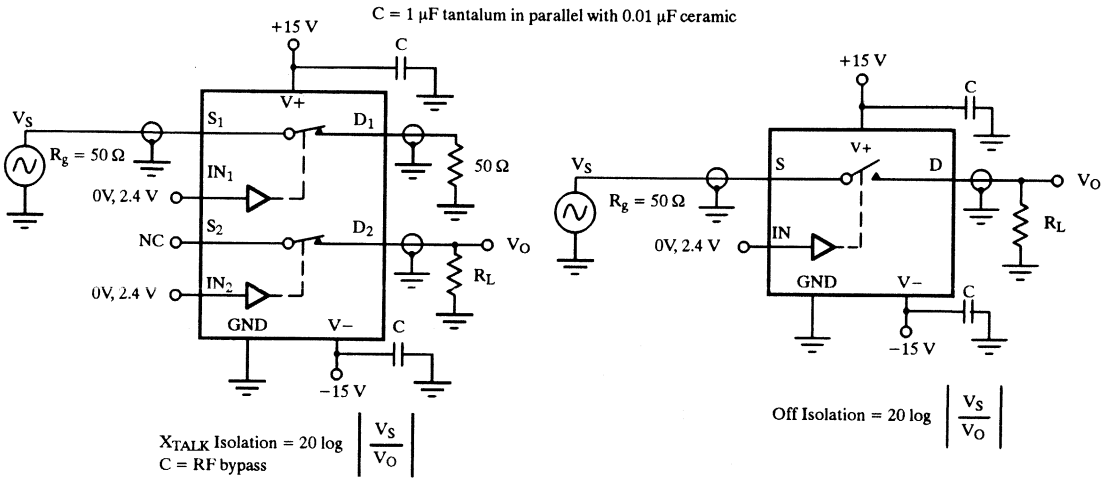
Figure 2. Switching Time



**Test Circuits (Cont'd)**

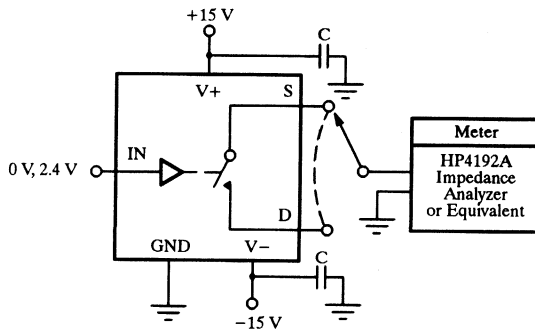


**Figure 3.** Charge Injection



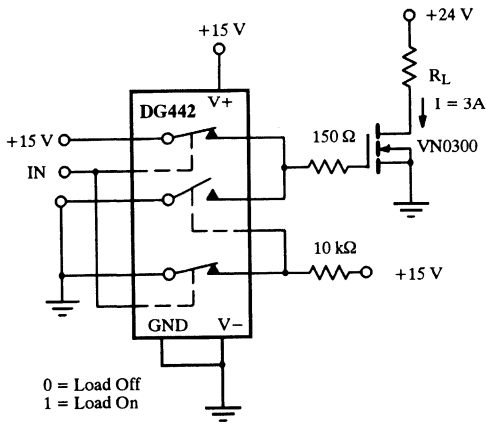
**Figure 4.** Crosstalk

**Figure 5.** Off Isolation

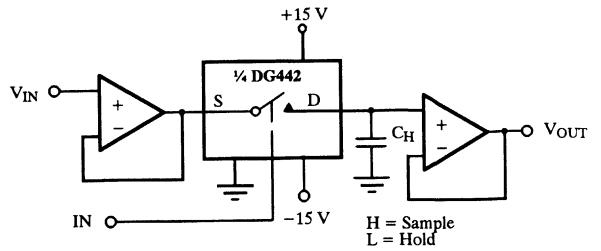


**Figure 6.** Source/Drain Capacitances

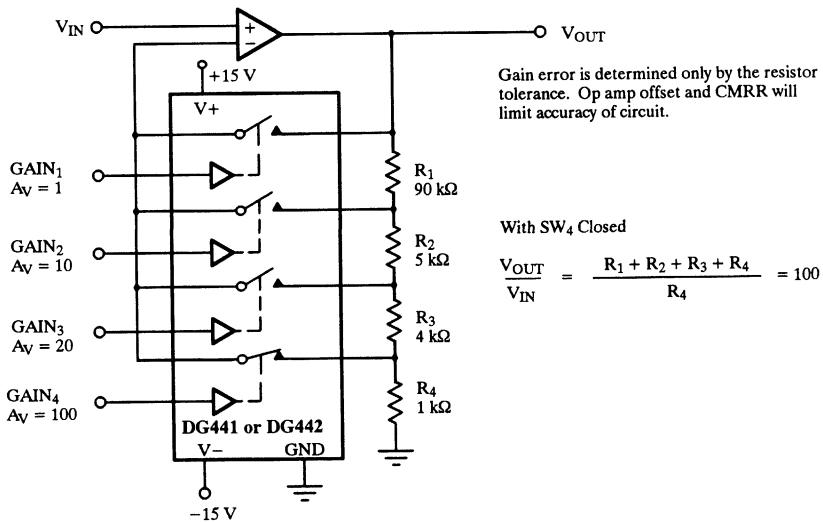
## Applications



**Figure 7.** Power MOSFET Driver



**Figure 8.** Open Loop Sample-and-Hold



**Figure 9.** Precision-Weighted Resistor Programmable-Gain Amplifier

## Quad SPST CMOS Analog Switches

### Features

- Low On-Resistance: 50  $\Omega$
- Low Leakage: 80 pA
- Low Power Consumption: 22 nW
- Fast Switching Action— $t_{ON}$ : 120 ns
- Low Charge Injection
- DG211/DG212 Upgrades
- TTL/CMOS Logic Compatible

### Benefits

- Low Signal Errors and Distortion
- Reduced Power Supply Requirements
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Errors
- Simple Interfacing

### Applications

- Audio Switching
- Battery Powered Systems
- Data Acquisition
- Sample-and-Hold Circuits
- Telecommunication Systems
- Automatic Test Equipment
- Single Supply Circuits
- Hard Disk Drives

### Description

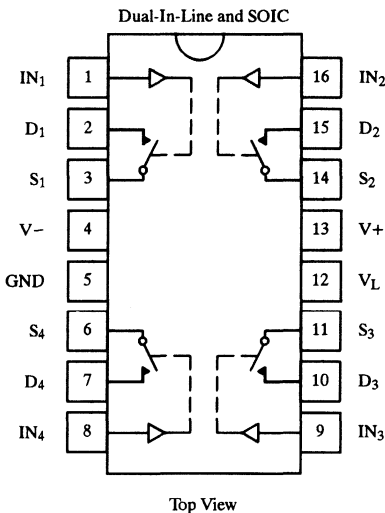
The DG444/DG445 monolithic quad analog switches are designed to provide high speed, low error switching of analog signals. The DG444 has a normally closed function. The DG445 has a normally open function. Combining low power (22 nW, typ) with high speed ( $t_{ON}$ : 120 ns, typ), the DG444/DG445 are ideally suited for upgrading DG211/212 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high-voltage ratings and superior switching performance, the DG444/DG445 are built on Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply levels when off.

### Functional Block Diagram and Pin Configuration

#### DG444



Truth Table

Logic	DG444	DG445
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq$  0.8 V, Logic "1"  $\geq$  2.4 V

Switches Shown for DG444 Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
-40°C to 85°C	16-Pin Plastic DIP	DG444DJ
		DG445DJ
	16-Pin Narrow SOIC	DG444DY
		DG445DY

## Absolute Maximum Ratings

V+ to V-	44 V
GND to V-	25 V
V <sub>L</sub>	(GND - 0.3 V) to (V+) + 0.3 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>	(V-) - 2 V to (V+) + 2 V or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle)	100 mA
Storage Temperature	-65 to 125°C

Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	450 mW
16-Pin Narrow Body SOIC <sup>d</sup>	600 mW

**Notes:**

- Signals on S<sub>X</sub>, D<sub>X</sub>, or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C.
- Derate 12 mW/°C above 75°C.

## Specifications for Dual Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified  V+ = 15 V, V- = -15 V V <sub>L</sub> = 5 V, V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit		
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>			
<b>Analog Switch</b>									
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	-15		15	V		
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±8.5 V V+ = 13.5 V, V- = -13.5 V	Room Full		50	85 100	Ω		
Switch Off Leakage Current	I <sub>S(off)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ∓15.5 V	Room Full	-0.5 -5	±0.01	0.5 5	nA		
	I <sub>D(off)</sub>		Room Full	-0.5 -5	±0.01	0.5 5			
Channel On Leakage Current	I <sub>D(on)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>S</sub> = V <sub>D</sub> = ±15.5 V	Room Full	-0.5 -10	±0.08	0.5 10			
<b>Digital Control</b>									
Input Current V <sub>IN</sub> Low	I <sub>IL</sub>	V <sub>IN</sub> under test = 0.8 V All Other = 2.4 V	Full	-500	-0.01	500	nA		
Input Current V <sub>IN</sub> High	I <sub>IH</sub>	V <sub>IN</sub> under test = 2.4 V All Other = 0.8 V	Full	-500	0.01	500			
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF V <sub>S</sub> = ±10 V, See Figure 2	Room			120	250	ns	
Turn-Off Time	t <sub>OFF</sub>		DG441	Room			110		140
			DG442	Room			160		210
Charge Injection <sup>e</sup>	Q	C <sub>L</sub> = 1 nF, V <sub>S</sub> = 0 V V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	Room		-1		pC		
Off Isolation <sup>e</sup>	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz	Room			60		dB	
Crosstalk (Channel-to-Channel) <sup>d</sup>	X <sub>TALK</sub>		Room			100			
Source Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz	Room			4		pF	
Drain Off Capacitance	C <sub>D(off)</sub>		Room			4			
Channel On Capacitance	C <sub>D(on)</sub>		V <sub>ANALOG</sub> = 0 V	Room			16		

**Specifications for Dual Supplies (Cont'd)**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^e$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Power Supplies</b>							
Positive Supply Current	I+	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room Full		0.001	1 5	$\mu\text{A}$
Negative Supply Current	I-		Room Full	-1 -5	-0.0001		
Logic Supply Current	I <sub>L</sub>		Room Full		0.001	1 5	
Ground Current	I <sub>GND</sub>		Room Full	-1 -5	-0.001		

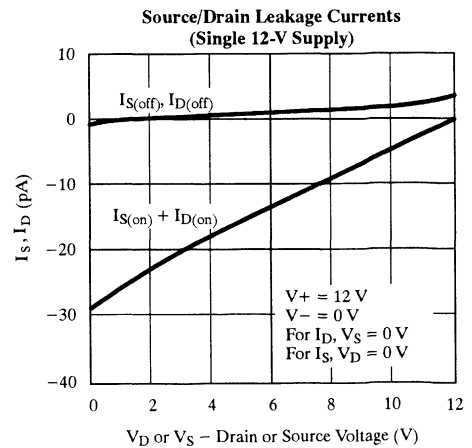
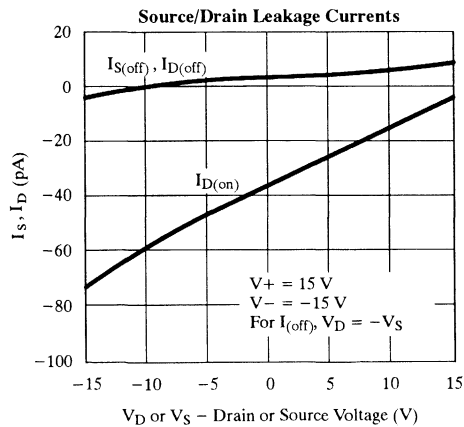
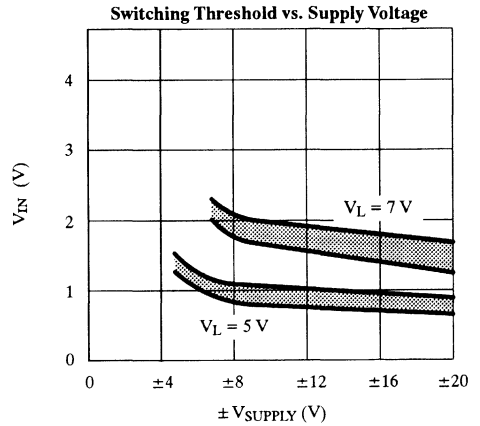
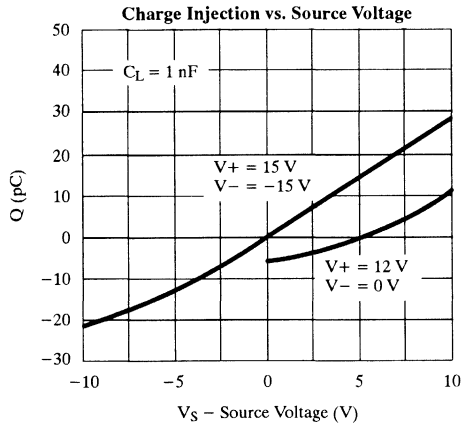
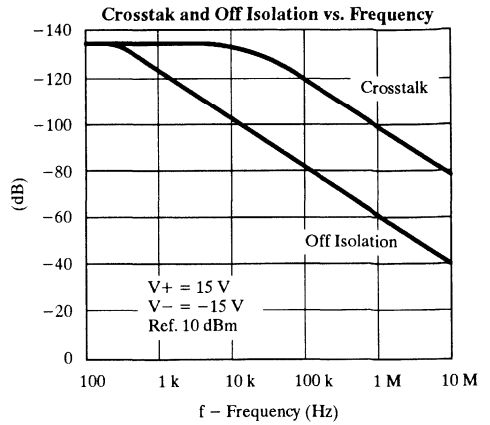
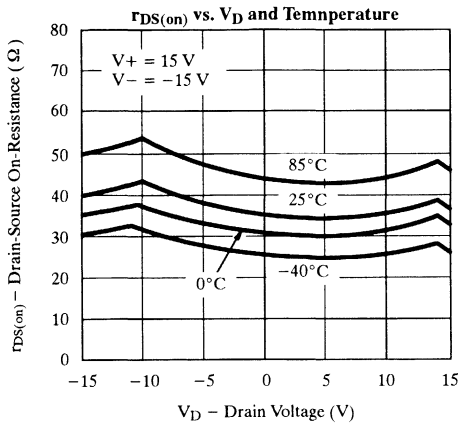
**Specifications for Unipolar Supplies**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^e$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	0		12	V
Drain-Source On-Resistance <sup>d</sup>	r <sub>DS(on)</sub>	$I_S = -10\text{ mA}, V_D = 3\text{ V}, 8\text{ V}$ $V_+ = 10.8\text{ V}, V_L = 5.25\text{ V}$	Room Full		100	160 200	$\Omega$
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}, V_S = 8\text{ V}$ See Figure 2	Room		300	450	ns
Turn-Off Time	t <sub>OFF</sub>		Room		60	200	
Charge Injection	Q	$C_L = 1\text{ nF}, V_{gen} = 6\text{ V}, R_{gen} = 0\ \Omega$	Room		2		pC
<b>Power Supplies</b>							
Positive Supply Current	I+	$V_+ = 13.2\text{ V}, V_{IN} = 0\text{ or }5\text{ V}$	Room Full		0.001	1 5	$\mu\text{A}$
Negative Supply Current	I-	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full	-1 -5	-0.0001		
Logic Supply Current	I <sub>L</sub>	$V_L = 5.25\text{ V}, V_{IN} = 0\text{ or }5\text{ V}$	Room Full		0.001	1 5	
Ground Current	I <sub>GND</sub>	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full	-1 -5	-0.001		

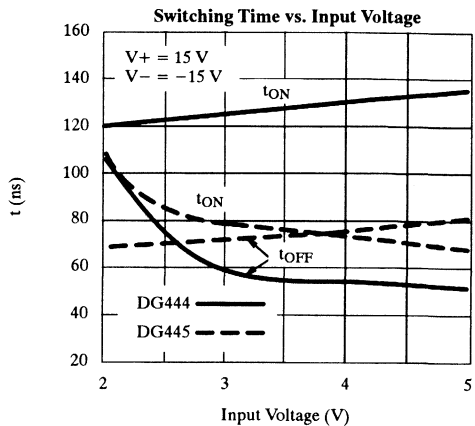
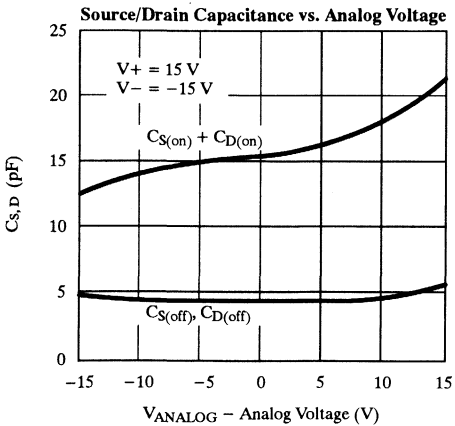
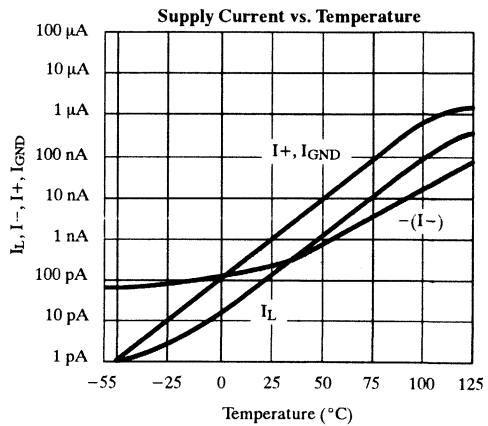
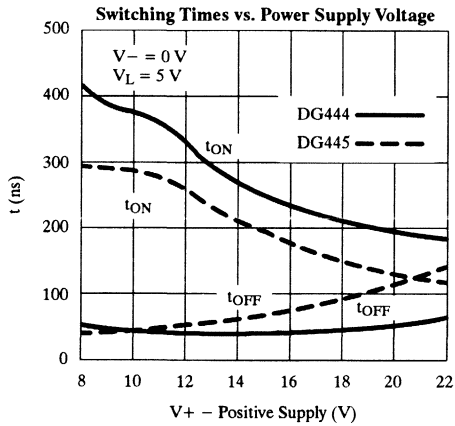
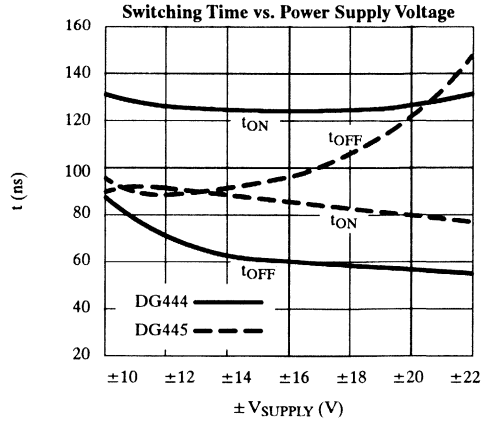
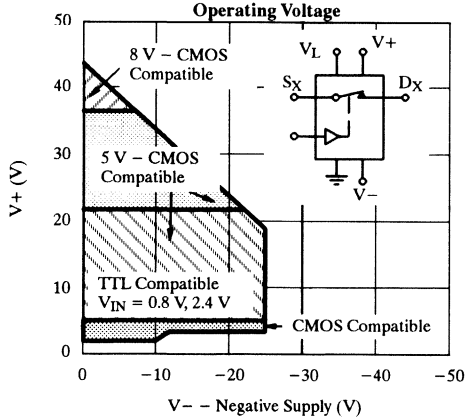
Notes:

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

## Typical Characteristics



**Typical Characteristics (Cont'd)**



## Schematic Diagram (Typical Channel)

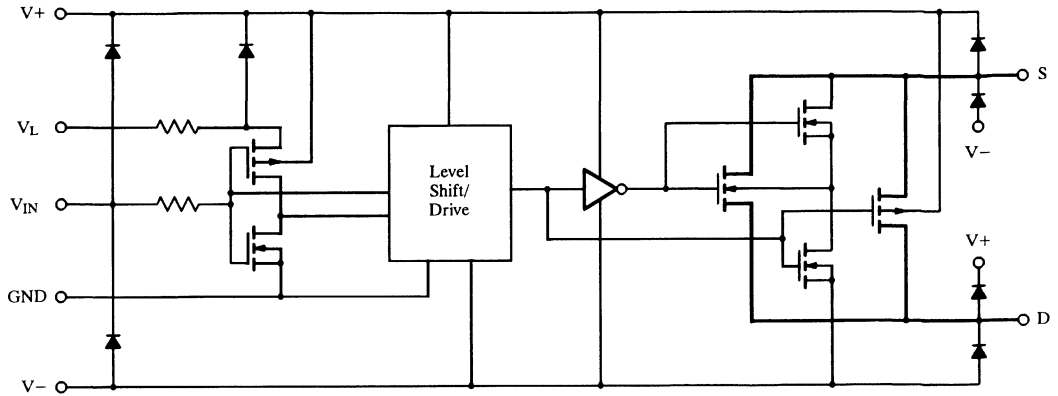
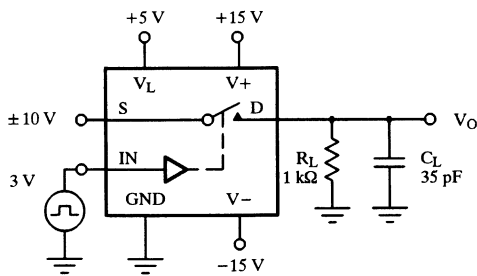
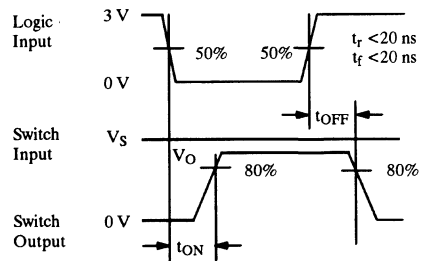


Figure 1.

## Test Circuits



$C_L$  (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG445.

Figure 2. Switching Time

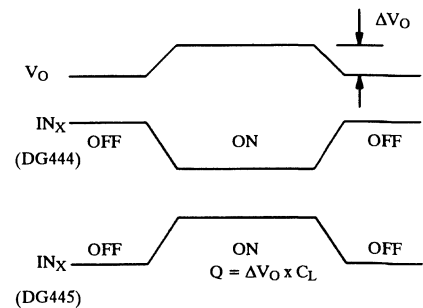
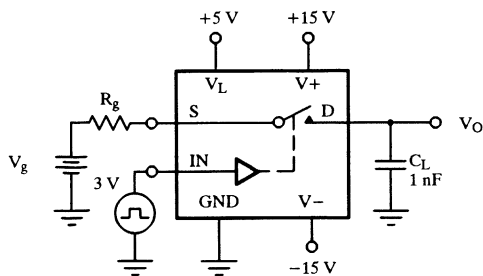
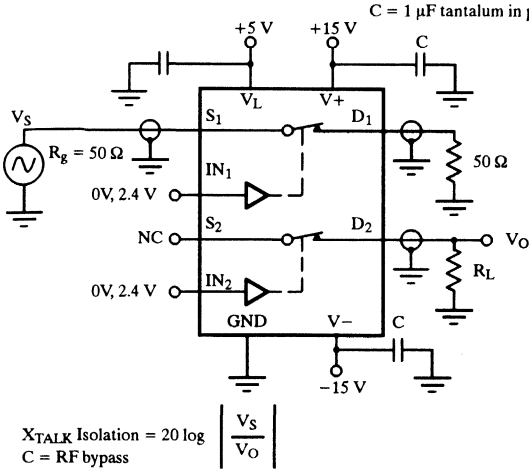


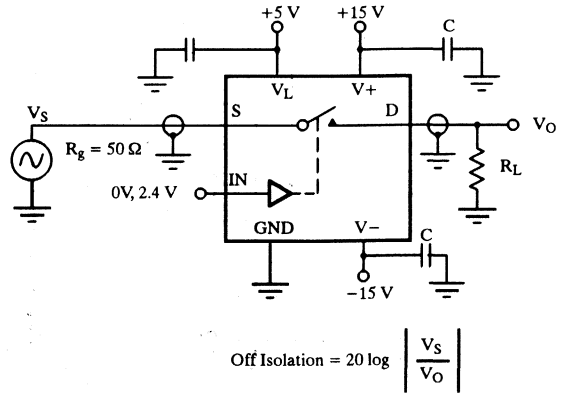
Figure 3. Charge Injection



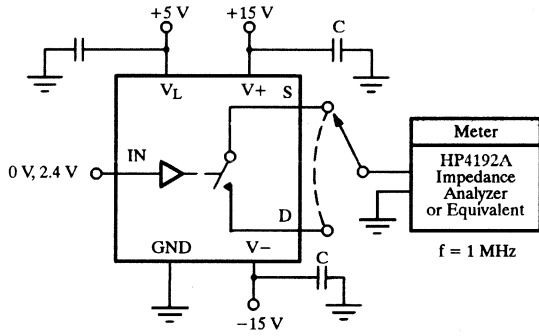
**Test Circuits (Cont'd)**



**Figure 4.** Crosstalk

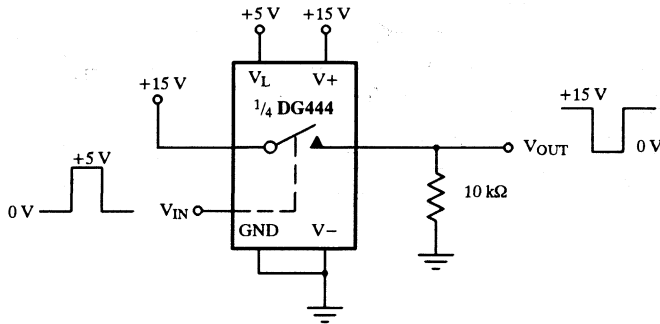


**Figure 5.** Off Isolation



**Figure 6.** Source/Drain Capacitances

**Applications**



**Figure 7.** Level Shifter

## Applications (Cont'd)

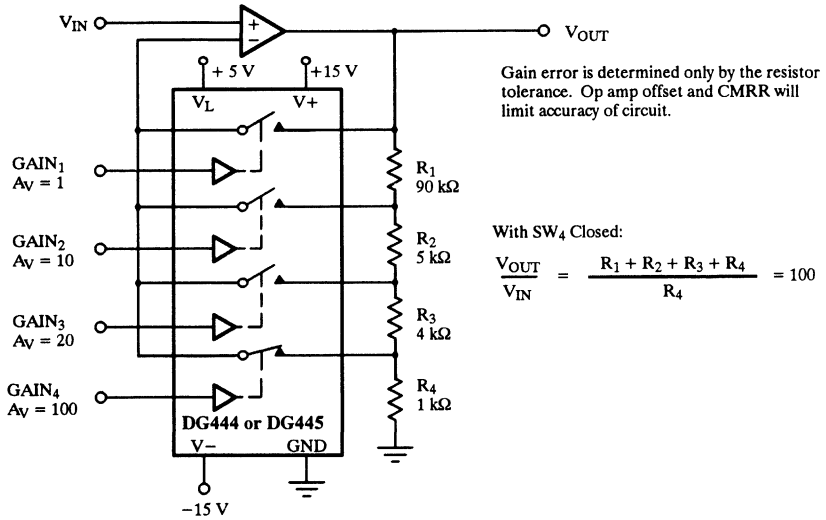


Figure 8. Precision-Weighted Resistor Programmable-Gain Amplifier

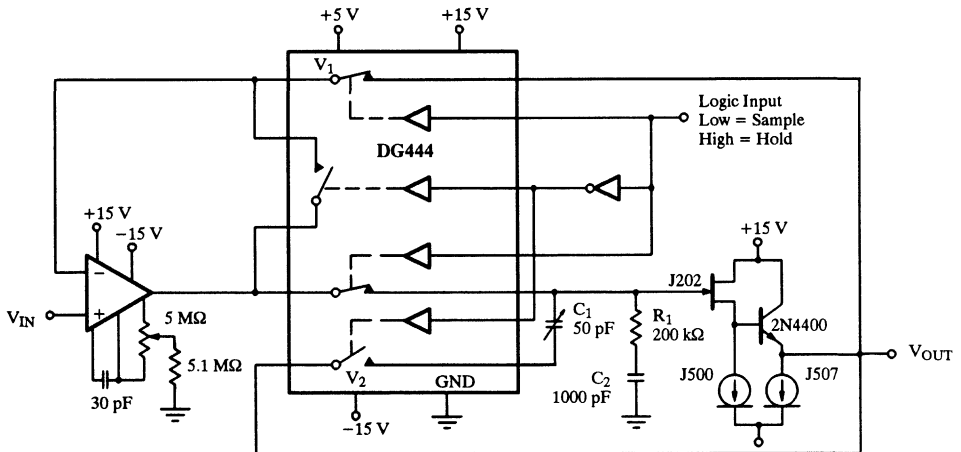


Figure 9. Precision Sample-and-Hold

## Wideband/Video "T" Switches

### Features

- Wide Bandwidth: 500 MHz
- Low Crosstalk: -85 dB
- High Off-Isolation: -80 dB @ 5 MHz
- "T" Switch Configuration
- TTL Logic Compatible
- Fast Switching— $t_{ON}$ : 45 ns
- Low  $r_{DS(on)}$ : 30  $\Omega$

### Benefits

- Flat Frequency Response
- High Color Fidelity
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Reduced Power Consumption
- Improved Data Throughput

### Applications

- RF and Video Switching
- RGB Switching
- Local and Wide Area Networks
- Video Routing
- Fast Data Acquisition
- ATE
- Radar/FLR Systems
- Video Multiplexing

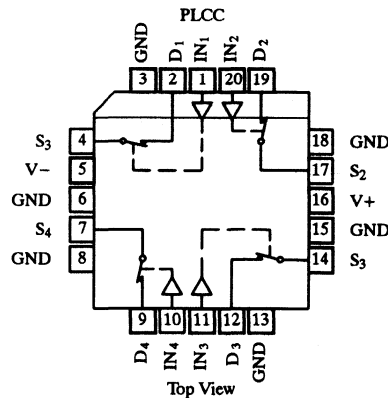
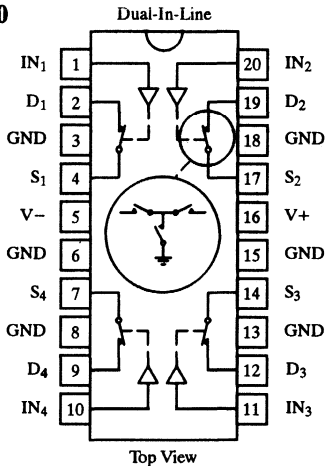
### Description

The DG540/541/542 are high performance monolithic wideband/video switches designed for switching RF, video and digital signals. By utilizing a "T" switch configuration on each channel, these devices achieve exceptionally low crosstalk and high off-isolation. The crosstalk and off-isolation of the DG540 are further improved by the introduction of extra GND pins between signal pins.

To achieve TTL compatibility, low channel capacitances and fast switching times, the DG540 family is built on the Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when on.

### Functional Block Diagrams and Pin Configurations

DG540



Ordering Information - DG540

Temp Range	Package	Part Number
-40 to 85°C	20-Pin Plastic DIP	DG540DJ
	20-Pin PLCC	DG540DN
-55 to 125°C	20-Pin Sidebrazed	DG540AP
		DG540AP/883

Truth Table

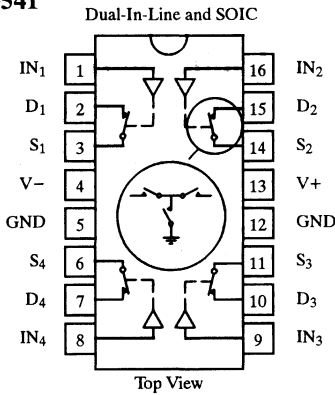
Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2$  V

Switches Shown for Logic "1" Input

## Functional Block Diagrams and Pin Configurations (Cont'd)

### DG541



Truth Table – DG541

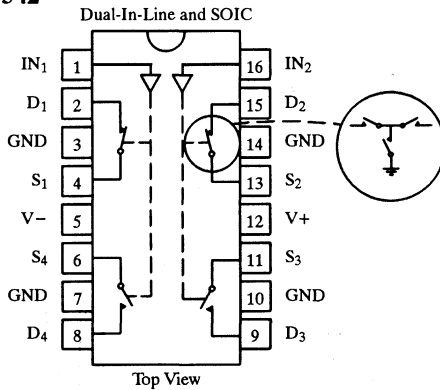
Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2$  V  
Switches Shown for Logic "1" Input

Ordering Information – DG541

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG541DJ
	16-Pin Narrow SOIC	DG541DY
-55 to 125°C	16-Pin Sidebraze	DG541AP
		DG541AP/883

### DG542



Truth Table – DG542

Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2$  V  
Switches Shown for Logic "1" Input

Ordering Information – DG542

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG542DJ
	16-Pin Narrow SOIC	DG542DY
-55 to 125°C	16-Pin Sidebraze	DG542AP
		DG542AP/883

## Absolute Maximum Ratings

V+ to V-	-0.3 V to 21 V
V+ to GND	-0.3 V to 21 V
V- to GND	-19 V to +0.3 V
Digital Inputs	(V-) -0.3 V to (V+) +0.3 V or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub>	(V-) -0.3 V to (V-) +14 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal)	20 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle max)	40 mA
Storage Temperature (AP Suffix)	-65 to 150°C
(DJ, DN, DY Suffixes)	-65 to 125°C

### Power Dissipation (Package)a

16-Pin Plastic DIP <sup>b</sup>	470 mW
20-Pin Plastic DIP <sup>c</sup>	800 mW
16-Pin Narrow Body SOIC <sup>d</sup>	640 mW
20-Pin PLCC <sup>d</sup>	800 mW
16-, 20-Pin Sidebraze DIP <sup>e</sup>	900 mW

### Notes:

- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C
- Derate 7 mW/°C above 25°C
- Derate 10 mW/°C above 75°C
- Derate 12 mW/°C above 75°C

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}$ $V_{\text{INH}} = 2\text{ V}, V_{\text{INL}} = 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffixes -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range	$V_{\text{ANALOG}}$	$V_- = -5\text{ V}, V_+ = 12\text{ V}$	Full		-5	8	-5	8	V	
Drain-Source On-Resistance	$r_{\text{DS(on)}}$	$I_S = -10\text{ mA}, V_D = 0\text{ V}$	Room Full	30		60 100		60 75	$\Omega$	
$r_{\text{DS(on)}}$ Match	$\Delta r_{\text{DS(on)}}$		Room	2		6		6		
Source Off Leakage Current	$I_{\text{S(off)}}$	$V_S = 0\text{ V}, V_D = 10\text{ V}$	Room Full	-0.05	-10 -500	10 500	-10 -100	10 100	nA	
Drain Off Leakage Current	$I_{\text{D(off)}}$	$V_S = 10\text{ V}, V_D = 0\text{ V}$	Room Full	-0.05	-10 -500	10 500	-10 -100	10 100		
Channel On Leakage Current	$I_{\text{D(on)}}$	$V_S = V_D = 0\text{ V}$	Room Full	-0.05	-10 -1000	10 1000	-10 -100	10 100		
<b>Digital Control</b>										
Input Voltage High	$V_{\text{INH}}$		Full		2		2		V	
Input Voltage Low	$V_{\text{INL}}$		Full			0.8		0.8		
Input Current	$I_{\text{IN}}$	$V_{\text{IN}} = \text{GND or } V_+$	Room Full	0.05	-1 -20	1 20	-1 -20	1 20	$\mu\text{A}$	
<b>Dynamic Characteristics</b>										
On State Input Capacitance <sup>e</sup>	$C_{\text{S(on)}}$	$V_S = V_D = 0\text{ V}$	Room	14		20		20	pF	
Off State Input Capacitance <sup>e</sup>	$C_{\text{S(off)}}$	$V_S = 0\text{ V}$	Room	2		4		4		
Off State Output Capacitance <sup>e</sup>	$C_{\text{D(off)}}$	$V_D = 0\text{ V}$	Room	2		4		4		
Bandwidth	BW	$R_L = 50\ \Omega$ , See Figure 5	Room	500					MHz	
Turn On Time	$t_{\text{ON}}$	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ 50% to 90% See Figure 2	DG540 DG541	Room Full	45		70 130		70 130	ns
			DG542	Room Full	55		100 160		100 160	
Turn Off Time	$t_{\text{OFF}}$		DG540 DG541	Room Full	20		50 85		50 85	
			DG542	Room Full	25		60 85		60 85	
Charge Injection	Q		$C_L = 1000\text{ pF}, V_S = 0\text{ V}$ See Figure 3	Room	-25					pC
Off Isolation	OIRR		$R_{\text{IN}} = 75\ \Omega, R_L = 75\ \Omega$ $f = 5\text{ MHz}$ , See Figure 4	DG540	Room	-80				
		DG541		Room	-60					
		DG542		Room	-75					
All Hostile Crosstalk	$X_{\text{TALK(AH)}}$	$R_{\text{IN}} = 10\ \Omega, R_L = 75\ \Omega$ $f = 5\text{ MHz}$ , See Figure 6	Room	-85						

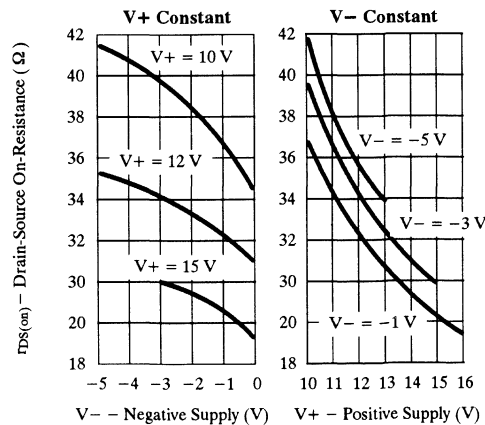
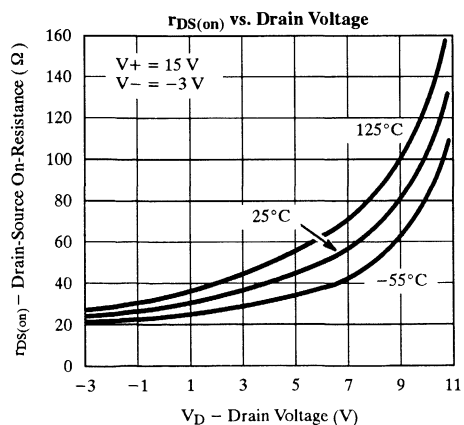
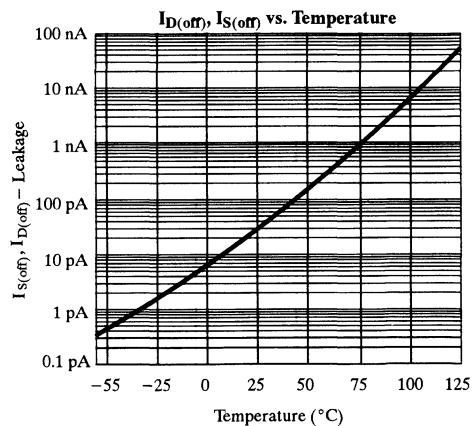
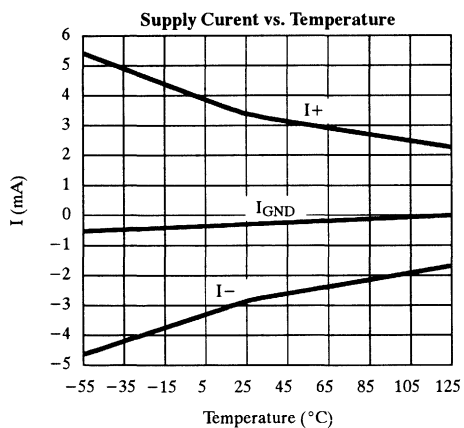
## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}$ $V_{INH} = 2\text{ V}, V_{INL} = 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffixes -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Power Supplies</b>										
Positive Supply Current	I+	All Channels On or Off	Room Full	3.5		6	9	6	9	mA
Negative Supply Current	I-		Room Full	-3.2	-6	-9	-6	-9		

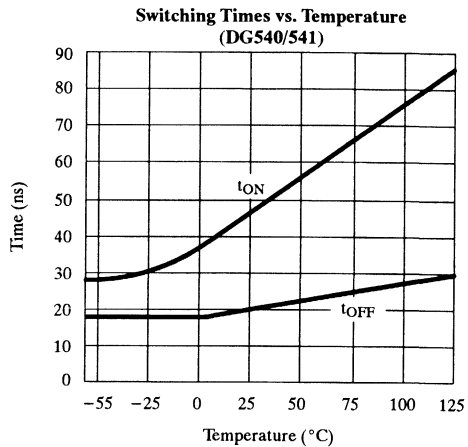
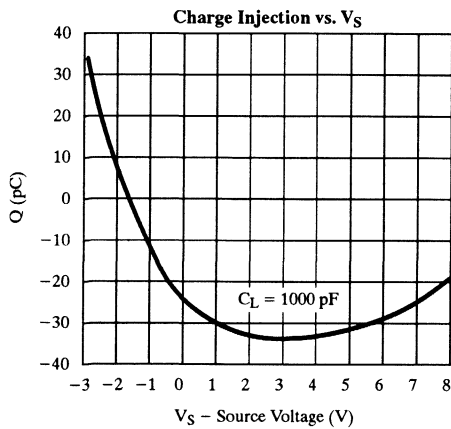
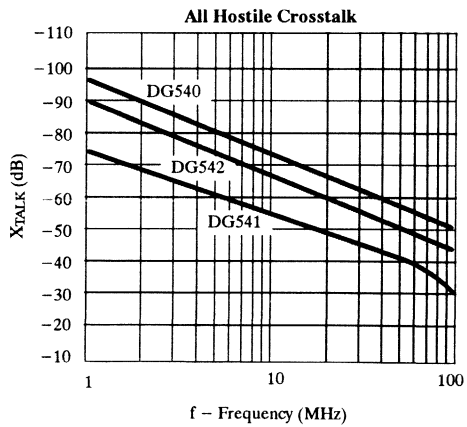
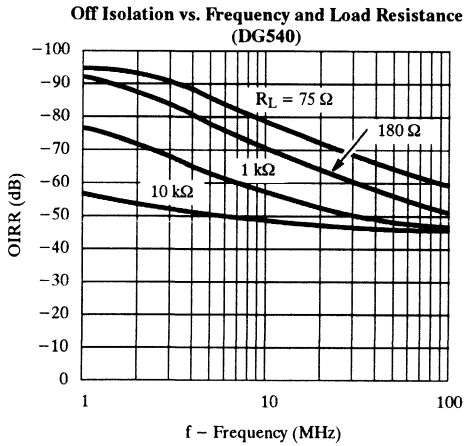
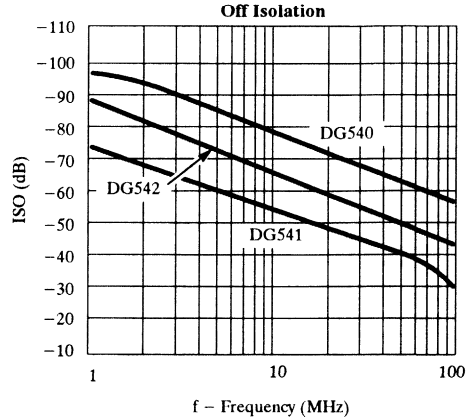
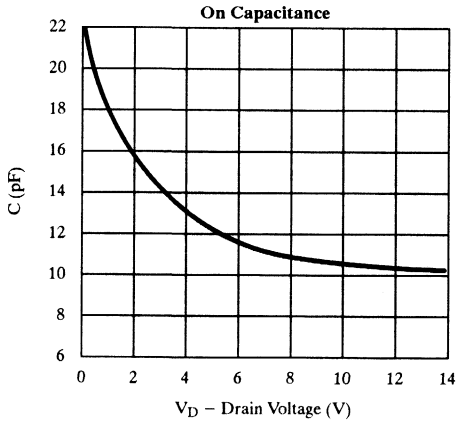
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

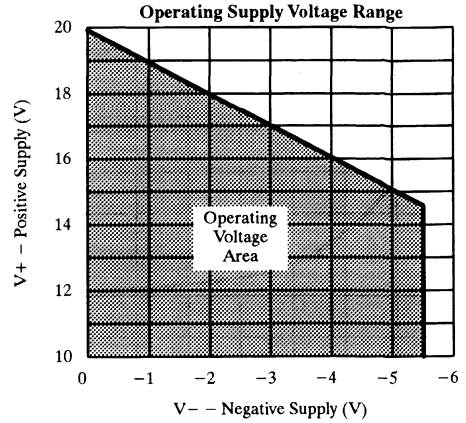
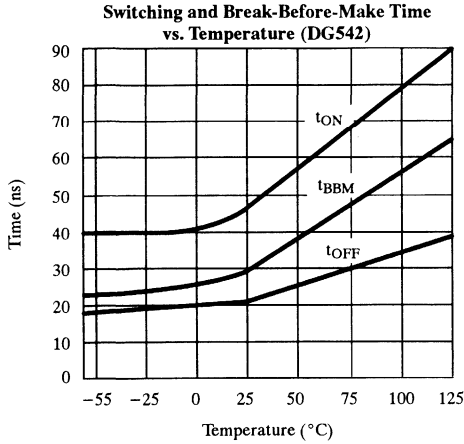
## Typical Characteristics



**Typical Characteristics (Cont'd)**



## Typical Characteristics (Cont'd)



## Schematic Diagram (Typical Channel)

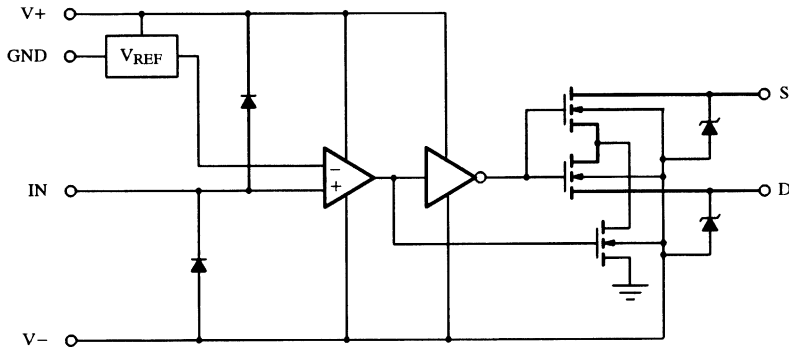
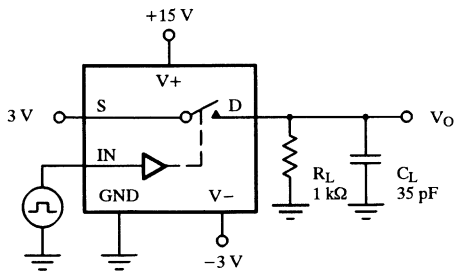


Figure 1.

## Test Circuits



$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + \tau_{DS(on)}}$$

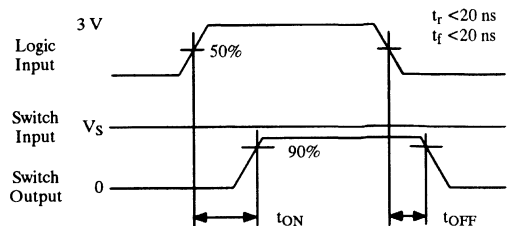
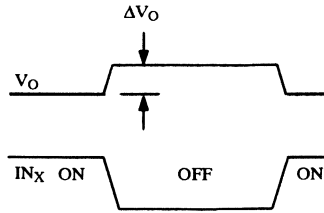
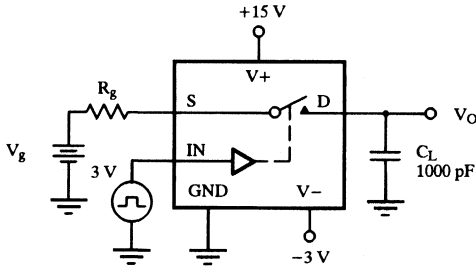


Figure 2. Switching Time

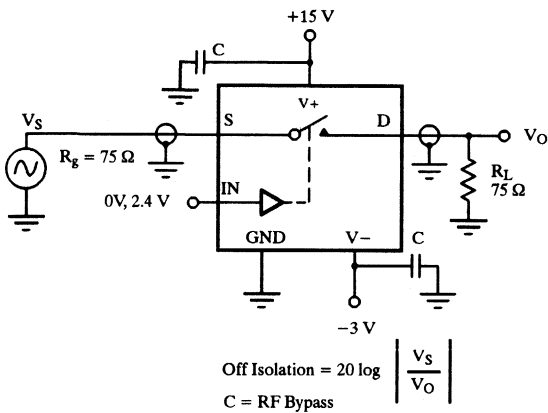


**Test Circuits (Cont'd)**



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $\Delta Q = C_L \times \Delta V_O$

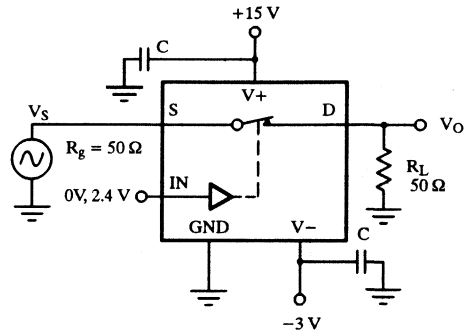
**Figure 3.** Charge Injection



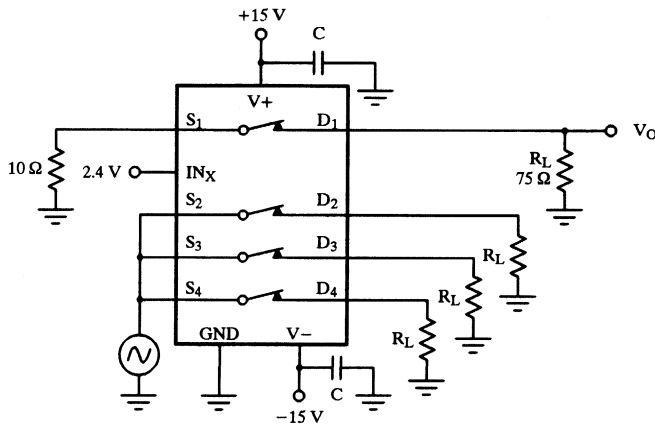
$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF Bypass

**Figure 4.** Off Isolation



**Figure 5.** Bandwidth



$$X_{\text{TALK(AH)}} = 20 \log_{10} \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

**Figure 6.** All Hostile Crosstalk

## Applications

### Device Description

The DG540/541/542 family of wideband switches offers true bidirectional switching of high frequency analog or digital signals with minimum signal crosstalk, low insertion loss, and negligible non-linearity distortion and group delay.

Built on the Siliconix D/CMOS process, these "T" switches provide excellent off-isolation with a bandwidth of around 500 MHz (350 MHz for DG541). Silicon-gate D/CMOS processing also yields fast switching speeds.

An on-chip regulator circuit maintains TTL input compatibility over the whole operating supply voltage range, easing control logic interfacing.

Circuit layout is facilitated by the interchangeability of source and drain terminals.

### Frequency Response

A single switch on-channel exhibits both resistance [ $r_{DS(on)}$ ] and capacitance [ $C_{S(on)}$ ]. This RC combination has an attenuation effect on the analog signal – which is frequency dependent (like an RC low-pass filter). The –3-dB bandwidth of the DG540 is typically 500 MHz (into 50  $\Omega$ ). This measured figure of 500 MHz illustrates that the switch channel can not be represented by a two stage RC combination. The on capacitance of the channel is distributed along the on-resistance, and hence becomes a more complex multi stage network of R's and C's making up the total  $r_{DS(on)}$  and  $C_{S(on)}$ . See Application Note AN502 for more details.

### Off-Isolation and Crosstalk

Off-isolation and crosstalk are affected by the load resistance and parasitic inter-electrode capacitances. Higher off-isolation is achieved with lower values of  $R_L$ . However, low values of  $R_L$  increase insertion loss requiring gain adjustments down the line. Stray capacitances, even a fraction of 1 pF, can cause a large crosstalk increase. Good layout and ground shielding techniques can considerably improve your ac circuit performance.

### Power Supplies

A useful feature of the DG54X family is its power supply flexibility. It can be operated from a single positive supply ( $V+$ ) if required ( $V-$  connected to ground).

Note that the analog signal must not exceed  $V-$  by more than –0.3 V to prevent forward biasing the substrate p-n junction. The use of a  $V-$  supply has a number of advantages:

- (291) It allows flexibility in analog signal handling, i.e., with  $V- = -5$  V and  $V+ = 12$  V; up to  $\pm 5$ -V ac signals can be controlled.
- (292) The value of on capacitance [ $C_{S(on)}$ ] may be reduced. A property known as 'the body-effect' on the DMOS switch devices causes various parametric effects to occur. One of these effects is the reduction in  $C_{S(on)}$  for an increasing  $V$  body–source. Note, however, that to increase  $V-$  normally requires  $V+$  to be reduced (since  $V+$  to  $V- = 21$  V max.). Reduction in  $V+$  causes an increase in  $r_{DS(on)}$ , hence a compromise has to be achieved. It is also useful to note that optimum video linearity performance (e.g., differential phase and gain) occurs when  $V-$  is around –3 V.
- (293)  $V-$  eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

### Decoupling

It is an established RF design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG54X is adversely affected by poor decoupling of power supply pins. Also, of even more significance, since the substrate of the device is connected to the negative supply, adequate decoupling of this pin is essential.

#### Rules:

- (1) Decoupling capacitors should be incorporated on all power supply pins ( $V+$ ,  $V-$ ). (See Figure 7.)
- (2) They should be mounted as close as possible to the device pins.
- (3) Capacitors should have good high frequency characteristics – tantalum bead and/or monolithic ceramic types are adequate.

Suitable decoupling capacitors are 1- to 10- $\mu$ F tantalum bead, plus 10- to 100-nF ceramic.

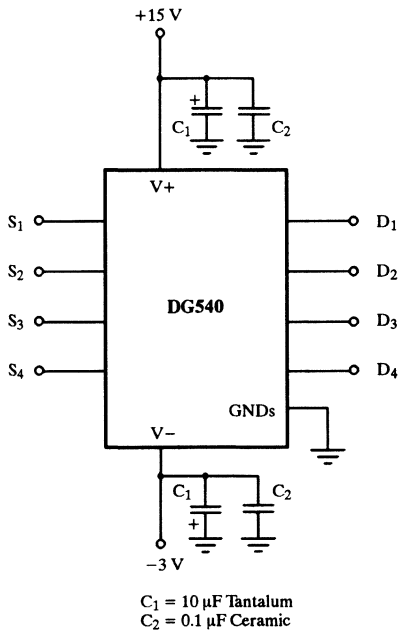


Figure 7. Supply Decoupling

## Board Layout

PCB layout rules for good high frequency performance must be observed to achieve the performance boasted by the DG540. Some tips for minimizing stray effects are:

- (1) Use extensive ground planes on double sided PCB, separating adjacent signal paths. Multilayer PCB is even better.
- (2) Keep signal paths as short as practically possible, with all channel paths of near equal length.
- (3) Careful arrangement of ground connections is also very important. Star connected system grounds eliminate signal current flowing through ground path parasitic resistance from coupling between channels.

Figure 8 shows a 4-channel video multiplexer using a DG540.

Figure 9 shows an RGB selector switch using two DG542s.

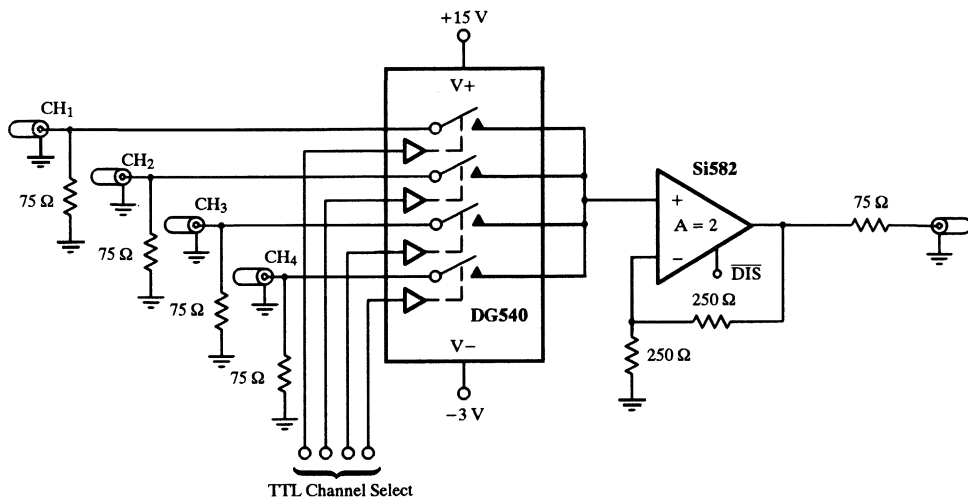


Figure 8. 4 by 1 Video Multiplexing Using the DG540

## Applications (Cont'd)

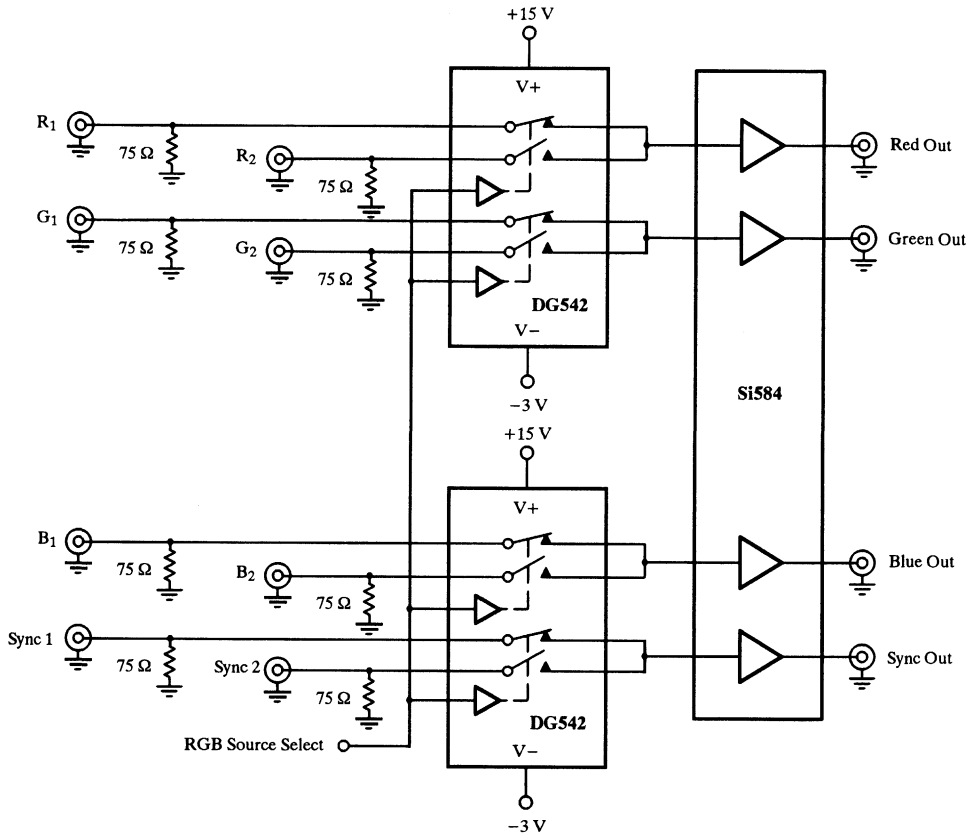


Figure 9. RGB Selector Using Two DG542s

# High-Speed Quad CMOS Analog Switch

## Features

- Fast Switching Action— $t_{ON}$ : 30 ns
- Low On-Resistance— $r_{DS(on)}$ : 20  $\Omega$
- Single-Supply Operation
- Low Charge Injection
- TTL and CMOS Logic Compatible

## Benefits

- Improved Data Throughput
- Reduced Switching Errors
- Simplified Power Supply
- Reduced Switching Transients
- Simplified Interfacing
- High Reliability

## Applications

- Hard Disk Drives
- Fast Sample-and-Hold Circuits
- Precision Instrumentation
- Computer Peripherals
- Low Noise Op Amp Gain Switching
- High-Rel Systems

## Description

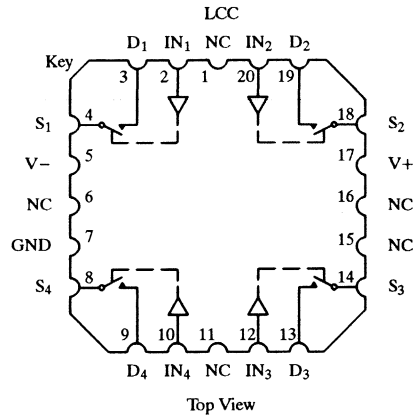
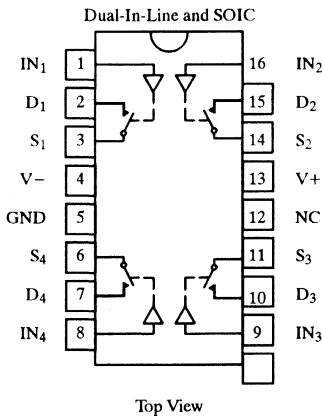
The DG601 is a high performance quad SPST CMOS analog switch intended for applications where fast switching, low charge injection and low on-resistance are required. The DG601 features single-supply operation, and is TTL-compatible with either a single 12-V supply, a single 5-V supply, or with  $\pm 5$ -V supplies.

Applications for the DG601 include 12-V systems requiring TTL or 5-V logic levels, such as disk drives and other

computer peripherals. The fast switching time and low charge injection make the DG601 ideal for high speed data acquisition applications such as sample and hold amplifiers, channel selection and gain ranging.

The DG601 is built on the Siliconix proprietary PolyMOS process, allowing low parasitic capacitance to facilitate high speed switching.

## Functional Block Diagram and Pin Configuration



### Ordering Information

Temp Range	Package	Part Number
40 to 85°C	16-Pin Plastic DIP	DG601DJ
	16-Pin Narrow SOIC	DG601DY
-55 to 125°C	16-Pin CerDIP	DG601AK
		DG601AK/883
	LCC-20	DG601AZ/883

### Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0"  $\leq 0.8$  V  
 Logic "1"  $\geq 2.4$  V  
 Switches Shown for Logic "1" Input



## Absolute Maximum Ratings

Voltages Referenced to V-	
V+	22 V
GND	13 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) plus 2 V or 30 mA, whichever occurs first
Current (any terminal)	30 mA
Current S or D (Pulsed 1 ms at 10% duty cycle)	100 mA
Storage Temperature (AK, AZ Suffixes)	-65 to 150°C
(DJ, DY Suffixes)	-65 to 125°C
Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	470 mW

16-Pin SOIC <sup>d</sup>	900 mW
16-Pin CerDIP <sup>e</sup>	900 mW
LCC-20 <sup>e</sup>	1200 mW

**Notes:**

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C
- Derate 7.7 mW/°C above 25°C
- Derate 12 mW/°C above 75°C

## Specifications<sup>a</sup> for Single 12-V Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		0	12	0	12	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V+ = 10.8 V, I <sub>S</sub> = 10 mA V <sub>D</sub> = 2 V, 10 V	Room Full	20		35			Ω
On-Resistance Matching <sup>g</sup>	Δr <sub>DS(on)</sub>		Room Full	2.2		6		6	
Switch Off Leakage Current	I <sub>S(off)</sub>	V+ = 13.2 V, V- = 0 V V <sub>D</sub> = 12.2 V, 1 V V <sub>S</sub> = 1 V, 12.2 V	Room Full	±0.01	-4	4	-4	4	nA
	I <sub>D(off)</sub>		Room Full	±0.01	-4	4	-4	4	
Channel On Leakage Current	I <sub>D(on)</sub>	V+ = 13.2 V, V- = 0 V V <sub>S</sub> , V <sub>D</sub> = 1 V, 12.2 V	Room Full	±0.1	-4	4	-4	4	
<b>Digital Control</b>									
Input Current with V <sub>IN</sub> Low	I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0 V	Full	-10 <sup>-5</sup>	-10		-10		μA
Input Current with V <sub>IN</sub> High	I <sub>IH</sub>	V <sub>IN</sub> Under Test = 5 V	Full	10 <sup>-5</sup>		10		10	
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF See Figure 2	Room	30		45		45	ns
Turn-Off Time	t <sub>OFF</sub>		Room	14		30		30	
Charge Injection	Q	C <sub>L</sub> = 1,000 pF, V <sub>gen</sub> = 6 V R <sub>gen</sub> = 0 Ω, See Figure 3	Room	13					pC
Off Isolation Reject Ratio	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	Room	69					dB
Crosstalk	X <sub>TALK</sub>		Room	88					
Source Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz, V <sub>S</sub> = 6 V	Room	8					pF
Drain Off Capacitance	C <sub>D(off)</sub>		Room	8					
Channel On Capacitance	C <sub>D(on)</sub>		Room	20					
<b>Power Supplies</b>									
Positive Supply Current	I+	V+ = 13.2 V, V- = 0 V V <sub>IN</sub> = 0 V or 5 V	Room Full	2.2		4		4	mA
Negative Supply Current	I-		Room Full	-2.1	-4		-4		

**Specifications<sup>a</sup> for Dual Supplies**

Parameter	Symbol	Test Conditions Unless Otherwise Specified  V <sub>+</sub> = 5 V, V <sub>-</sub> = -5 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-5	5	-5	5	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>+</sub> = 4.5 V, V <sub>-</sub> = -4.5 V I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±3.5 V	Room Full	27		40 60		40 60	Ω
On-Resistance Matching <sup>g</sup>	Δr <sub>DS(on)</sub>		Room Full	2		6 10		6 10	
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>+</sub> = 5.5 V, V <sub>-</sub> = -5.5 V V <sub>D</sub> = ∓4.5 V, V <sub>S</sub> = ±4.5 V	Room	0.01					nA
	I <sub>D(off)</sub>		Room	0.01					
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>+</sub> = 5.5 V, V <sub>-</sub> = 5.5 V V <sub>S</sub> = V <sub>D</sub> = ±4.5 V	Room	0.1					
<b>Digital Control</b>									
Input Current with V <sub>IN</sub> Low	I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0 V All Other = 5 V	Room	-10					pA
Input Current with V <sub>IN</sub> High	I <sub>IH</sub>	V <sub>IN</sub> Under Test = 5 V All Other = 0 V	Room	10					
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF See Figure 2	Room	34					ns
Turn-Off Time	t <sub>OFF</sub>		Room	20					
Charge Injection	Q	V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω C <sub>L</sub> = 1 nF, See Figure 3	Room	11					pC
Source Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V	Room	8					pF
Drain Off Capacitance	C <sub>D(off)</sub>		Room	8					
Channel On Capacitance	C <sub>D(on)</sub>		Room	21					
<b>Power Supplies</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 5.5 V, V <sub>-</sub> = -5.5 V V <sub>IN</sub> = 0 V or 5 V	Room	1.8					mA
Negative Supply Current	I <sub>-</sub>		Room	-1.8					

**Specifications<sup>a</sup> for Single 5-V Supply**

Parameter	Symbol	Test Conditions Unless Otherwise Specified  V <sub>+</sub> = 5 V, V <sub>-</sub> = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		0	5	0	5	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>+</sub> = 4.5 V, I <sub>S</sub> = -10 mA V <sub>D</sub> = 2 V, 3.5 V	Room Full	50		100 140		100 140	Ω
On-Resistance Matching <sup>g</sup>	Δr <sub>DS(on)</sub>		Room Full	2		10 15		10 15	
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>+</sub> = 5.5 V V <sub>D</sub> = 1 V, V <sub>S</sub> = 4.5 V	Room	±0.01					nA
	I <sub>D(off)</sub>		Room	±0.01					
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>+</sub> = 5.5 V V <sub>S</sub> = V <sub>D</sub> = 4.5 V, 1 V	Room	±0.1					

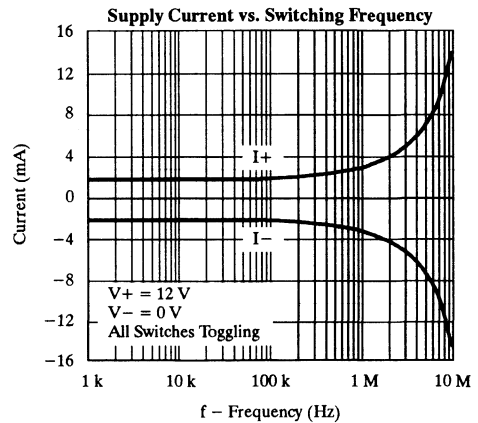
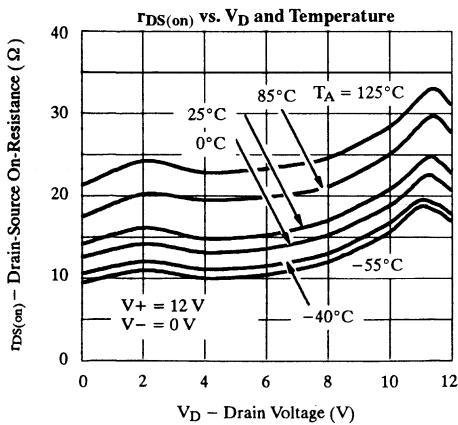
## Specifications<sup>a</sup> for Single 5-V Supply (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Digital Control</b>									
Input Current with $V_{IN}$ Low	$I_{IL}$	$V_{IN}$ Under Test = 0 V	Room	-10					pA
Input Current with $V_{IN}$ High	$I_{IH}$	$V_{IN}$ Under Test = 5 V	Room	10					
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ See Figure 2	Room	32					ns
Turn-Off Time	$t_{OFF}$		Room	25					
Charge Injection	Q	$V_{gen} = 2.5\text{ V}, R_{gen} = 0\ \Omega$ $C_L = 1\text{ nF}$ , See Figure 3	Room	6					pC
Source Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}, V_S = 2.5\text{ V}$	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	22					
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_+ = 5.5\text{ V}, V_{IN} = 0\text{ V}$ or 5 V	Room	1.2					mA
Negative Supply Current	I-		Room	-0.8					

**Notes:**

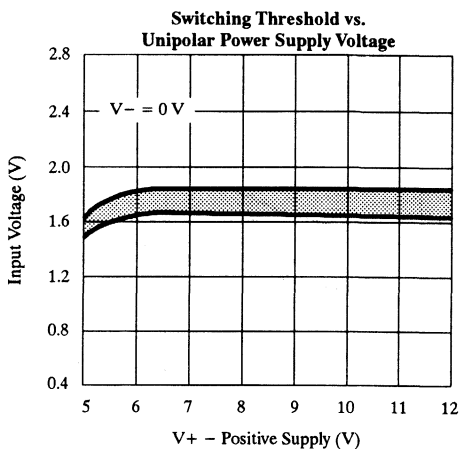
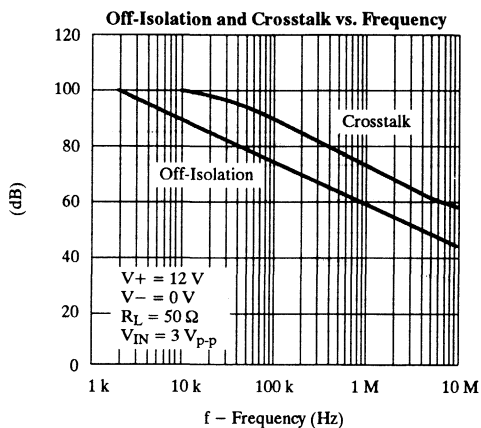
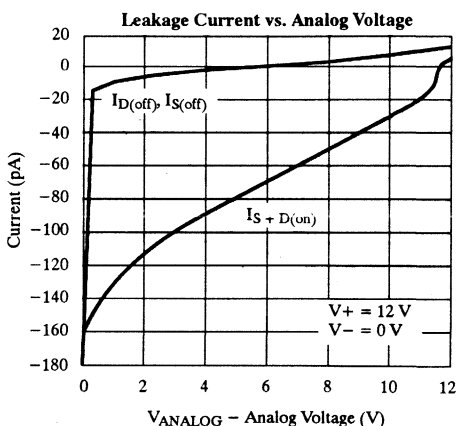
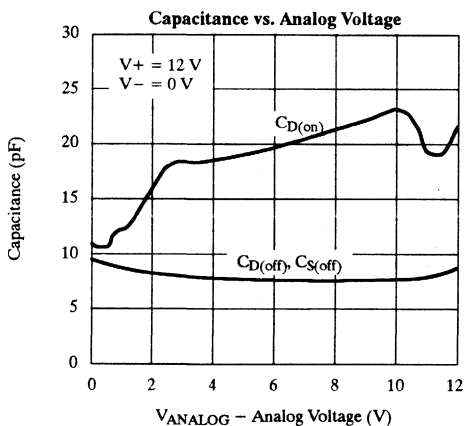
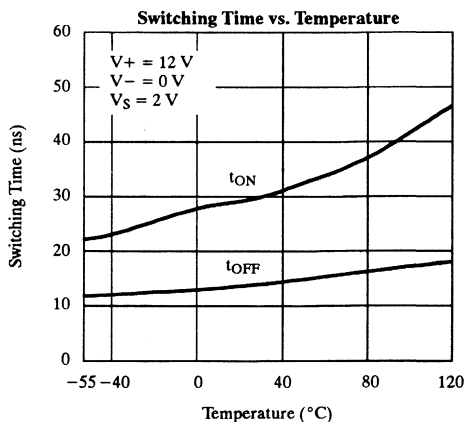
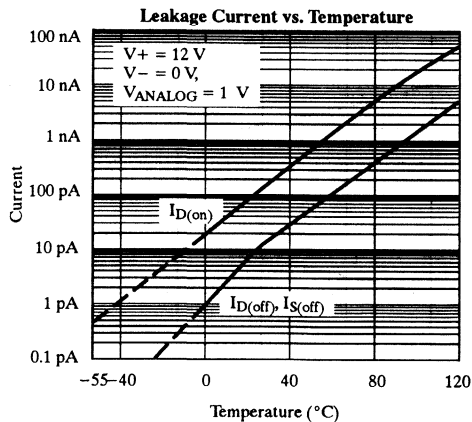
- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.
- $\Delta r_{DS(on)}$  compares on-resistance at the specified  $V_D$  values.

## Typical Characteristics

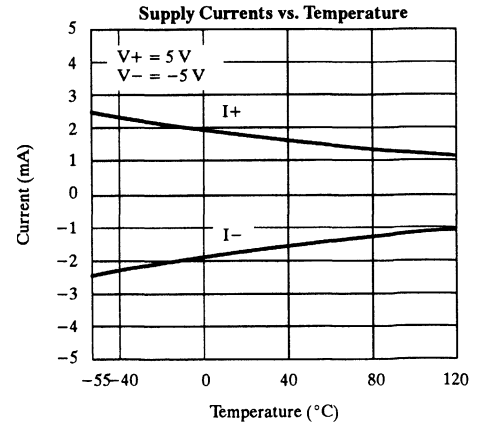
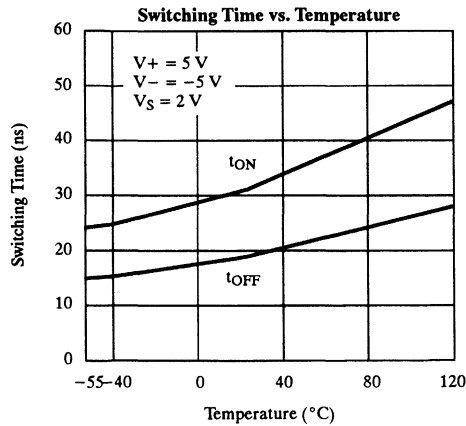
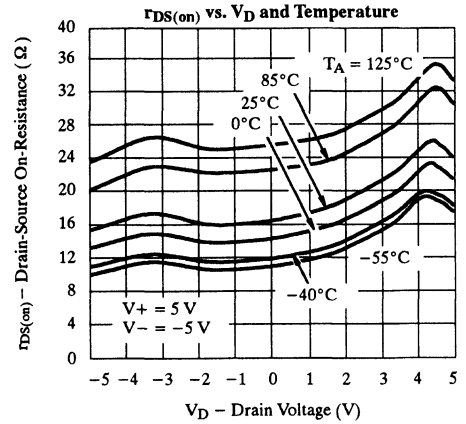
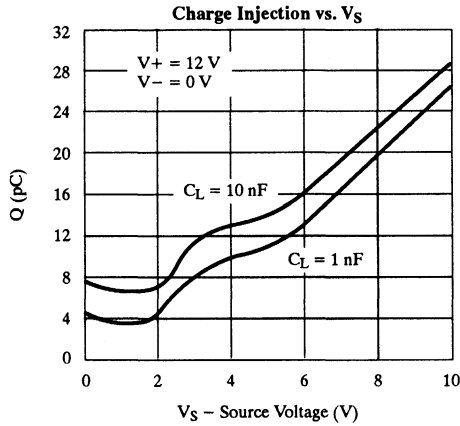
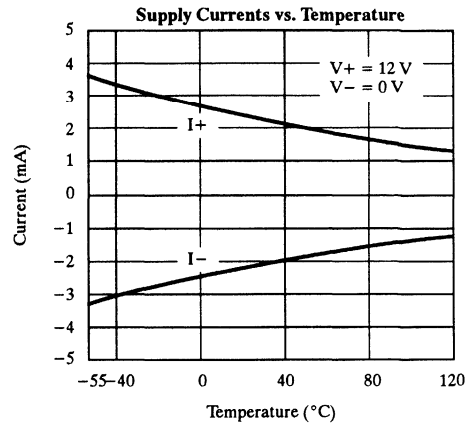
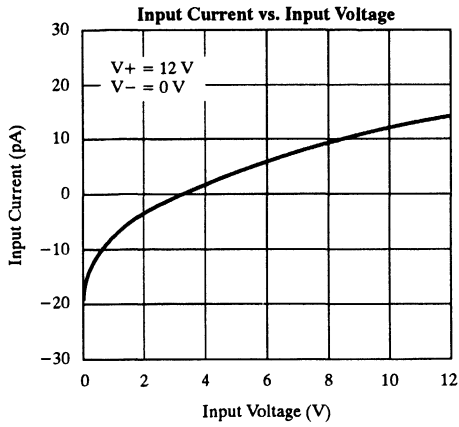




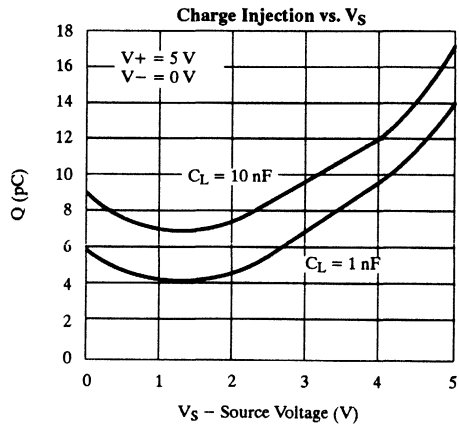
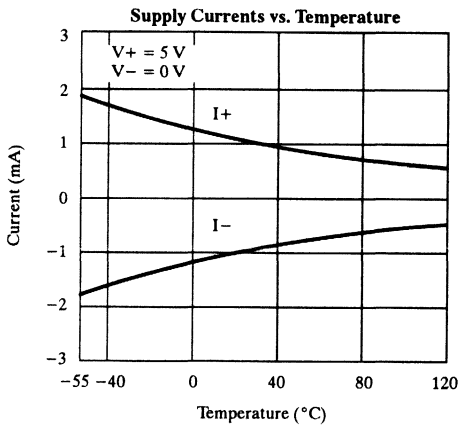
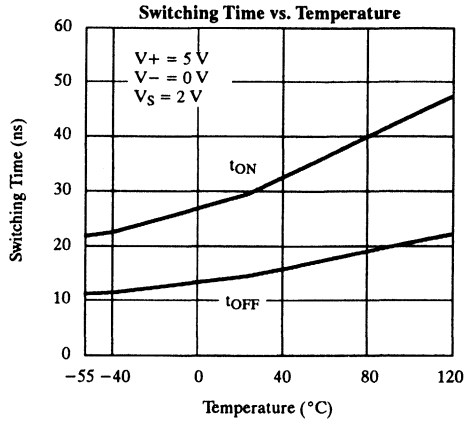
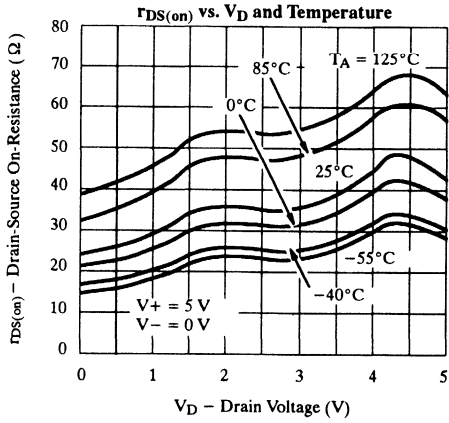
**Typical Characteristics (Cont'd)**



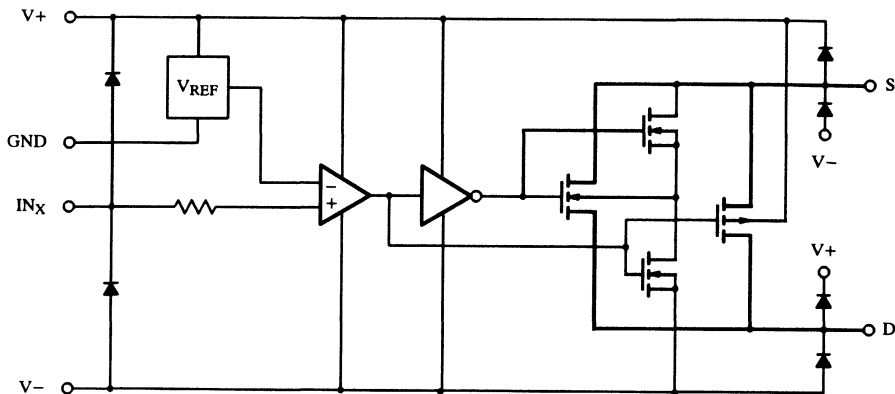
## Typical Characteristics (Cont'd)



**Typical Characteristics (Cont'd)**

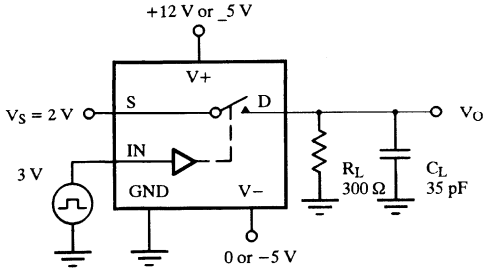


**Schematic Diagram (Typical Channel)**



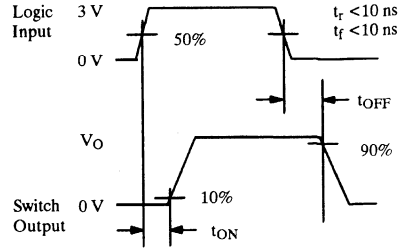
**Figure 1**

## Test Circuits

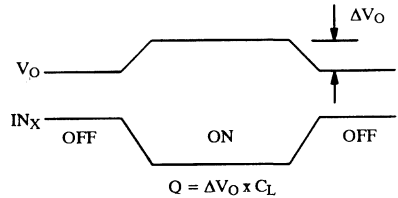
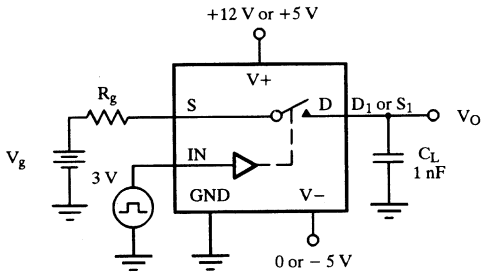


$C_L$  (includes fixture and stray capacitance)

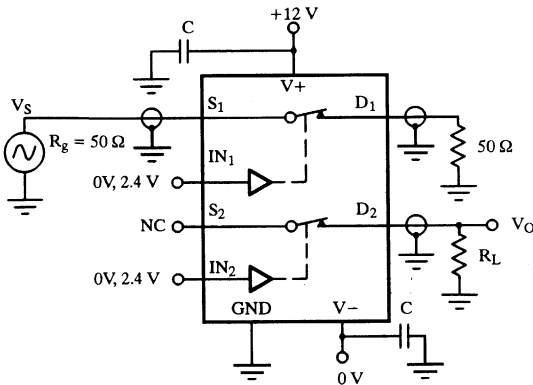
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



**Figure 2** Switching Time



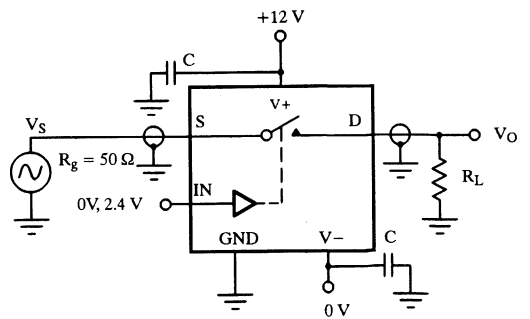
**Figure 3** Charge Injection



$$X_{TALK} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

**Figure 4** Crosstalk

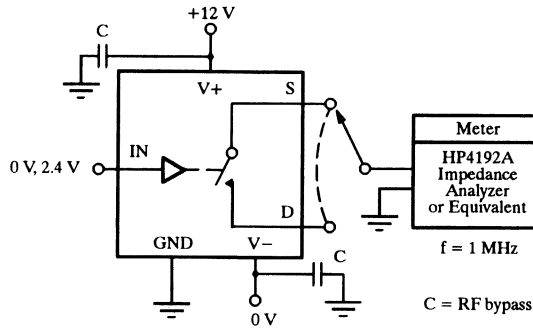


$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

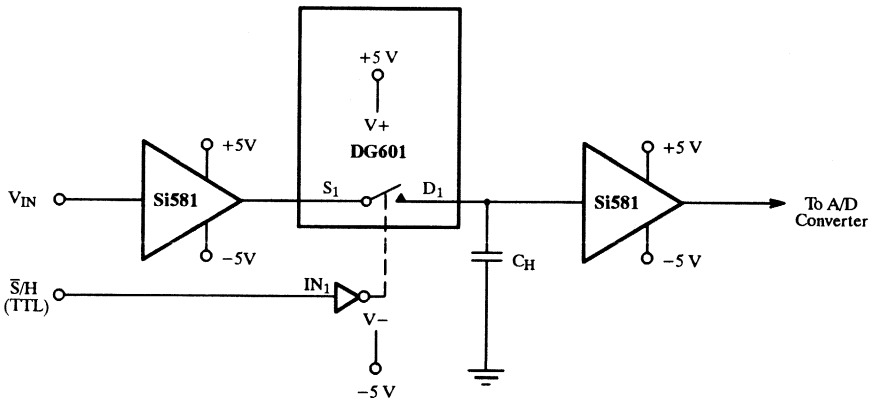
C = RF bypass

**Figure 5** Off Isolation

**Test Circuits (Cont'd)**



**Figure 6** Source/Drain Capacitances



**Figure 7** Simple High-Speed Sample-and-Hold Circuit for Data Acquisition System Front Ends

**Applications**

**Application Examples**

Analog switches are found in a variety of applications. The DG601 is useful in applications that require low-supply voltages, high-speed switching, and/or low on-resistance. Computer peripherals, such as disk drives, are an example of single-supply (12-V or 5-V) systems that use analog switches for sampling, signal conditioning, signal routing, and level translation. High-speed data acquisition systems typically use  $\pm 5$ -V supplies for the flash converters, and they require very fast, accurate switches for the input sample-and-hold amplifiers.

**Sample-and-Hold Amplifiers**

Figure 7 shows a sample-and-hold amplifier that provides a very fast sample acquisition time with the  $\pm 5$ -V power supplies that are required for high-speed A/D converters. The circuit is controlled by the sample-and-hold input, which is a TTL (5-V CMOS) control line. When a logic "0" is applied to the sample-and-hold input, the switch is turned on. A sample of the input signal is acquired by charging up the hold capacitor ( $C_H$ ) to the value of the input signal. When a logic "1" is applied, the switch is turned off. The value of the input signal at the time the switch is turned off is held in  $C_H$ . The sample-and-hold amplifier is designed for the following features:

## Sample-and-Hold Amplifiers (Cont'd)

### 1. $\pm 5$ -V Operation

The DG601 and Si581 buffer are both rated for  $\pm 5$ -V operation.

### 2. Low Pedestal Error

This is a result of the low charge injection of the DG601. Pedestal error can be reduced even further by using other switches in the quad to cancel out the injected charge (Figure 8).

### 3. Fast Acquisition Time

Sample-and-hold amplifiers take advantage of the fast switching time of the DG601 with a (+5-V supply,  $t_{ON}$  is typically 50 ns) and the high slew rate (800 V/ $\mu$ s) of the Si581.

The 20- $\mu$ A bias current for the Si581 will result in a 20-mV/ $\mu$ s droop rate, which is adequate for 8-bit operation at a 1-MHz sampling rate. Better droop rate can be achieved with a lower input-bias current buffer, such as a FET input device.

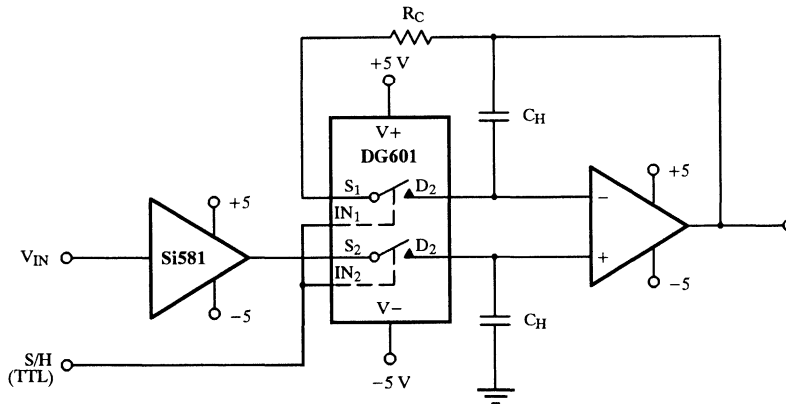
### 4. TTL-Compatible Operation

## Precision Signal Routing

The low on-resistance of the DG601 makes it an ideal choice for digitally controlled analog signal conditioning applications, such as channel selection and gain ranging in low-voltage systems. High-voltage switches (like the DG201A) suffer increased on-resistance and logic incompatibility when operated at lower supply voltages like +12 V. The 30- $\Omega$  on-resistance of the DG601 helps to maintain low impedance levels and reduce switch resistance-induced offsets and noise.

## Level Translation Applications

The DG601 makes an excellent level translator for use with MOSPOWER drivers, relay drivers, JFET drivers, GaAs FET drivers, DMOS drivers, and other circuits that require high-speed 5-V logic compatibility and an output range up to 12 V. Figure 9 shows one-half of a DG601 acting as the interface between the TTL and the Si9950 half-bridge driver. The Si9950 has a 1000-pF input capacitance, which is difficult to drive from a standard logic gate. The DG601 delivers a fast level translation from a TTL signal to provide 12 V of enhancement on the Si9950. A 180- $\Omega$  resistor is placed in series with the Si9950 input to limit the current through the DG601 to 100 mA (worst case). This prevents the current from exceeding the absolute maximum current rating. Increased gate drive current can be handled by connecting two sets of switches in parallel.

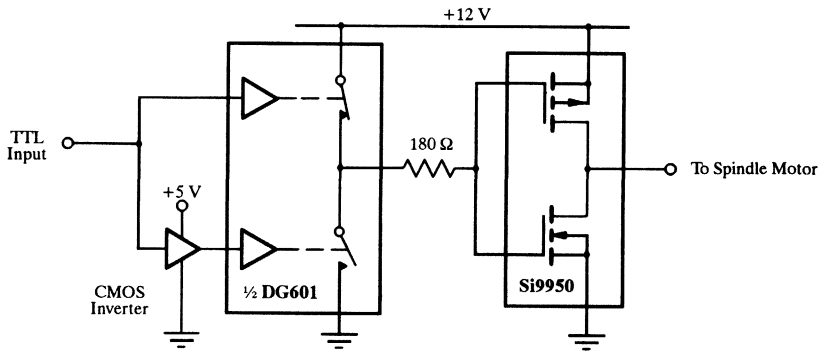


**Figure 8** Using On-Board Switches to Cancel Out Charge Injection

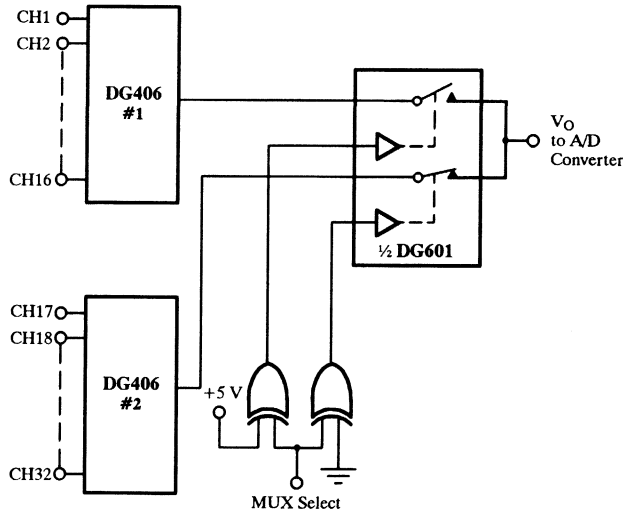
**Conclusion**

The DG601 has many applications in low-voltage systems, having been designed and specified for 12-V, TTL-compatible operation. It is also excellent in  $\pm 5$ -V and single 5-V supply applications where fast switching speed,

low charge injection, and low on-resistance are required. This data sheet highlights some typical applications to assist the design engineer in getting optimum performance in low-voltage mixed analog/digital systems.



**Figure 9** DG601 Provides Level Translation for MOSFET Gate Drive



**Figure 10** Super Multiplexing Improves Settling Times

## High-Speed, Low-Glitch D/CMOS Analog Switches

### Features

- Fast Switching— $t_{ON}$ : 12 ns
- Low Charge Injection:  $\pm 2$  pC
- Wide Bandwidth: 500 MHz
- 5-V CMOS Logic Compatible
- Low  $r_{DS(on)}$ : 18  $\Omega$
- Low Quiescent Power : 1.2 nW
- Single Supply Operation

### Benefits

- Improved Data Throughput
- Minimal Switching Transients
- Improved System Performance
- Easily Interfaced
- Low Insertion Loss
- Minimal Power Consumption

### Applications

- Fast Sample-and-Holds
- Synchronous Demodulators
- Pixel-Rate Video Switching
- Disk/Tape Drives
- DAC Deglitching
- Switched Capacitor Filters
- GaAs FET Drivers
- Satellite Receivers

### Description

The DG611/612/613 feature high-speed low-capacitance lateral DMOS switches. Charge injection has been minimized to optimize performance in fast sample-and-hold applications.

Each switch conducts equally well in both directions when on and blocks up to 16 V<sub>p-p</sub> when off. Capacitances have been minimized to ensure fast switching and low-glitch energy. To achieve such fast and clean switching performance, the DG611/612/613 are built on the Siliconix proprietary

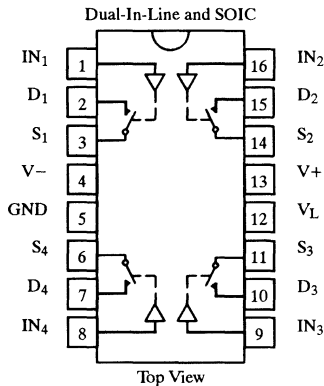
D/CMOS process. This process combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. An epitaxial layer prevents latchup.

The DG611 and DG612 differ only in that they respond to opposite logic levels. The versatile DG613 has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, one DPDT.

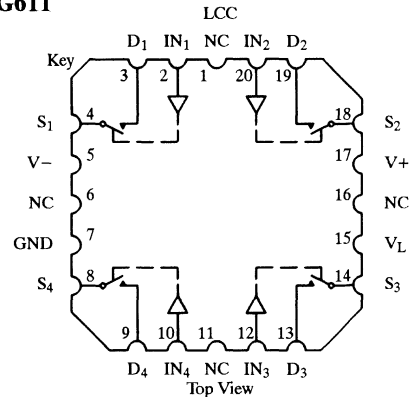
For additional information see Applications Note AN207.

### Functional Block Diagram and Pin Configuration

#### DG611



#### DG611



#### Ordering Information – DG611/612

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG611DJ
		DG612DJ
	16-Pin Narrow SOIC	DG611DY
		DG612DY
-55 to 125°C	16-Pin CerDIP	DG611AK/883
		DG612AK/883
	LCC-20	DG611AZ/883
		DG612AZ/883

#### Four SPST Switches per Package

#### Truth Table

Logic	DG611	DG612
0	ON	OFF
1	OFF	ON

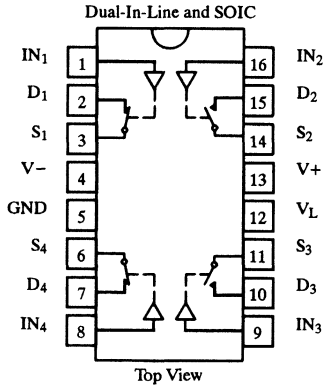
Logic "0"  $\leq 1$  V  
Logic "1"  $\geq 4$  V

Switches Shown for DG611 Logic "1" Input

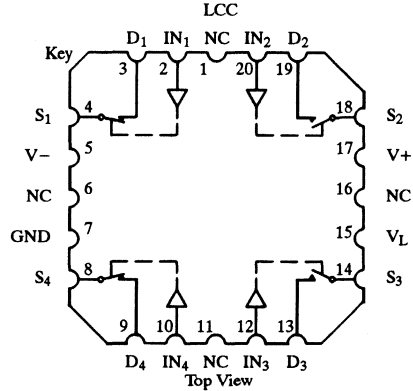


**Functional Block Diagram and Pin Configuration (Cont'd)**

**DG613**



**DG613**



**Ordering Information – DG613**

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG613DJ
	16-Pin Narrow SOIC	DG613DY
-55 to 125°C	16-Pin CerDIP	DG613AK/883
	LCC-20	DG613AZ/883

**Four SPST Switches per Package**

**Truth Table**

Logic	SW <sub>1</sub> , SW <sub>4</sub>	SW <sub>2</sub> , SW <sub>3</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 1 V  
Logic "1" ≥ 4 V

Switches Shown for Logic "1" Input

**Absolute Maximum Ratings**

V+ to V-	-0.3 V to 21 V
V+ to GND	-0.3 V to 21 V
V- to GND	-19 V to 0.3 V
V <sub>L</sub> to GND	-1 V to (V+) + 1 V or 20 mA, whichever occurs first
V <sub>IN</sub> <sup>a</sup>	(V-) -1 V to (V+) + 1 V or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub> <sup>a</sup>	(V-) -0.3 V to (V-) + 16 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal)	±30 mA
Current, S or D (Pulsed at 1 μs, 10% Duty Cycle)	±100 mA
Storage Temperature: CerDIP	-65 to 150°C
Plastic	-65 to 125°C

**Power Dissipation (Package)<sup>b</sup>**

16-Pin Plastic DIP <sup>c</sup>	470 mW
16-Pin Narrow SOIC <sup>d</sup>	600 mW
16-Pin CerDIP <sup>e</sup>	900 mW
20-Pin LCC <sup>e</sup>	900 mW

**Notes:**

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C
- Derate 7.6 mW/°C above 75°C
- Derate 12 mW/°C above 75°C

**CAUTION:** ESD (electrostatic discharge) sensitive. All pins are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Use proper ESD control procedures.

**Recommended Operating Range**

V+	5 V to 21 V
V-	-10 V to 0 V
V <sub>L</sub>	4 V to V+

V <sub>IN</sub>	0 V to V <sub>L</sub>
V <sub>ANALOG</sub>	V- to (V+) - 5 V

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 4\text{ V}, 1\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$	$V_- = -5\text{ V}, V_+ = 12\text{ V}$	Full		-5	7	-5	7	V
Switch On-Resistance	$r_{DS(on)}$	$I_S = -1\text{ mA}, V_D = 0\text{ V}$	Room	18		45		45	Ω
Resistance Match Bet Ch.	$\Delta r_{DS(on)}$		Room	2					
Source Off Leakage	$I_{S(off)}$	$V_S = 0\text{ V}, V_D = 10\text{ V}$	Room Hot	$\pm 0.001$	-0.25 -20	0.25 20	-0.25 -20	0.25 20	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_S = 10\text{ V}, V_D = 0\text{ V}$	Room Hot	$\pm 0.001$	-0.25 -20	0.25 20	-0.25 -20	0.25 20	
Switch On Leakage Current	$I_{D(on)}$	$V_S = V_D = 0\text{ V}$	Room Hot	$\pm 0.001$	-0.4 -40	0.4 40	-0.4 -40	0.4 40	
<b>Digital Control</b>									
Input Voltage High	$V_{IH}$		Full		4		4		V
Input Voltage Low	$V_{IL}$		Full			1		1	
Input Current	$I_{IN}$		Room Hot	0.005	-1 -20	1 20	-1 -20	1 20	μA
Input Capacitance	$C_{IN}$		Room	5					pF
<b>Dynamic Characteristics</b>									
Off State Input Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}$	Room	3					pF
Off State Output Capacitance	$C_{D(off)}$	$V_D = 0\text{ V}$	Room	2					
On State Input Capacitance	$C_{S(on)}$	$V_S = V_D = 0\text{ V}$	Room	10					
Bandwidth	BW	$R_L = 50\text{ Ω}$	Room	500					MHz
Turn-On Time <sup>e</sup>	$t_{ON}$	$R_L = 300\text{ Ω}, C_L = 3\text{ pF}, V_S = \pm 2\text{ V}$ See Test Circuit, Figure 2	Room	12		25		25	ns
Turn-Off Time <sup>e</sup>	$t_{OFF}$		Room	8		20		20	
Turn-On Time	$t_{ON}$	$R_L = 300\text{ Ω}, C_L = 75\text{ pF}, V_S = \pm 2\text{ V}$ See Test Circuit, Figure 2	Room Full	19		35 50		35 50	
Turn-Off Time	$t_{OFF}$		Room Full	16		25 35		25 35	
Charge Injection <sup>e</sup>	Q	$C_L = 1\text{ nF}, V_S = 0\text{ V}$	Room	4					pC
Ch. Injection Change <sup>e, g</sup>	$\Delta Q$	$C_L = 1\text{ nF},  V_S  \leq 3\text{ V}$	Room	3		4		4	
Off Isolation <sup>e</sup>	OIRR	$R_{IN} = 50\text{ Ω}, R_L = 50\text{ Ω}, f = 5\text{ MHz}$	Room	74					dB
Crosstalk <sup>e</sup>	$X_{TALK}$	$R_{IN} = 10\text{ Ω}, R_L = 50\text{ Ω}, f = 5\text{ MHz}$	Room	87					
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V or } 5\text{ V}$	Room Full	0.005		1 5		1 5	μA
Negative Supply Current	$I_-$		Room Full	-0.005	-1 -5		-1 -5		
Logic Supply Current	$I_L$		Room Full	0.005		1 5		1 5	
Ground Current	$I_{GND}$		Room Full	-0.005	-1 -5		-1 -5		

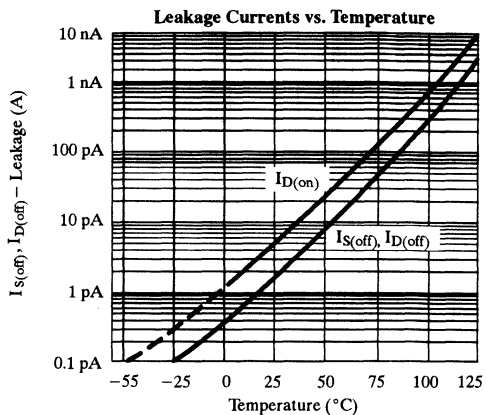
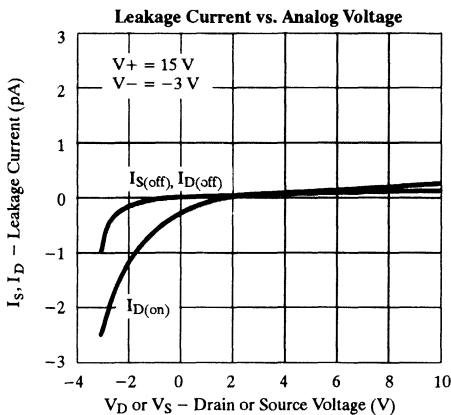
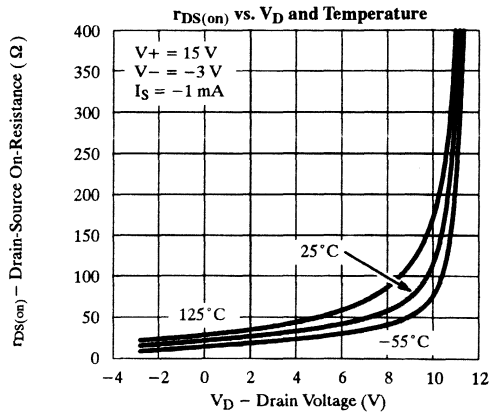
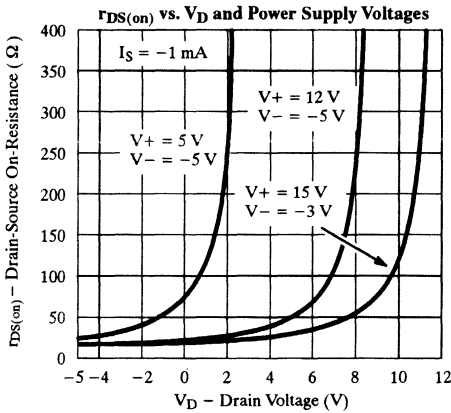
**Specifications<sup>a</sup> for Unipolar Supplies**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 4\text{ V}, 1\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		0	7	0	7	V
Switch On-Resistance	$r_{DS(on)}$	$I_S = -1\text{ mA}, V_D = 1\text{ V}$	Room	25		60		60	$\Omega$
<b>Dynamic Characteristics</b>									
Turn-On Time <sup>e</sup>	$t_{ON}$	$R_L = 300\ \Omega, C_L = 3\text{ pF}, V_S = 2\text{ V}$ See Test Circuit, Figure 2	Room	15		30		30	ns
Turn-Off Time <sup>e</sup>	$t_{OFF}$		Room	10		25		25	

**Notes:**

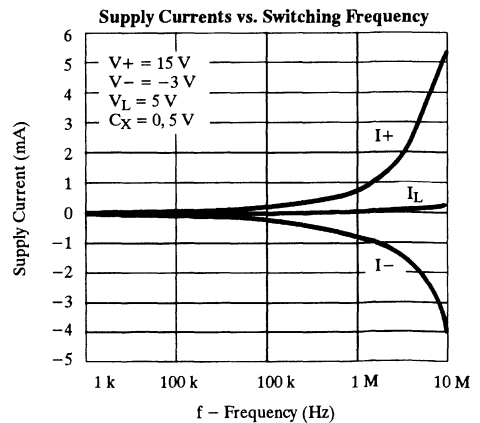
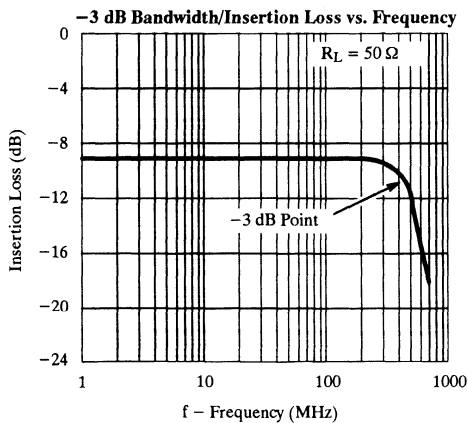
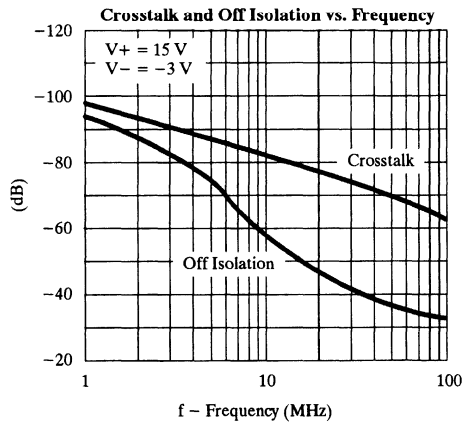
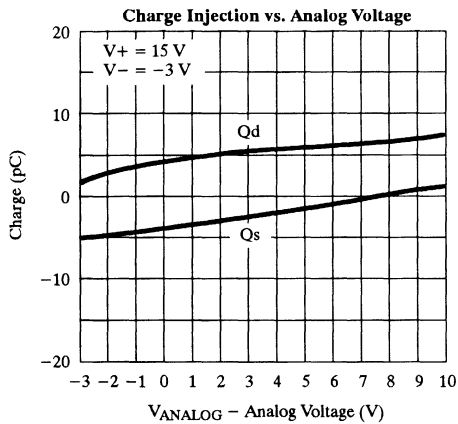
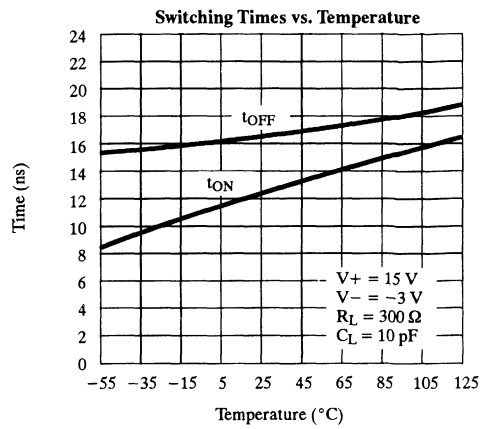
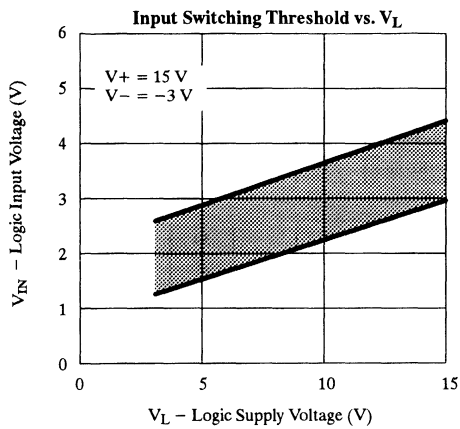
- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.
- g.  $\Delta Q = |Q \text{ at } V_S = 3\text{ V} - Q \text{ at } V_S = -3\text{ V}|$ .

**Typical Characteristics**



**1**

## Typical Characteristics (Cont'd)



**Schematic Diagram (Typical Channel)**

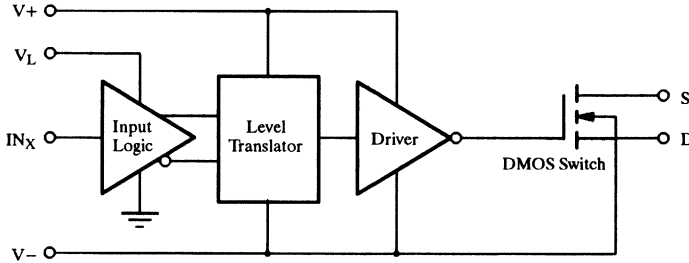
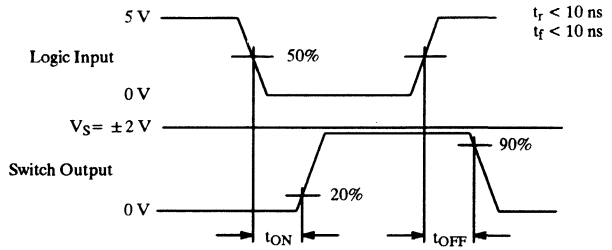
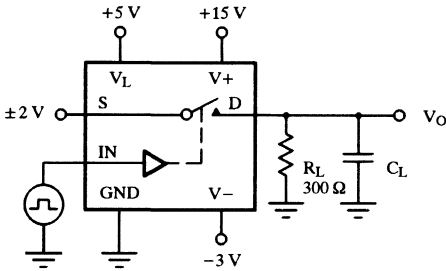


Figure 1.

**Test Circuits**



C<sub>L</sub> (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2. Switching Time

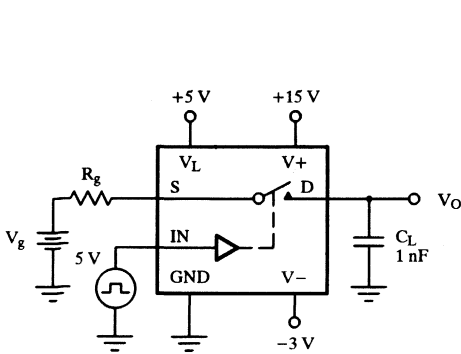
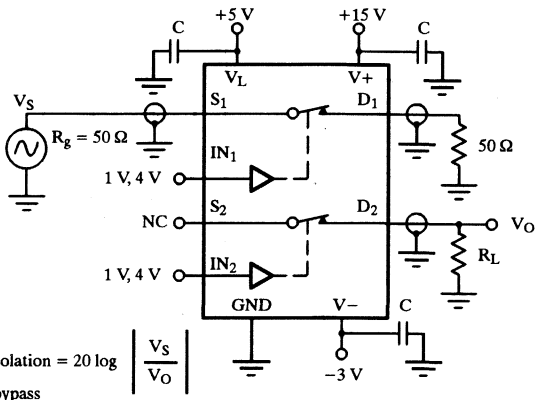


Figure 3. Charge Injection



$$X_{TALK} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Figure 4. Crosstalk

## Applications

### High-Speed Sample-and-Hold

In a fast sample-and-hold application, the analog switch characteristics are critical. A fast switch reduces aperture uncertainty. A low charge injection eliminates offset (step) errors. A low leakage reduces droop errors. The Si581, a fast input buffer, helps to shorten acquisition and settling

times. A low leakage, low dielectric absorption hold capacitor must be used. Polycarbonate, polystyrene and polypropylene are good choices. The JFET output buffer reduces droop due to its low input bias current. (See Figure 5.)

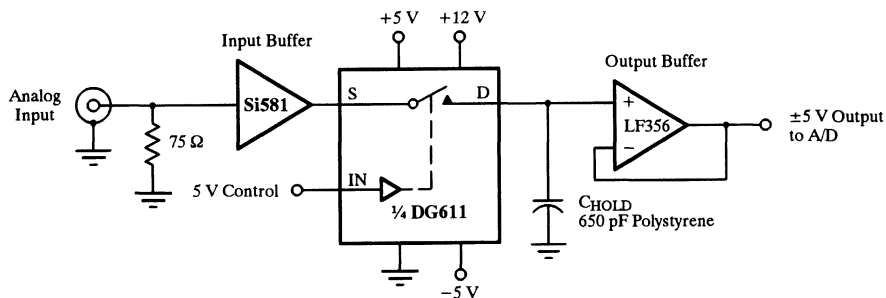


Figure 5. High-Speed Sample-and-Hold

### Pixel-Rate Switch

Windows, picture-in-picture, title overlays are economically generated using a high-speed analog switch such as the DG613. For this application the two video

sources must be synclocked. The glitch-less analog switch eliminates halos. (See Figure 6.)

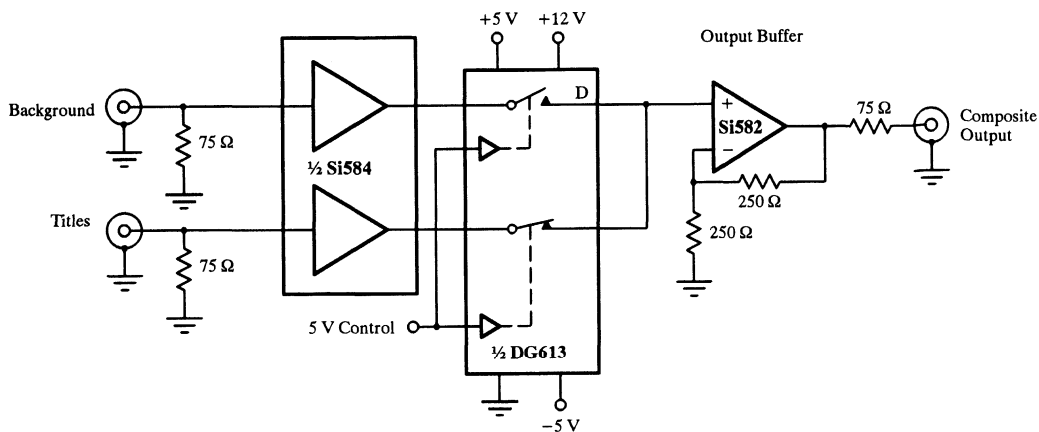


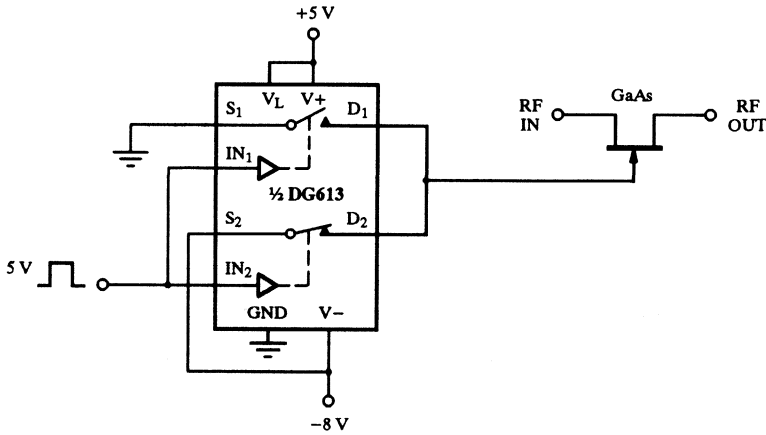
Figure 6. A Pixel-Rate Switch Creates Title Overlays

**Applications (Cont'd)**

**GaAs FET Drivers**

Figure 7 illustrates a high-speed GaAs FET driver. To turn the GaAs FET on 0 V are applied to its gate via S<sub>1</sub>, whereas to turn it off, -8 V are applied via S<sub>2</sub>. This high-speed,

low-power driver is especially suited for applications that require a large number of RF switches, such as phased array radars.



**Figure 7.** A High-Speed GaAs FET Driver that Saves Power

## Low On-Resistance Wideband/Video Switches

### Features

- Wide Bandwidth: 500 MHz
- Low Crosstalk at 5 MHz: -85 dB
- Low  $r_{DS(on)}$ : 5  $\Omega$ , DG642
- TTL Logic Compatible
- Fast Switching:  $t_{ON}$  50 ns
- Single Supply Compatibility
- High Current: 100 mA, DG642

### Benefits

- High Precision
- Improved Frequency Response
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Low Power Consumption

### Applications

- RF and Video Switching
- RGB Switching
- Video Routing
- Cellular Communications
- ATE
- Radar/FLIR Systems
- Satellite Receivers
- Programmable Filters

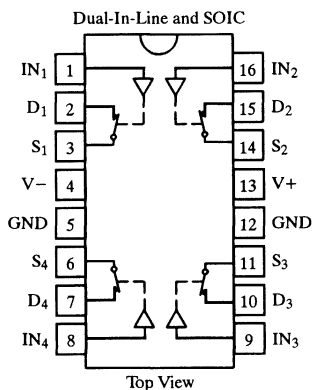
### Description

The DG641/642/643 are high performance monolithic video switches designed for switching wide bandwidth analog and digital signals. DG641 is a quad SPST, DG642 is a single SPDT, and DG643 is a dual SPDT function. These devices have exceptionally low on-resistances (5  $\Omega$  typ—DG642), low capacitance and high current handling capability.

To achieve TTL compatibility, low channel capacitances and fast switching times, the DG641/642/643 are built on the Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when on, and blocks up to 14  $V_{p-p}$  when off. An epitaxial layer prevents latchup.

### Functional Block Diagram and Pin Configuration

#### DG641



#### Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq$  0.8 V  
 Logic "1"  $\geq$  2.4 V

Switches Shown for Logic "1" Input

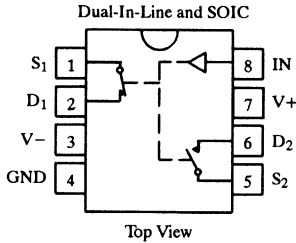
#### Ordering Information - DG641

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG641DJ
	16-Pin Narrow SOIC	DG641DY



## Functional Block Diagram and Pin Configuration

### DG642



**Truth Table**

Logic	SW <sub>1</sub>	SW <sub>2</sub>
0	OFF	ON
1	ON	OFF

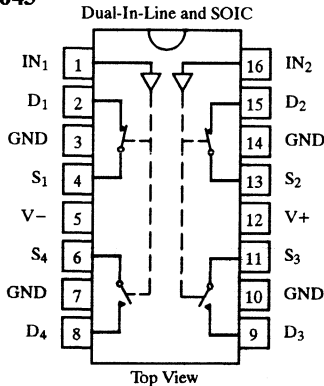
Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

#### Ordering Information – DG642

Temp Range	Package	Part Number
-40 to 85°C	8-Pin Plastic DIP	DG642DJ
	8-Pin Narrow SOIC	DG642DY

### DG643



**Truth Table**

Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V

Switches Shown for Logic "1" Input

#### Ordering Information – DG643

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG643DJ
	16-Pin Narrow SOIC	DG643DY

## Absolute Maximum Ratings

V+ to V-	-0.3 V to 21 V
V+ to GND	-0.3 V to 21 V
V- to GND	-19 V to +0.3 V
Digital Inputs	(V-) -0.3 V to (V+) +0.3 V or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub>	(V-) -0.3 V to (V-) +14 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal Except S or D)	20 mA
Continuous Current S or D: DG641/643	75 mA
DG642	100 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle max)	DG641/643 200 mA DG642 300 mA

Storage Temperature	-65 to 125°C
Power Dissipation (Package) <sup>b</sup>	
8-Pin Plastic DIP and Narrow SOIC <sup>c</sup>	300 mW
16-Pin Plastic DIP <sup>d</sup>	470 mW
16-Pin Narrow SOIC <sup>e</sup>	600 mW

#### Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 7.6 mW/°C above 75°C
- Derate 6 mW/°C above 75°C
- Derate 10 mW/°C above 75°C

## Specifications for DG641 and DG643

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}$ $V_{INH} = 2.4\text{ V}, V_{INL} = 0.8\text{ V}^e$	Temp <sup>a</sup>	Limits -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$	$V_- = -5\text{ V}, V_+ = 12\text{ V}$	Full	-5		8	V
		$V_- = \text{GND}, V_+ = 12\text{ V}$	Full	0		8	
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = 0\text{ V}$	Room Full		8	15 20	$\Omega$
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room		1	2	
Source Off Leakage Current	$I_{S(off)}$	$V_S = 0\text{ V}, V_D = 10\text{ V}$	Room Full	-10 -100	-0.02	10 100	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_S = 10\text{ V}, V_D = 0\text{ V}$	Room Full	-10 -100	-0.02	10 100	
Channel On Leakage Current	$I_{D(on)}$	$V_S = V_D = 0\text{ V}$	Room Full	-10 -100	-0.1	10 100	
<b>Digital Control</b>							
Input Voltage High	$V_{INH}$		Full	2.4			V
Input Voltage Low	$V_{INL}$		Full			0.8	
Input Current	$I_{IN}$	$V_{IN} = \text{GND}$ or $V_+$	Room Full	-1 -20	0.05	1 20	$\mu\text{A}$
<b>Dynamic Characteristics</b>							
On State Input Capacitance <sup>d</sup>	$C_{S(on)}$	$V_S = V_D = 0\text{ V}$	Room		10	20	pF
Off State Input Capacitance <sup>d</sup>	$C_{S(off)}$	$V_S = 0\text{ V}$	Room		4	12	
Off State Output Capacitance <sup>d</sup>	$C_{D(off)}$	$V_D = 0\text{ V}$	Room		4	12	
Bandwidth	BW	$R_L = 50\ \Omega$ , See Figure 6	Room		500		MHz
Turn On Time	$t_{ON}$	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ , See Figure 2	Room Full		50	70 140	ns
Turn Off Time	$t_{OFF}$		Room Full		28	50 85	
Charge Injection	Q	$C_L = 1000\text{ pF}, V_D = 0\text{ V}$ , See Figure 3	Room		-19		pC
Off Isolation	OIRR	$R_{IN} = 75\ \Omega, R_L = 75\ \Omega, f = 5\text{ MHz}$ See Figure 4	Room		-60		dB
All Hostile Crosstalk	$X_{TALK(AH)}$	$R_{IN} = 10\ \Omega, R_L = 75\ \Omega, f = 5\text{ MHz}$ See Figure 5	Room		-87		
<b>Power Supplies</b>							
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V}$ or $V_{IN} = 5\text{ V}$	Room Full		3.5	6 9	mA
Negative Supply Current	$I_-$		Room Full		-6 -9		

**Notes:**

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

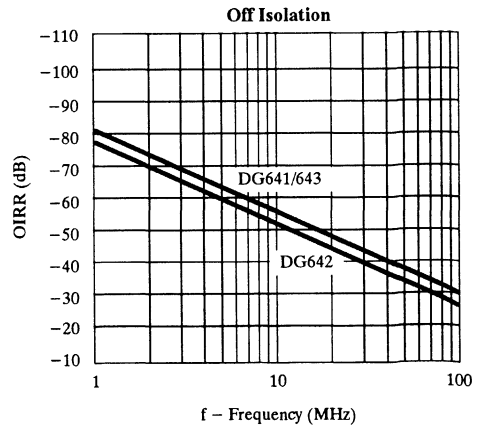
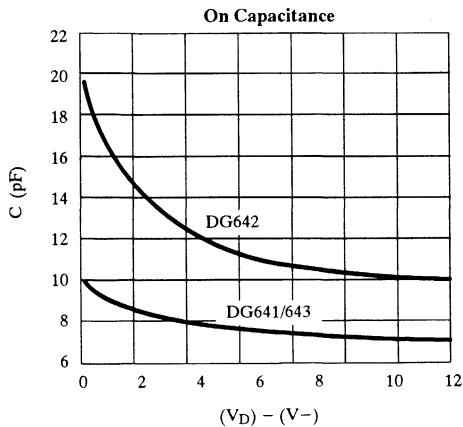
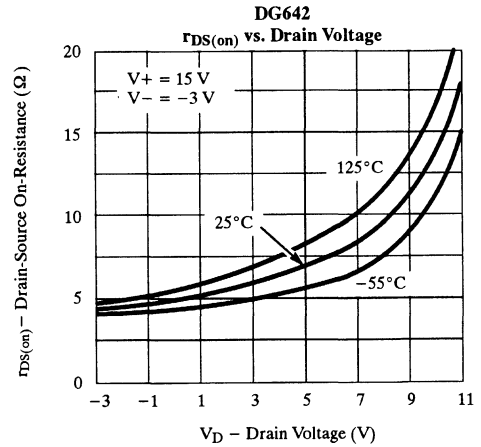
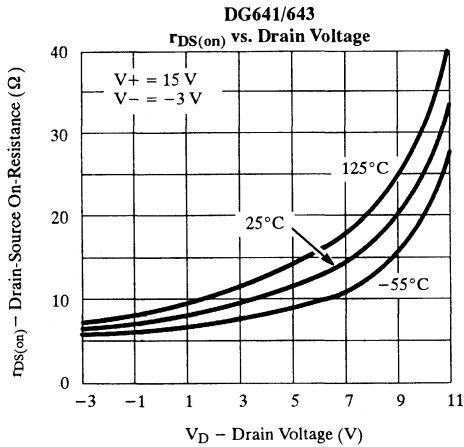
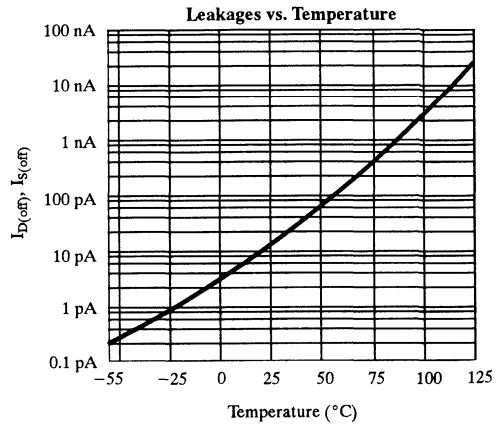
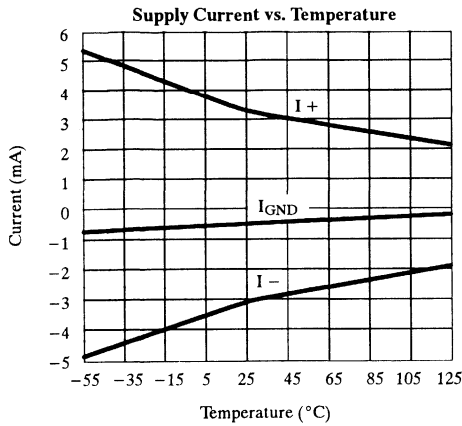
**Specifications for DG642**

Parameter	Symbol	Test Conditions Unless Otherwise Specified  V+ = 15 V, V- = -3 V VINH = 2.4 V, VINL = 0.8 V <sup>c</sup>	Temp <sup>a</sup>	Limits -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	VANALOG	V- = -5 V, V+ = 12 V	Full	-5		8	V
		V- = GND, V+ = 12 V	Full	0		8	
Drain-Source On-Resistance	rDS(on)	IS = -10 mA, VD = 0 V	Room		5	8	Ω
	Full				9		
rDS(on) Match	ΔrDS(on)		Room		0.5	1	
Source Off Leakage Current	IS(off)	VS = 0 V, VD = 10 V	Room	-10	-0.04	10	nA
	Full		Full	-200		200	
Drain Off Leakage Current	ID(off)	VS = 10 V, VD = 0V	Room	-10	-0.04	10	
	Full		Full	-200		200	
Channel On Leakage Current	ID(on)	VS = VD = 0 V	Room	-10	-0.2	10	
	Full		Full	-200		200	
<b>Digital Control</b>							
Input Voltage High	VINH		Full	2.4			V
Input Voltage Low	VINL		Full			0.8	
Input Current	IIN	VIN = GND or V+	Room	-1	0.05	1	μA
	Full		Full	-20		20	
<b>Dynamic Characteristics</b>							
On State Input Capacitance <sup>d</sup>	CS(on)	VS = VD = 0 V	Room		19	40	pF
Off State Input Capacitance <sup>d</sup>	CS(off)	VS = 0 V	Room		8	20	
Off State Output Capacitance <sup>d</sup>	CD(off)	VD = 0 V	Room		8	20	
Bandwidth	BW	RL = 50 Ω, See Figure 6	Room		500		MHz
Turn On Time	tON	RL = 1 kΩ, CL = 35 pF, See Figure 2	Room		60	100	ns
	Full				160		
Turn Off Time	tOFF		Room		40	60	
	Full		Full		100	100	
Charge Injection	Q	CL = 1000 pF, VD = 0 V, See Figure 3	Room		-40		pC
Off Isolation		RIN = 75 Ω, RL = 75 Ω, f = 5 MHz See Figure 4	Room		-63		dB
All Hostile Crosstalk	XTALK(AH)	RIN = 10 Ω, RL = 75 Ω, f = 5 MHz See Figure 5	Room		-85		
<b>Power Supplies</b>							
Positive Supply Current	I+	VIN = 0 V or VIN = 5 V	Room		3.5	6	mA
	Full				9		
Negative Supply Current	I-		Room	-6	-3		
	Full		Full	-9			

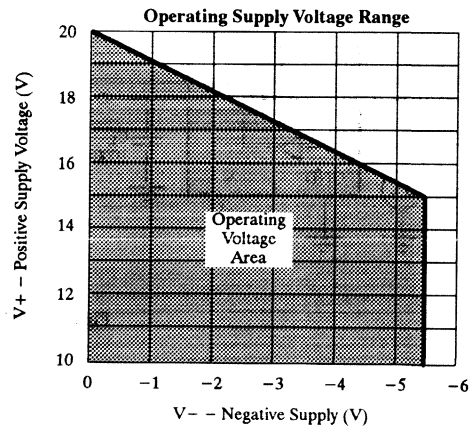
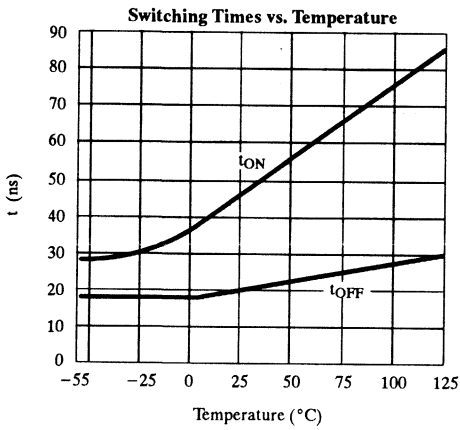
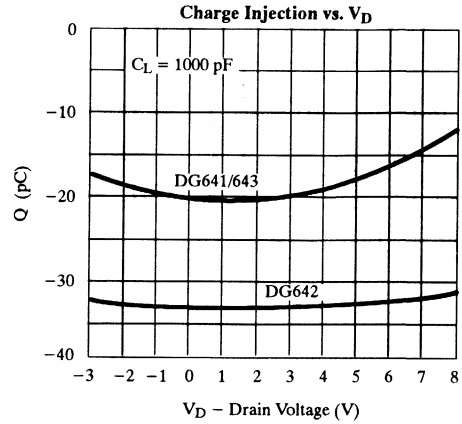
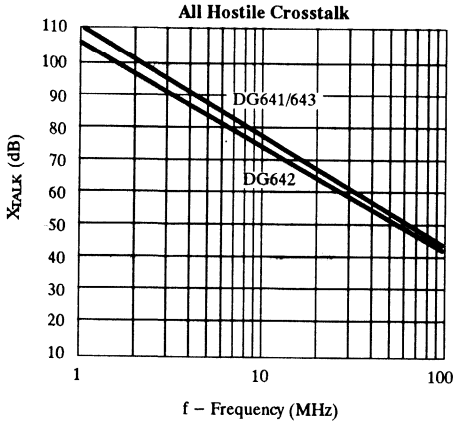
Notes:

- a. Room = 25°C, Full = as determined by the operating temperature suffix.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guaranteed by design, not subject to production test.
- e. VIN = input voltage to perform proper function.

## Typical Characteristics



## Typical Characteristics



## Schematic Diagram (Typical Channel)

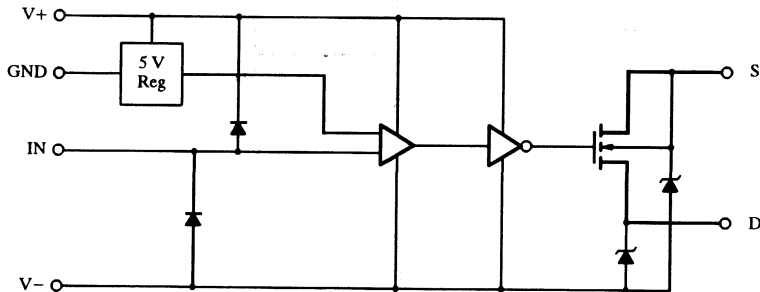


Figure 1.

## Test Circuits

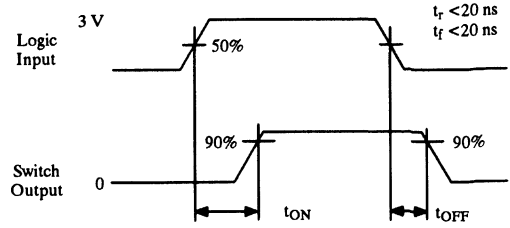
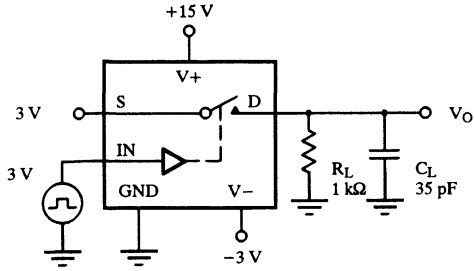
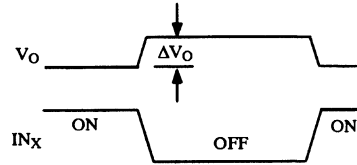
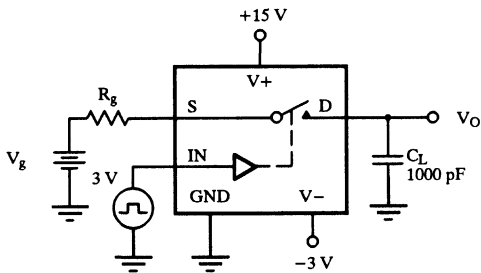


Figure 2. Switching Time



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

Figure 3. Charge Injection

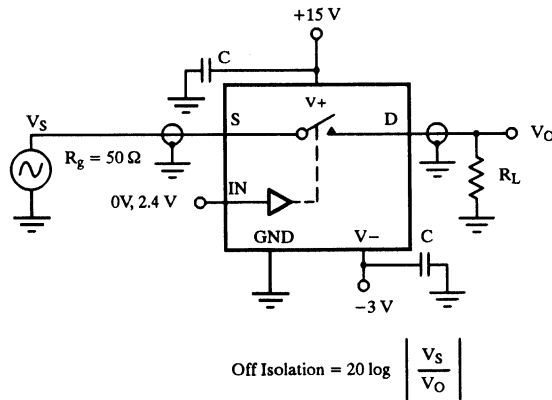
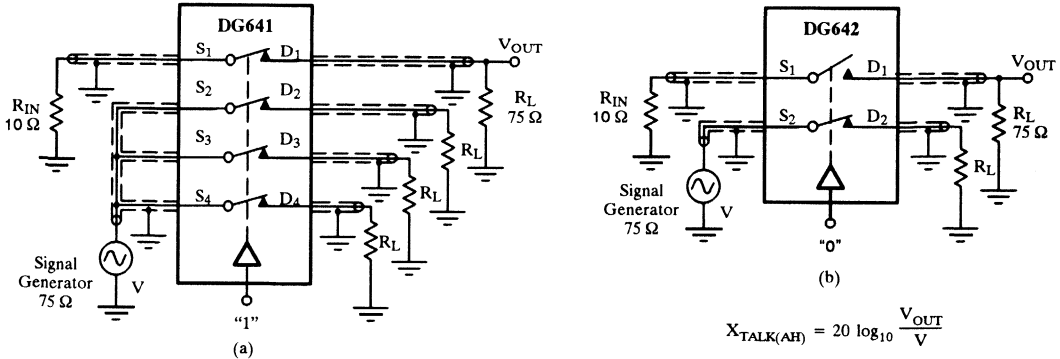
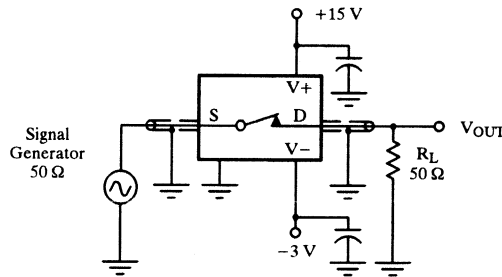


Figure 4. Off Isolation

**Test Circuits**



**Figure 5.** All Hostile Crosstalk – XTALK(AH)



**Figure 6.** Bandwidth

**Applications**

**Device Description**

The DG641/642/643 switches offer true bidirectional switching of high frequency analog or digital signals with minimum signal crosstalk, low insertion loss, and negligible non-linearity distortion and group delay.

Built on the Siliconix D/CMOS process, these switches provide excellent off-isolation with a bandwidth of around 500 MHz. The silicon-gate D/CMOS processing also yields fast switching speeds.

An on-chip regulator circuit maintains TTL input compatibility over the whole operating supply voltage range shown, easing control logic interfacing.

Circuit layout is facilitated by the interchangeability of source and drain terminals.

**Frequency Response**

A single switch on-channel exhibits both resistance [ $r_{DS(on)}$ ] and capacitance [ $C_{S(on)}$ ]. This RC combination has an attenuation effect on the analog signal – which is frequency dependent (like an RC low-pass filter). The –3 dB bandwidth of the DG641/642/643 is typically 500 MHz (into 50  $\Omega$ ).

## Applications (Cont'd)

### Power Supplies

Power supply flexibility is a useful feature of the DG641/642/643 series. It can be operated from a single positive supply (V+) if required (V- connected to ground).

Note that the analog signal must not exceed V- by more than -0.3 V to prevent forward biasing the substrate p-n junction. The use of a V- supply has a number of advantages:

1. It allows flexibility in analog signal handling, i.e., with V- = -5 V and V+ = 12 V; up to ±5-V ac signals can be controlled.
2. The value of on capacitance [ $C_{S(on)}$ ] may be reduced. A property known as 'the body-effect' on the DMOS switch devices causes various parametric effects to occur. One of these effects is the reduction in  $C_{S(on)}$  for an increasing V body-source. Note however that to increase V- normally requires V+ to be reduced (since V+ to V- = 21 V max.). A reduction in V+ causes an increase in  $r_{DS(on)}$ , hence a compromise has to be achieved. It is also useful to note that tests indicate that optimum video linearity performance (e.g., differential phase and gain) occurs when V- is around -3 V.
3. V- eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

### Decoupling

It is an established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG641/642/643 series is adversely affected by poor decoupling of power supply pins. Also, of even more significance, since the substrate of the device is connected to the negative supply, adequate decoupling of this pin is essential. Suitable decoupling capacitors are 1- to 10- $\mu$ F tantalum bead, plus 10- to 100-nF ceramic or polyester.

#### Rules:

1. Decoupling capacitors should be incorporated on all power supply pins (V+, V-). (See Figure 7).
2. They should be mounted as close as possible to the device pins.

3. Capacitors should be of a suitable type with good high frequency characteristics - tantalum bead and/or ceramic disc types are adequate.

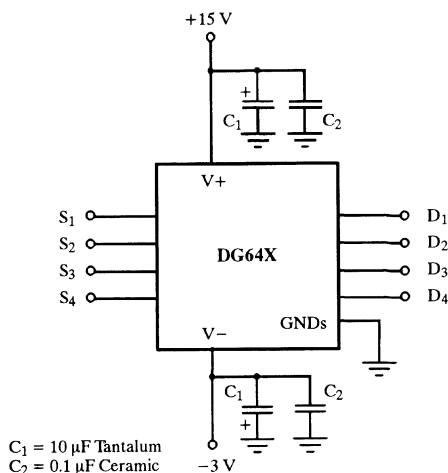


Figure 7. Supply Decoupling

### Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by these analog switches. Some tips for minimizing stray effects are:

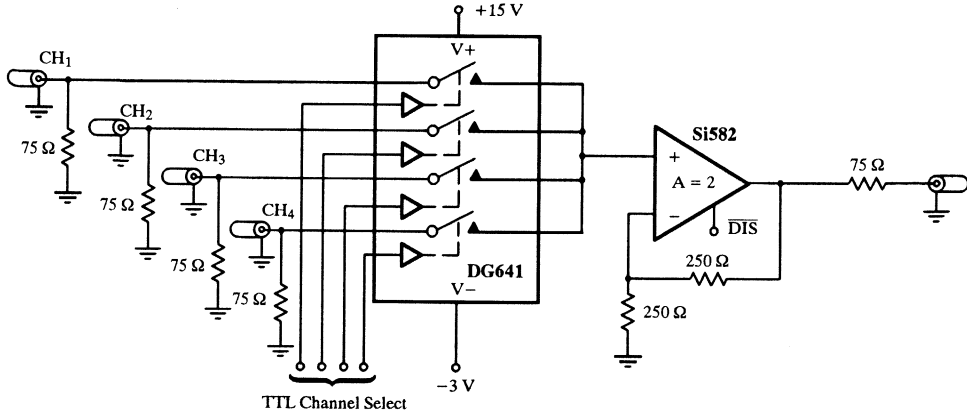
1. Use extensive ground planes on double sided PCB, separating adjacent signal paths. Multilayer PCB is even better.
2. Keep signal paths as short as practically possible, with all channel paths of near equal length.
3. Careful arrangement of ground connections is also very important. Star connected system grounds eliminate signal current, flowing through ground path parasitic resistance, from coupling between channels.

Figure 8 shows a 4-channel video multiplexer using a DG641.

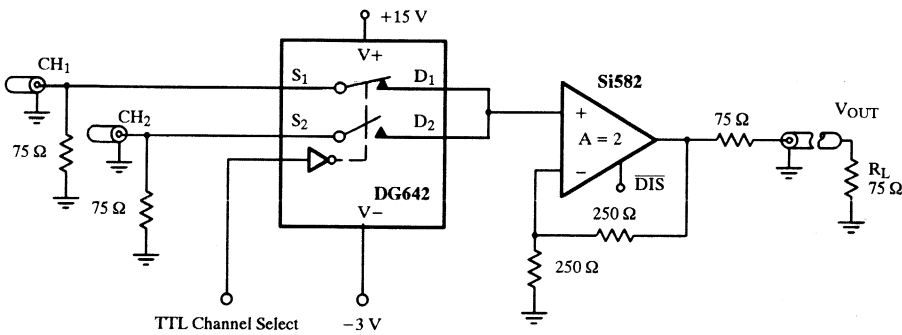
In Figure 9, two coax cables terminated on 75  $\Omega$  bring two video signals to the DG642 switch. The two drains tied together lower the on-state capacitance. An Si582 video amplifier drives a double terminated 75- $\Omega$  cable. The double terminated coax cable eliminates line reflections.



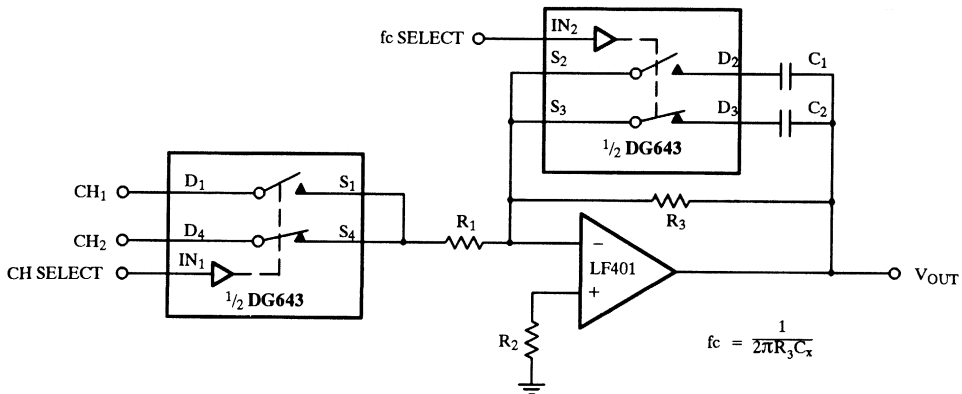
**Applications (Cont'd)**



**Figure 8.** 4 by 1 Video Multiplexing Using the DG641



**Figure 9.** 2-Channel Video Selector Using the DG642



**Figure 10.** Active Low Pass Filter with Selectable Inputs and Break Frequencies

## Monolithic General Purpose CMOS Analog Switch

### Features

- $\pm 15\text{-V}$  Input Range
- On-Resistance:  $< 50\ \Omega$
- Break-Before-Make Switching
- TTL and CMOS Compatible

### Benefits

- Improved Signal Headroom
- Reduced Switching Errors
- No Shorting of Inputs
- Simple Interfacing

### Applications

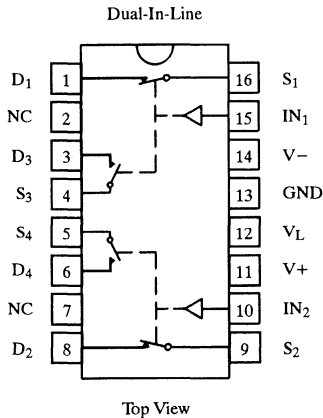
- Audio Switching
- Instrumentation
- Battery Powered Systems

### Description

The DG5043 solid state analog switch is recommended for general purpose applications in instrumentation, and process control. Built on the Siliconix PLUS-40 high voltage CMOS process, this device provides ease-of-use and performance advantages to the system designer. Key performance features of the DG5043 are 1- $\mu\text{s}$  switching,

low power supply requirements, and break-before-make switching. Each switch conducts equally well in either direction, when on, and blocks up to 30 V peak-to-peak when off. Off leakage current is 1-nA maximum. An epitaxial layer prevents latch up. For new designs, DG403 is recommended.

### Functional Block Diagram and Pin Configuration



Truth Table

Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0" =  $\leq 0.8\ \text{V}$   
Logic "1" =  $\geq 2\ \text{V}$   
Switches shown for Logic "1" input.

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG5043CJ

### Absolute Maximum Ratings

V <sub>+</sub> to V <sub>-</sub>	44 V
GND to V <sub>-</sub>	25 V
V <sub>L</sub>	(GND - 0.3 V) to 44 V
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>	(V <sub>-</sub> ) -2 V to (V <sub>+</sub> plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous	30 mA
Current, S or D (Pulsed 1 ms 10% duty)	100 mA
Storage Temperature	-65 to 125°C

### Power Dissipation (Package)<sup>b</sup>

16-Pin Plastic DIP <sup>c</sup>	470 mW
---------------------------------	--------

### Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C

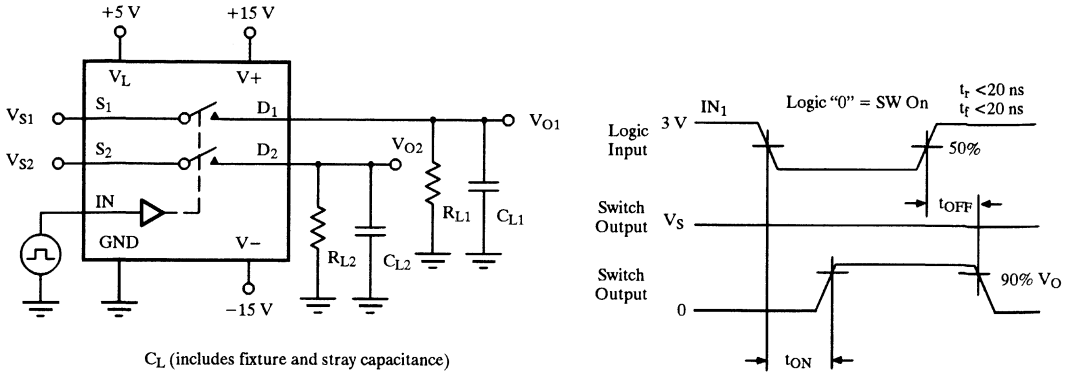
**Specifications**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2\text{ V}, 0.8\text{ V}^e$	Temp <sup>a</sup>	C Suffix 0 to 70°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$		Full	-15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = \pm 10\text{ V}$	Room Full			50 75	$\Omega$
Switch Off Leakage Current	$I_{S(off)}$	$V_S = V_D = 14\text{ V}$	Room Full	-1 -100		1 100	nA
		$V_S = V_D = -14\text{ V}$	Room Full	-1 -100		1 100	
Channel On Leakage Current	$I_{D(on)}$	$V_S = V_D = 14\text{ V}$	Room Full			2 200	nA
		$V_S = V_D = -14\text{ V}$	Room Full	-2 -200			
<b>Digital Control</b>							
Input Current with $V_{IN}$ Low	$I_{IL}$	$V_{IN}$ Under Test = 0.8 V	Full	-1		1	$\mu\text{A}$
Input Current with $V_{IN}$ High	$I_{IH}$	$V_{IN}$ Under Test = 2 V	Full	-1		1	
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	$V_S = \pm 10\text{ V}, R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ See Figure 1	Room			1200	ns
Turn-Off Time	$t_{OFF}$		Room			700	
Charge Injection <sup>d</sup>	Q	$C_L = 10\text{ nF}, V_{gen} = 0\text{ V}, R_{gen} = 0\text{ }\Omega$	Room		30		pC
Off Isolation <sup>d</sup>	OIRR	$R_L = 75\text{ }\Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room		75		dB
Crosstalk (Channel-to-Channel) <sup>d</sup>	$X_{TALK}$	$R_L = 75\text{ }\Omega, V_S = 2\text{ V}_{P-P}, f = 1\text{ MHz}$	Room		89		
Source Off Capacitance	$C_{S(off)}$	$V_D = V_S = 0\text{ V}, f = 1\text{ MHz}$	Room		15		pF
Drain Off Capacitance <sup>d</sup>	$C_{D(off)}$		Room		17		
Channel On Capacitance <sup>d</sup>	$C_{D(on)}$		Room		45		
<b>Power Supplies</b>							
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ or }2.4\text{ V}$	Full			300	$\mu\text{A}$
Negative Supply Current	$I_-$		Full	-300			
Logic Supply Current	$I_L$	$V_{IN} = 0\text{ or }2.4\text{ V}$	Full			300	
Ground Current	$I_{GND}$		Full	-300			

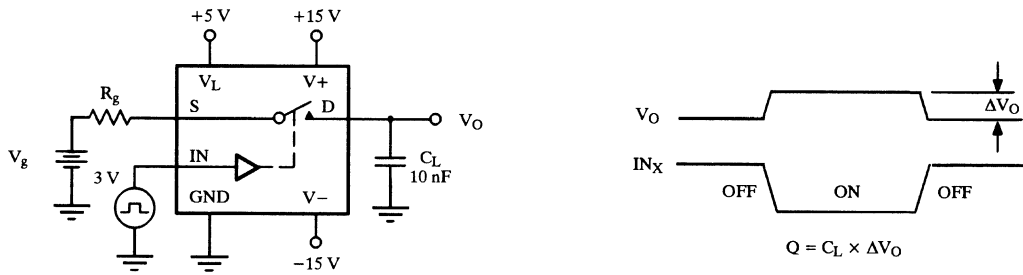
Notes:

- a. Room = 25°C, Full = as determined by the operating temperature suffix.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guaranteed by design, not subject to production test.
- e.  $V_{IN}$  = input voltage to perform proper function.

## Test Circuits



**Figure 1.** Switching Time



**Figure 2.** Charge Injection

# Low-Power, High-Speed CMOS Analog Switch

## Features

- $\pm 15\text{-V}$  Input Range
- On-Resistance:  $50\ \Omega$
- Fast Switching Action— $t_{ON}$ : 100 ns
- Low Power— $P_D$ :  $<350\ \mu\text{W}$
- TTL and CMOS Compatible

## Benefits

- Improved Signal Headroom
- Low Signal Errors
- Break-Before-Make Switching Action
- Reduced Power Consumption
- Simple Interfacing

## Applications

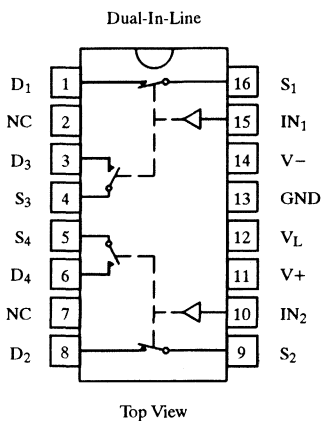
- Audio Switching
- Precision Switching
- High-Speed Switching
- Battery Powered Systems

## Description

The DG5143 solid state analog switch is built on the Siliconix proprietary high-voltage silicon gate process to achieve high voltage rating and superior switch time on/off performance. Break-before-make switching action guarantees that an on-channel will be turned off before the off-channel can turn on. The DG5143 features ultra-low power supply requirements and TTL and CMOS compatibility.

Each switch conducts equally well in both directions when on and blocks input voltages to the supply values when off. This switch is ideal for battery powered industrial applications with a maximum power supply current of  $1\ \mu\text{A}$ . An epitaxial layer prevents latchup.

## Functional Block Diagram and Pin Configuration



Truth Table

Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8\ \text{V}$   
Logic "1"  $\geq 2.4\ \text{V}$

Switches Shown for Logic "1" Input

Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG5143CJ

## Absolute Maximum Ratings

(V+) - (V-)	< 36 V
(V+) - (V <sub>D</sub> ) <sup>a</sup>	< 30 V
(V <sub>D</sub> ) - (V-) <sup>a</sup>	< 30 V
(V <sub>D</sub> ) - (V <sub>S</sub> ) <sup>a</sup>	< ±22 V
(V <sub>L</sub> ) - (V-)	< 33 V
(V <sub>L</sub> ) - (V <sub>IN</sub> )	< 30 V
V <sub>L</sub>	< 20 V
V <sub>IN</sub> <sup>a</sup>	< 20 V

Continuous Current, Any Terminal	30 mA
Peak Current, S or D (pulsed a 1 ms, 10% duty cycle max)	100 mA
Storage Temperature	-65 to 125°
Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP	450 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.

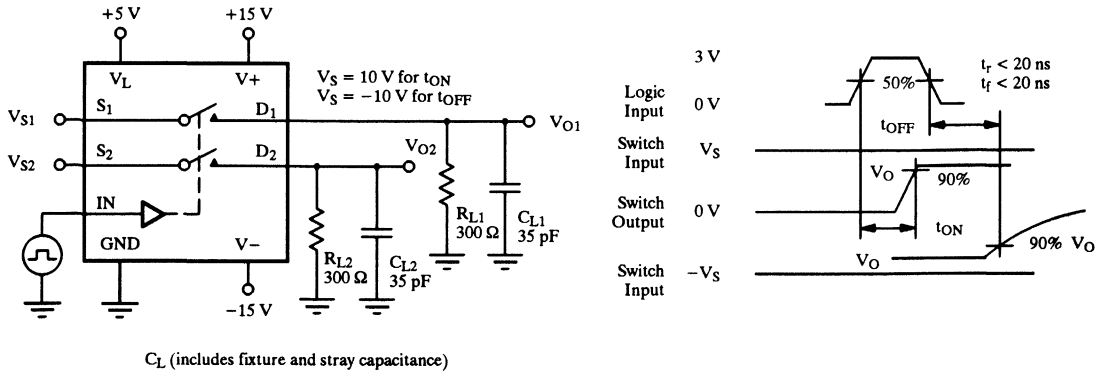
## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V, V <sub>L</sub> = 5 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	Temp <sup>a</sup>	C Suffix 0 to 70°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	-15		15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = -10 mA	Room Full			75 100	Ω
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>D</sub> = ∓10 V, V <sub>S</sub> = ±10 V	Room Full	-5 -20		5 20	nA
	I <sub>D(off)</sub>		Room Full	-5 -20		5 20	
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = -10 to 10 V	Room Full	-2 -40		2 40	
<b>Digital Control</b>							
Input Current with V <sub>IN</sub> Low	I <sub>IL</sub>		Full	-1		1	μA
Input Current with V <sub>IN</sub> High	I <sub>IH</sub>		Full	-1		1	
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF See Figure 1	Room			175	ns
Turn-Off Time	t <sub>OFF</sub>		Room			150	
Break-Before-Make	t <sub>ON</sub> - t <sub>OFF</sub>		Room			5	
Charge Injection <sup>d</sup>	Q	C <sub>L</sub> = 10,000 pF, V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	Room			150	pC
Off Isolation <sup>d</sup>	OIRR	R <sub>L</sub> = 100 Ω, C <sub>L</sub> ≤ 5 pF, f = 1 MHz	Room	-50			
Channel-to-Channel Crosstalk <sup>d</sup>	X <sub>TALK</sub>	Any Other Channel Switches R <sub>L</sub> = 100 Ω, C <sub>L</sub> ≤ 5 pF, f = 1 MHz	Room			-50	dB
<b>Power Supplies</b>							
Positive Supply Current	I+	V <sub>IN</sub> = 0 V or 5 V Switch Duty Cycle <10%	Room			10	μA
Negative Supply Current	I-		Room	-10			
Logic Supply Current	I <sub>L</sub>		Room			10	
Ground Current	I <sub>GND</sub>		Room	-10			

Notes:

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

**Test Circuits**



**Figure 1.** Switching Time





<b>General Information</b>	<b>1</b>
<b>    Analog Switches</b>	<b>1</b>
<b>    Analog Multiplexers</b>	<b>2</b>
<b>Wideband/Video Amplifiers</b>	<b>3</b>
<b>    Voltage Converters</b>	<b>4</b>
<b>    Appendix</b>	<b>5</b>
<b>Worldwide Sales Offices and Distributors</b>	<b>6</b>

## About Analog Multiplexers

Analog multiplexers represent a higher level of integration than analog switches. They have many (4, 8, 16, or more) inputs with only one or two common outputs. Multiplexers are used where it is necessary to transfer information from many input channels to a common output, most often when only one transmission line is available for all data transfer between various points. The transmitted signals are in either analog or digital form. Siliconix multiplexers handle analog signals, passing bipolar voltages or currents, which are often obtained from transducers. The analog signals represent physical phenomena such as temperature, pressure, velocity, and flow speech. Typical applications include data acquisition, industrial process control, aircraft systems monitoring, medical electronics, telemetry, and telecommunications.

### Differential vs. Single-Ended Multiplexing

When is it better to select a differential multiplexer versus a single-ended configuration? Figures 1 and 2 demonstrate both options. Single-ended multiplexing, as shown in Figure 1, applies to systems that have signal sources which are close to full-scale range and referenced to a common point (usually ground). Another case is where different signal sources with small signal amplitude (mV range) are generated by transducers. Instrumentation amplifiers can be used to precondition the signals and provide a common reference. This step reduces feedthrough errors and losses while tailoring each signal source to a desired voltage (or current) to obtain the maximum resolution available in an A/D or D/A converter or other device driven by the multiplexers.

Differential multiplexing (Figure 2) is utilized for low-level switching and in noisy environments. It can tolerate switching transients or some mismatch without a significant degradation of signal accuracy. Major considerations are switch matching ( $r_{DS(on)}$ ,  $I_{(off)}$ , and capacitance), common-mode rejection, and the system's tolerance to switching transients introduced by the break-before-make switching sequence.

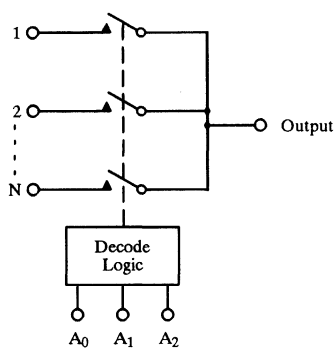


Figure 1. Single-Ended Multiplexing

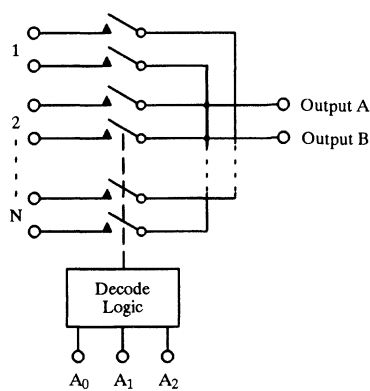


Figure 2. Differential Multiplexing

The DG4XX series of Siliconix multiplexers is designed to reduce switching errors, glitching, and power consumption while providing improved data throughput and increased ruggedness. For data acquisition, hi-rel, and battery operated systems, the rugged DG406/407 and DG408/409 multiplexers are the answer for designs requiring low on-resistance, low charge injection, fast transition time, and single-supply capability.

Other DG4XX family members include the DG428 and DG429, which have on-chip address and control latches to simplify design in microprocessor-based applications, as well as the DG485 octal analog switch array for low-power multiplexing in serial control applications.

## D/CMOS Wideband/Video Multiplexers

The DG535 and DG536 are 16-channel wideband/video multiplexers which use the Siliconix D/CMOS process to combine wideband DMOS “T” switches with high-density, high-speed CMOS logic and switch drivers to form monolithic wideband/video multiplexing systems. These devices include on-board latches to hold the address selection data and all of the necessary control logic to facilitate connection into larger arrays, matrices, and multiplexers. The DG534 and DG538 are 4- and 8- channel wideband/video multiplexers which, like the DG535 and DG536, feature address latches and control logic with the addition of data feedback and TTL compatibility. They make excellent wideband/video crosspoints, routers, and multiplexers, reducing board space, power dissipation, component count, and cost, while simplifying system design and improving reliability.

For detailed information on these products, please refer to the individual data sheets and to application notes AN501 and AN502.

## Crosspoints

The DG884 is the first monolithic wideband/video crosspoint switch available for commercial use. Any of eight video inputs can simultaneously be routed to any of our outputs. This highly integrated device offers a major reduction of the physical size and component count needed to implement a video switching matrix. The DG884 uses double-diffused DMOS switching elements to maintain low capacitance and low levels of crosstalk among signal paths.

Double-diffused CMOS latches, chip select, reset, readback, and disable functions are all included on the chip to ease system design, save power, and improve system reliability.

## Factors Affecting Systems Performance

In any multiplexer application, the following factors should be considered:

1. **System Attenuation:** Includes loss in the analog signal caused by the multiplexer and the transmission path. This is a frequency dependent factor.
2. **Channel Isolation:** At low frequencies, this is principally a function of channel off-leakage currents, and at high frequencies, it is a function of device and system capacitance.
3. **Crosstalk:** There are several sources of crosstalk, including overlap between switching channels, off-switch capacitance, inter-switch capacitance, stray circuit capacitance, and distortion in the transmission medium.

4. **Noise:** There are several sources of noise, including thermal or Johnson noise generated in any resistance components, crosstalk, leakages, switching transients, as well as thermal EMFs and transmission path pick up.
5. **Switching Rate:** This is important in sampling system where it determines the maximum bandwidth frequency of the multiplexers (via the sampling theorem) and defines crosstalk errors.
6. **Settling Time:** Although settling time is a function for the source and load impedances, the multiplexer's contribution is directly related to the  $t_{DS(on)} \times C_{S(on)}$  time constant and to the charge injection of the multiplexer.

## Glossary of Terms

### Bandwidth

The "3 dB down" point of the frequency response characteristic.

### Crosspoint Switch

A two-dimensional array of analog switches or analog multiplexers that allows for the routing of signals from any input to any output.

### Crosstalk

A measure of how much of an unwanted signal appears on a given analog channel due to spurious capacitive or inductive coupling from another channel.

### D/CMOS

Semiconductor process that combines DMOS FETs and CMOS logic on a monolithic chip.

### Differential Gain

Expressed as a percentage, this is a form of distortion that appears as changes in the amplitude of the chrominance (color) signal as a function of luminance (brightness) amplitude.

### Differential Multiplexer

An analog multiplexer that selects both the high and the low side of each signal. It can be thought of as two single-ended multiplexers operating in tandem.

### Differential Phase

Measured in degrees, this is the phase shift of the color subcarrier resulting from changes in luminance level.

### DMOS (Double-Diffused MOS)

A type of field-effect transistor featuring low on-resistance and low capacitance.

### Input Capacitance

The capacitive load that the input terminal of an analog switch presents to the signal source. It is specified for two conditions, with the switch on or off.

### **Insertion Loss**

Expressed in dB, this is a measure of the signal loss caused by the impedance of the analog switch at a given frequency.

### **Off-Isolation**

A measure of how much of the signal applied to an “open” switch appears at its output due to parasitic components such as gate-to-channel capacitance and lead inductance.

### **On-resistance**

The dc input-to-output resistance of an analog switch channel when the switch is turned on.

### **Output Capacitance**

The capacitive load that the output of an off switch adds to the output node.

### **PLCC Package (Plastic Leaded Chip Carrier)**

A surface-mount package characterized for its small size and reliable lead-to-printed circuit board mechanical interface

### **Readback**

A feature that allows for the inspection of the control latch contents in a multiplexer or crosspoint switch.

### **Single-Ended Multiplexer**

An array of analog switches that selects one of several analog input signals.

### **“T” Switch**

An analog switch configuration consisting of two series switches and a shunt switch to ground. It is used to improve dramatically the off-isolation of the array.

### **Video Amplifier**

An amplifier, typically with a gain of 2, which is normally used at the output of a video multiplexer or crosspoint to drive a length of double-terminated coaxial cable.

### **Video Buffer**

A current amplifier that is used is to preserve signal quality by eliminating the capacitive loading effect to several video multiplexer inputs on a common signal source. This is normally a unity gain buffer.

### **Wideband**

A relative term that is used in this book to refer to a frequency spectrum that is more than 2 MHz wide.

# Analog Multiplexer Selector Guide

Functional Configuration	Part No.	Max $r_{DS(on)}$ ( $\Omega$ )	Max $I_{S(on)}$ (mA)	Analog Range (V)	Transition Time (ns)	Typical Charge Injection (pC)	On-Chip Logic Regulator	Max Power Consumption (mW)	Package	Comments	Page
2-Channel Differential	DG534A	90	20	-5 to 10	0.3	-70	-	59.5	J, N, P	Video, Latches	2-86
	DG534A	90	20	-5 to 10	0.3	-70	-	59.5	J, N, P	Video, Latches	2-86
	DG538A	90	20	-5 to 10	0.3	-70	-	59.5	J, N, P	Video, Latches	2-86
4-Channel Differential	DG409	100	1	$\pm 15$	0.25	20	Yes	0.9	J, K, Y, Z	High Speed	2-11
	DG429	100	1	$\pm 15$	0.25	4	Yes	1.58	J, K, N	Latchable, High Speed	2-22
	DG509A	400	10	$\pm 15$	1.0	20	Yes	58.5	J, K, Y	-	2-60
	DG529	400	10	$\pm 15$	1.0	4	Yes	60	J, K	Latchable	2-70
	DG459	1200	2	-9.5 to 10	0.5	-	Yes	3	J, K, Z	Fault Protected	2-34
8-Channel Single-Ended	DG538A	90	20	-5 to 10	0.3	-70	-	59.5	J, N, P	Video, Latches	2-86
	DG408	100	1	$\pm 15$	0.2	20	Yes	0.9	J, K, Y	High Speed	2-11
	DG428	100	1	$\pm 15$	0.25	4	Yes	1.58	J, K, N	Latchable, High Speed	2-22
	DG508A	400	10	$\pm 15$	1.0	20	Yes	59.5	J, K, Y, Z	-	2-60
	DG528	400	10	$\pm 15$	1.0	4	Yes	60	J, K	Latchable	2-70
8-Channel Differential	DG458	1200	2	-9.5 to 10	0.5	-	Yes	3	J, K, Z	Fault Protected	2-34
	DG407	100	1	$\pm 15$	0.3	15	Yes	0.5	J, K, N, Z	High Speed	2-1
16-Channel Single-Ended	DG507A	400	5	$\pm 15$	1.0	20	Yes	58.5	J, K, R	-	2-52
	DG535	90	10	0 to 10	0.3	-35	-	0.75	J, P	Low Power, Video	2-102
	DG536	90	10	0 to 10	0.3	-35	-	0.75	M, N	Low Power, Video	2-102
	DG406	100	1	$\pm 15$	0.3	20	Yes	0.47	J, K, N, Z	Low Power, Fast	2-1
	DG506A	400	10	$\pm 15$	1.0	20	Yes	58.5	J, K, N, R, Z	-	2-52
Specials	DG485	85	20	$\pm 15$	0.2	17	-	0.11	J, N, Z	8-Ch, Serial Control	2-42
	DG884	90	20	-5 to 8	0.3	-100	-	92.5	M, N	8x4 Video Crosspoint	2-113
	DG894	100	10	-5 to 8	0.2	-	Yes	136	J, W	RGB Video Mux	2-126

P = Sidebrake

N = PLCC  
Z = LCC

M = CLCC  
Y = SOIC

K = CerDIP  
W = SOIC Wide-Body

J = Plastic DIP  
R = Sidebrake

# 16-Channel/Dual 8-Channel High Performance CMOS Analog Multiplexers

## Features

- Low On-Resistance— $r_{DS(on)}$ : 50  $\Omega$
- Low Charge Injection— $Q$ : 15 pC
- Fast Transition Time— $t_{TRANS}$ : 200 ns
- Low Power: 0.2 mW
- Single Supply Capability
- 44-V Supply Max Rating

## Benefits

- Higher Accuracy
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness
- Superior to DG506/507A
- Wide Supply Ranges:  $\pm 5$  V to  $\pm 20$  V

## Applications

- Data Acquisition Systems
- Audio Signal Routing
- Medical Instrumentation
- ATE Systems
- Battery Powered Systems
- High-Rel Systems
- Single Supply Systems

## Description

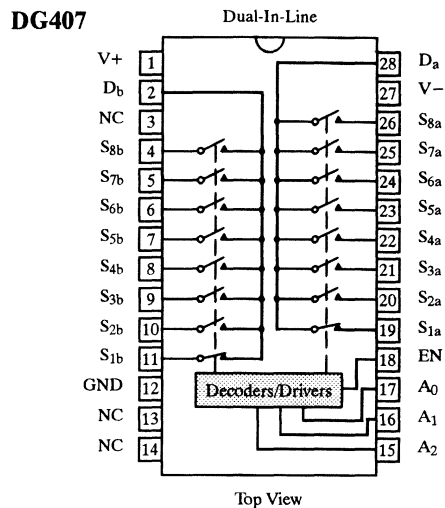
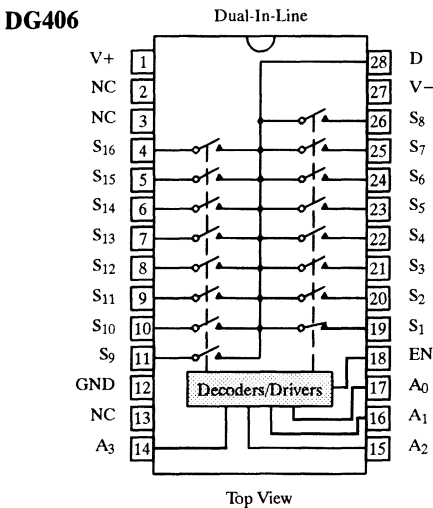
The DG406 is a 16-channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. The DG407 selects one of eight differential inputs to a common differential output. Break-before-make switching action protects against momentary shorting of inputs.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address ( $A_x$ ) and enable (EN) are TTL compatible over the full specified operating temperature range.

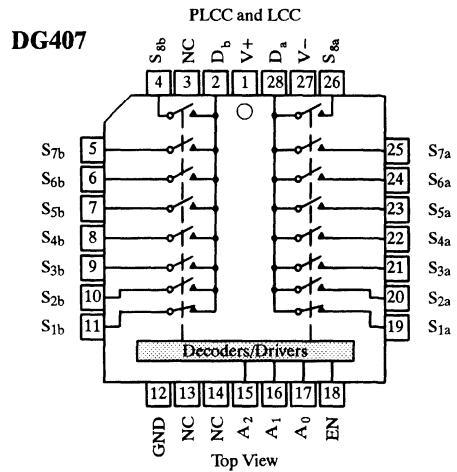
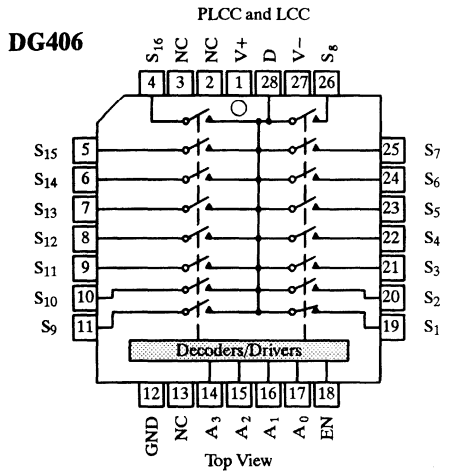
Applications for the DG406/407 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications. For additional application information, see application note AN206.

Designed in the 44-V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts, allowing operation with  $\pm 20$ -V supplies. Additionally single (12-V) supply operation is allowed. An epitaxial layer prevents latchup.

## Functional Block Diagrams and Pin Configurations



## Functional Block Diagrams and Pin Configurations (Cont'd)



Truth Table — DG406

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Ordering Information — DG406

Temp Range	Package	Part Number
-40 to 85°C	28-Pin Plastic DIP	DG406DJ
	28-Pin PLCC	DG406DN
-55 to 125°C	28-Pin CerDIP	DG406AK/883
	LCC-28	DG406AZ/883

Truth Table — DG407

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" =  $V_{AL} \leq 0.8\text{ V}$   
 Logic "1" =  $V_{AH} \geq 2.4\text{ V}$   
 X = Don't Care

Ordering Information — DG407

Temp Range	Package	Part Number
-40 to 85°C	28-Pin Plastic DIP	DG407DJ
	28-Pin PLCC	DG407DN
-55 to 125°C	28-Pin CerDIP	DG407AK/883
	LCC-28	DG407AZ/883



**Absolute Maximum Ratings**

Voltages Referenced to V-  
 V+ ..... 44 V  
 GND ..... 25 V  
 Digital Inputs<sup>a</sup>, V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first  
 Current (Any Terminal) ..... 30 mA  
 Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max) ..... 100 mA  
 Storage Temperature (AK, AZ Suffix) ..... -65 to 150°C (DJ, DN Suffix) ..... -65 to 125°C

Power Dissipation (Package)<sup>b</sup>  
 28-Pin Plastic DIP<sup>c</sup> ..... 625 mW  
 28-Pin CerDIP<sup>d</sup> ..... 1.2 W  
 28-Pin Plastic PLCC<sup>e</sup> ..... 450 mW  
 LCC-28<sup>e</sup> ..... 1.35 W

- Notes:  
 a. Signals on S<sub>X</sub>, D<sub>X</sub> or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.  
 b. All leads soldered or welded to PC board.  
 c. Derate 6 mW/°C above 75°C  
 d. Derate 12 mW/°C above 75°C  
 e. Derate 13.5 mW/°C above 75°C

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>AL</sub> = 0.8 V, V <sub>AH</sub> = 2.4 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V	
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = -10 mA Sequence Each Switch On	Room Full	50		100 125		100 125	Ω	
r <sub>DS(on)</sub> Matching Between Channels <sup>g</sup>	Δr <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V	Room	5					%	
Source Off Leakage Current	I <sub>S(off)</sub>		Room Full	0.01	-0.5 -50	0.5 50	-0.5 -5	0.5 5		
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>EN</sub> = 0 V V <sub>D</sub> = ±10 V, V <sub>S</sub> = ∓10 V	DG406	Room Full	0.04	-1 -200	1 200	-1 -40	1 40	nA
			DG407	Room Full	0.04	-1 -100	1 100	-1 -20	1 20	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = ±10 V Sequence Each Switch On	DG406	Room Full	0.04	-1 -200	1 200	-1 -40	1 40	nA
			DG407	Room Full	0.04	-1 -100	1 100	-1 -20	1 20	
<b>Digital Control</b>										
Logic High Input Voltage	V <sub>INH</sub>		Full		2.4		2.4		V	
Logic Low Input Voltage	V <sub>INL</sub>		Full			0.8	0.8			
Logic High Input Current	I <sub>AH</sub>	V <sub>A</sub> = 2.4 V, 15 V	Full		-1	1	-1	1	μA	
Logic Low Input Current	I <sub>AL</sub>	V <sub>EN</sub> = 0 V, 2.4 V, V <sub>A</sub> = 0 V	Full		-1	1	-1	1		
Logic Input Capacitance	C <sub>in</sub>	f = 1 MHz	Room	7					pF	
<b>Dynamic Characteristics</b>										
Transition Time	t <sub>TRANS</sub>	See Figure 2	Room Full	200		300 400		300 400	ns	
Break-Before-Make Interval	t <sub>OPEN</sub>	See Figure 4	Room Full	50	25 10		25 10			
Enable Turn-On Time	t <sub>ON(EN)</sub>	See Figure 3	Room Full	150		200 400		200 400		
Enable Turn-Off Time	t <sub>OFF(EN)</sub>		Room Full	70		150 300		150 300		
Charge Injection	Q	C <sub>L</sub> = 1 nF, V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω	Room	15					pC	
Off Isolation <sup>h</sup>	OIRR	V <sub>EN</sub> = 0 V, R <sub>L</sub> = 1 kΩ, f = 100 kHz	Room	-69					dB	

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{AL} = 0.8\text{ V}, V_{AH} = 2.4\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Dynamic Characteristics (Cont'd)</b>										
Source Off Capacitance	$C_{S(off)}$	$V_{EN} = 0\text{ V}, V_S = 0\text{ V}, f = 1\text{ MHz}$	Room	8					pF	
Drain Off Capacitance	$C_{D(off)}$	$V_{EN} = 0\text{ V}, V_D = 0\text{ V}$ $f = 1\text{ MHz}$	Room	130						
Drain On Capacitance	$C_{D(on)}$		DG407	Room	65					
			DG406	Room	140					
		DG407	Room	70						
<b>Power Supplies</b>										
Positive Supply Current	I+	$V_{EN} = V_A = 0\text{ or }5\text{ V}$	Room Full	13		30 75		30 75	μA	
Negative Supply Current	I-		Room Full	-0.01	-1 -10		-1 -10			
Positive Supply Current	I+	$V_{EN} = 2.4\text{ V}, V_A = 0\text{ V}$	Room Full	50		100 500		100 200		
Negative Supply Current	I-		Room Full	-0.01	-1 -10		-1 -10			

## Specifications<sup>a</sup> for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_{AL} = 0.8\text{ V}, V_{AH} = 2.4\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		0	12	0	12	V	
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = 3\text{ V}, 10\text{ V}, I_S = -1\text{ mA}$ Sequence Each Switch On	Room	90		120		120	Ω	
$r_{DS(on)}$ Matching Between Channels <sup>g</sup>	$\Delta r_{DS(on)}$		Room	5					%	
Source Off Leakage Current	$I_{S(off)}$	$V_{EN} = 0\text{ V}$ $V_D = 10\text{ V or }0.5\text{ V}$ $V_S = 0.5\text{ V or }10\text{ V}$	Room	0.01					nA	
Drain Off Leakage Current	$I_{D(off)}$		DG406	Room	0.04					
			DG407	Room	0.04					
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 10\text{ V}$ Sequence Each Switch On	DG406	Room	0.04					
			DG407	Room	0.04					
<b>Dynamic Characteristics</b>										
Switching Time of Multiplexer	$t_{TRANS}$	$V_{S1} = 8\text{ V}, V_{S8} = 0\text{ V}, V_{IN} = 2.4\text{ V}$	Room	300		450		450	ns	
Enable Turn-On Time	$t_{ON(EN)}$	$V_{INH} = 2.4\text{ V}, V_{INL} = 0\text{ V}$ $V_{S1} = 5\text{ V}$	Room	250		600		600		
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	150		300		300		
Charge Injection	Q	$C_L = 1\text{ nF}, V_S = 6\text{ V}, R_S = 0$	Room	20					pC	

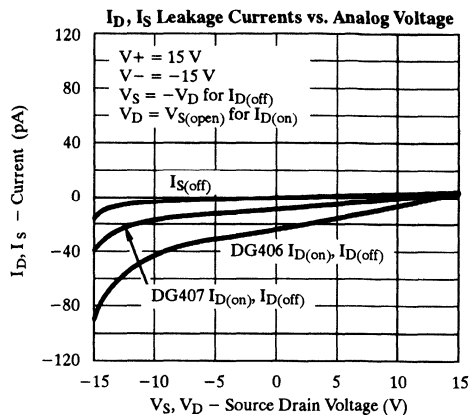
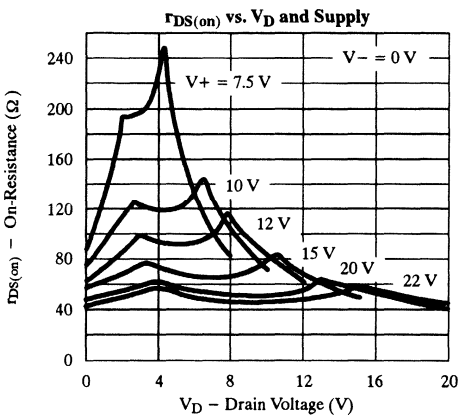
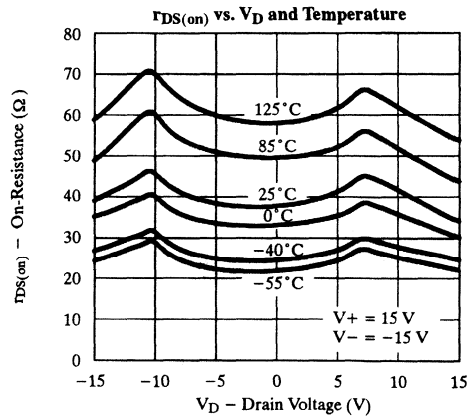
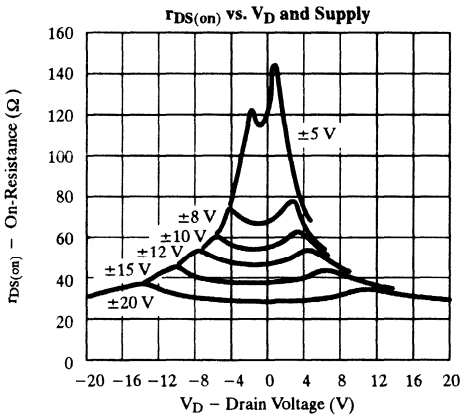
**Specifications<sup>a</sup> for Single Supply**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_{AL} = 0.8\text{ V}, V_{AH} = 2.4\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_{EN} = 0\text{ V or } 5\text{ V}, V_A = 0\text{ V or } 5\text{ V}$	Room Full	13		30		30	μA
Negative Supply Current	I-		Room Full	-0.01	-1		-1	-5	

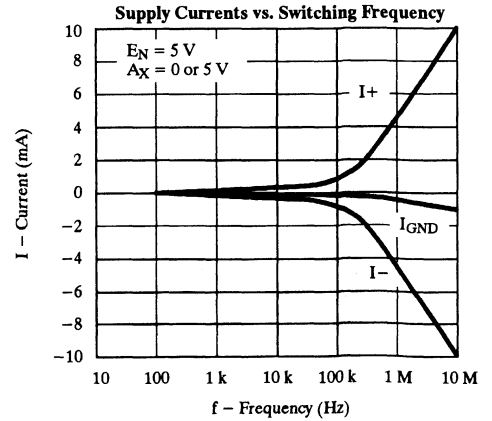
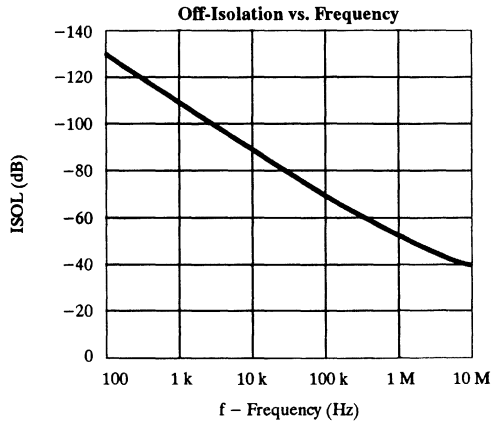
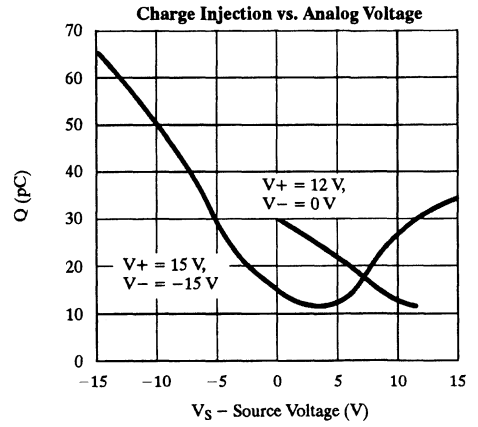
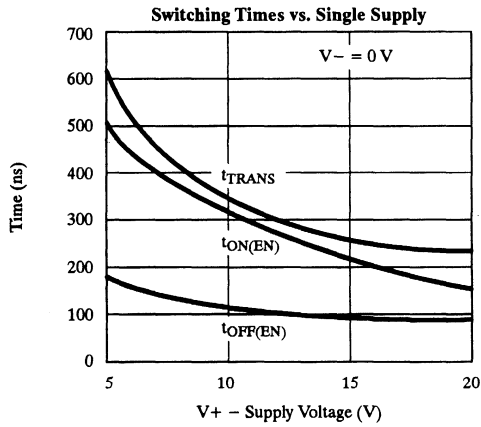
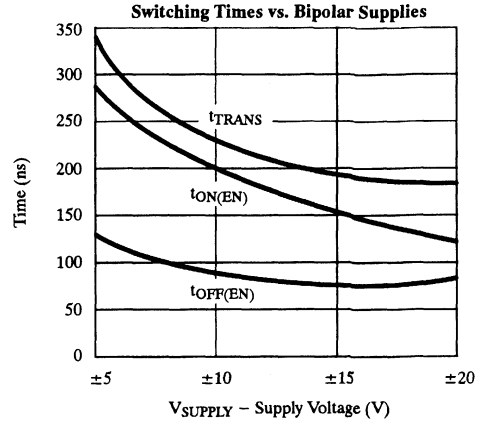
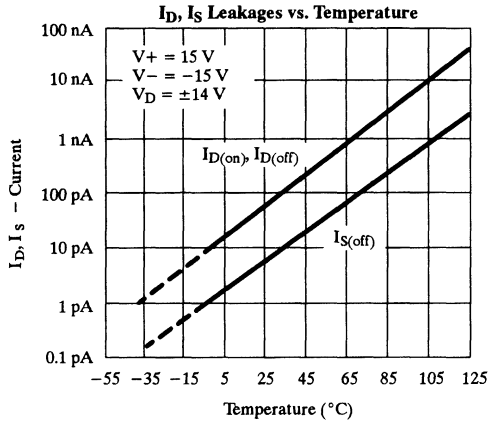
**Notes:**

- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.
- g.  $\Delta r_{DS(on)} = r_{DS(on) MAX} - r_{DS(on) MIN}$ .
- h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin.

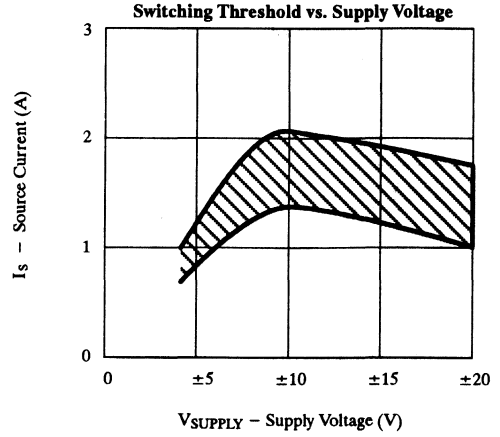
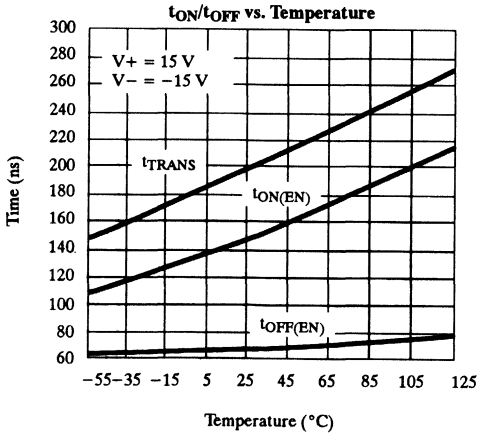
**Typical Characteristics**



## Typical Characteristics (Cont'd)



**Typical Characteristics (Cont'd)**



**Schematic Diagram (Typical Channel)**

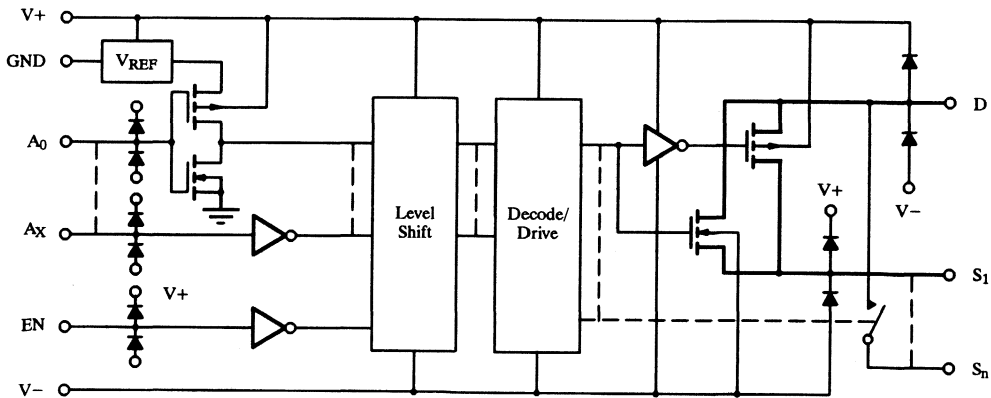
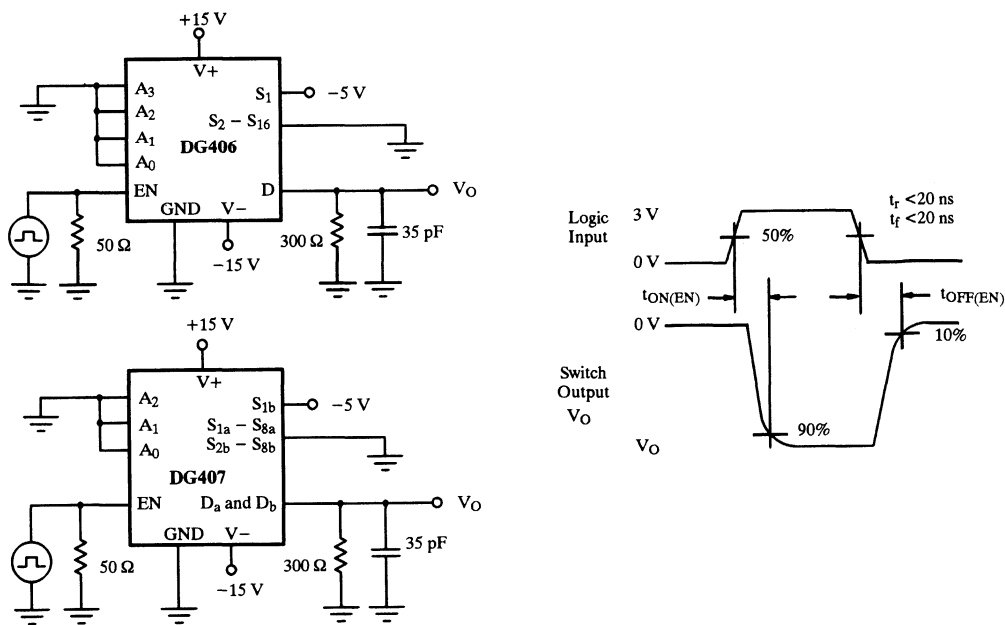
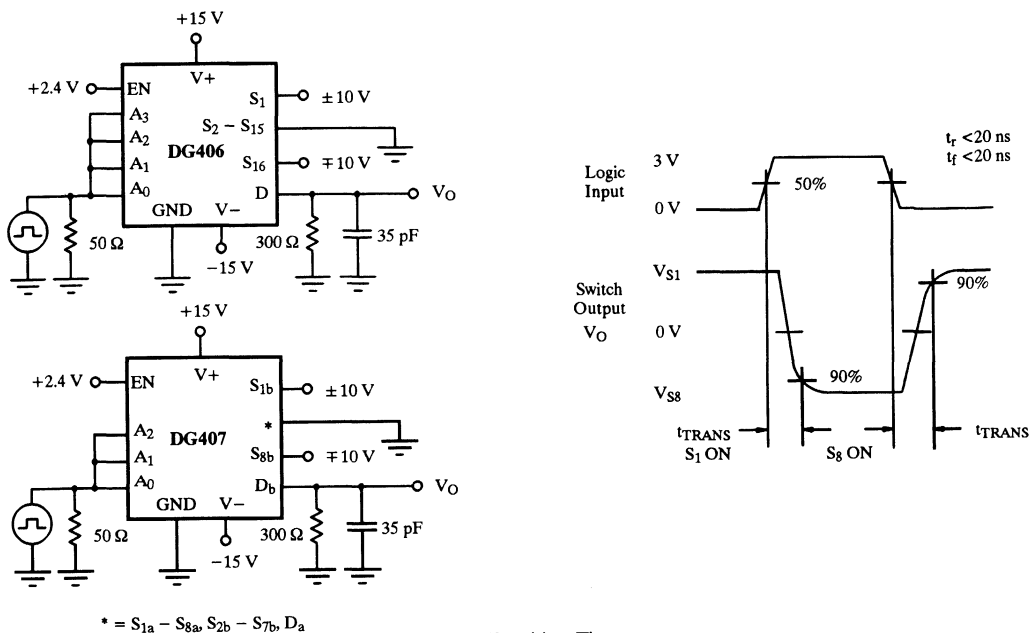
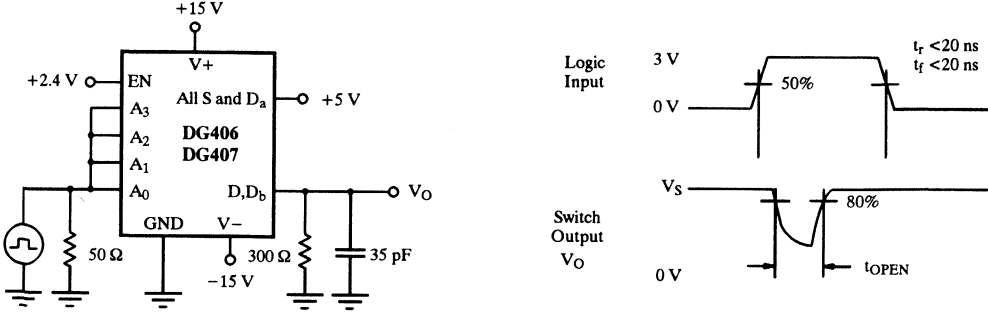


Figure 1.

## Test Circuits



**Test Circuits (Cont'd)**



**Figure 4.** Break-Before-Make Interval

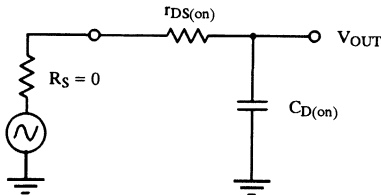
**Application Hints**

Sampling speed is limited by two consecutive events: the transition time of the multiplexer, and the settling time of the sampled signal at the output.

$t_{TRANS}$  is given on the data sheet. Settling time at the load depends on several parameters:  $r_{DS(on)}$  of the multiplexer, source impedance, multiplexer and load capacitances, charge injection of the multiplexer and accuracy desired.

The settling time for the multiplexer alone can be derived from the model shown in Figure 5. Assuming a low impedance signal source like that presented by an op amp or a buffer amplifier, the settling time of the RC network for a given accuracy is equal to  $n\tau$ :

% Accuracy	# Bits	n
0.25	8	6
0.012	12	9
0.0017	15	11



**Figure 5.** Simplified Model of One Multiplexer Channel

The maximum sampling frequency of the multiplexer is:

$$f_s = \frac{1}{N(t_{SETTLING} + t_{TRANS})} \tag{195}$$

where N = number of channels to scan

$$t_{SETTLING} = n\tau = n \times r_{DS(on)} \times C_{D(on)}$$

For the DG406 then, at room temp and for 12-bit accuracy, using the maximum limits:

$$f_s = \frac{1}{16(9 \times 100 \Omega \times 100 \times 10^{-12} \text{ F}) + 300 \times 10^{-12} \text{ s}} \tag{196}$$

or

$$f_s = 694 \text{ kHz} \tag{197}$$

From the sampling theorem, to properly recover the original signal, the sampling frequency should be more than twice the maximum component frequency of the original signal. This assumes perfect bandlimiting. In a real application sampling at three to four times the filter cutoff frequency is a good practice.

Therefore from equation (197) above:

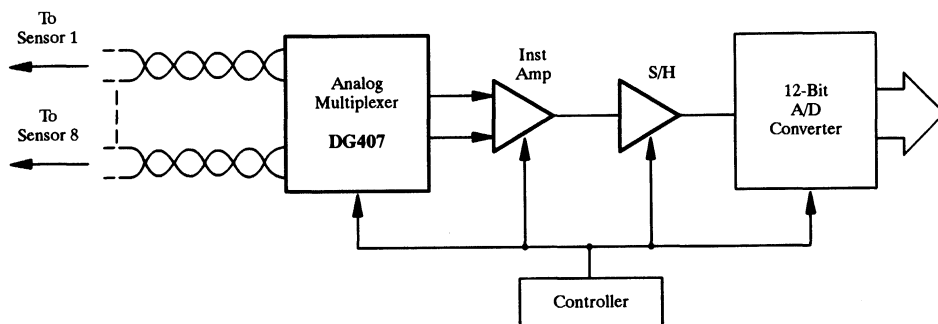
$$f_c = \frac{1}{4} \times f_s = 173 \text{ kHz} \tag{198}$$

From this we can see that the DG406 can be used to sample 16 different signals whose maximum component frequency can be as high as 173 kHz. If for example, two channels are used to double sample the same incoming signal then its cutoff frequency can be doubled.

## Application Hints (Cont'd)

The block diagram shown in Figure 6 illustrates a typical data acquisition front end suitable for low-level analog signals. Differential multiplexing of small signals is preferred since this method helps to reject any common mode noise. This is especially important when the sensors are located at a distance and it may eliminate the need for individual amplifiers. A low  $r_{DS(on)}$ , low leakage

multiplexer like the DG407 helps to reduce measurement errors. The low power dissipation of the DG407 minimizes on-chip thermal gradients which can cause errors due to temperature mismatch along the parasitic thermocouple paths. Please refer to Application Note AN203 for additional information.



**Figure 6.** Measuring low-level analog signals is more accurate when using a differential multiplexing technique.



# 8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

## Features

- Low On-Resistance— $r_{DS(on)}$ : 100  $\Omega$
- Low Charge Injection— $Q$ : 20 pC
- Fast Transition Time— $t_{TRANS}$ : 160 ns
- Low Power— $I_{SUPPLY}$ : 10  $\mu$ A
- Single Supply Capability
- 44-V Supply Max Rating

## Benefits

- Reduced Switching Errors
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness
- Superior to DG508/509A
- Wide Supply Ranges ( $\pm 5$  V to  $\pm 20$  V)

## Applications

- Data Acquisition Systems
- Audio Signal Routing
- ATE Systems
- Battery Powered Systems
- High Rel Systems
- Single Supply Systems
- Medical Instrumentation

## Description

The DG408 is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address ( $A_0, A_1, A_2$ ). The DG409 is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address ( $A_0, A_1$ ). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs,

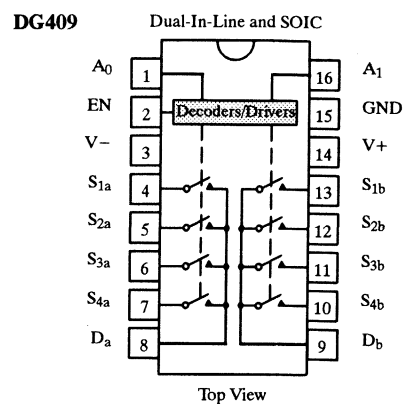
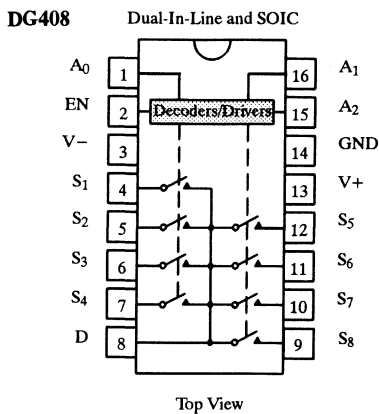
address ( $A_x$ ) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG408/409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44-V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

For additional information please see App Note AN201 and Technical TA201.

## Functional Block Diagrams and Pin Configurations



Truth Table — DG408

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Truth Table — DG409

A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = V<sub>AL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>AH</sub> ≥ 2.4 V  
 X = Don't Care

Ordering Information — DG408

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG408DJ
	16-Pin SOIC	DG408DY
-55 to 125°C	16-Pin CerDIP	DG408AK
		DG408AK/883
		5962-920401MEA
	LCC-20*	5962-920401M2A

Ordering Information — DG409

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG409DJ
	16-Pin SOIC	DG409DY
-55 to 125°C	16-Pin CerDIP	DG409AK
		DG409AK/883
		5962-920402MEA
	LCC-20*	5962-920402M2A

\*Block Diagram and Pin Configuration not shown.

## Absolute Maximum Ratings

Voltage Referenced to V-	
V+ .....	44 V
GND .....	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub> .....	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal) .....	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max) .....	100 mA
Storage Temperature (AK Suffix) .....	-65 to 150°C
(DJ, DY Suffix) .....	-65 to 125°C
Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup> .....	450 mW

16-Pin Narrow SOIC <sup>d</sup> .....	600 mW
16-Pin CerDIP <sup>e</sup> .....	900 mW
LCC-20 <sup>f</sup> .....	750 mW

### Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub> or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 6 mW/°C above 75°C.
- Derate 7.6 mW/°C above 75°C.
- Derate 12 mW/°C above 75°C.
- Derate 10 mW/°C above 75°C.

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{AL} = 0.8\text{ V}, V_{AH} = 2.4\text{ V}^f$		Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
						Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$			Full		-15	15	-15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}, I_S = -10\text{ mA}$		Room Full	40		100 125		100 125	$\Omega$
$r_{DS(on)}$ Matching Between Channels <sup>g</sup>	$\Delta r_{DS(on)}$	$V_D = \pm 10\text{ V}$		Room			15		15	%
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_{EN} = 0\text{ V}$		Room Full		-0.5 -50	0.5 50	-0.5 -5	0.5 5	
Drain Off Leakage Current	$I_{D(off)}$	$V_D = \pm 10\text{ V}, V_S = \mp 10\text{ V}$ $V_{EN} = 0\text{ V}$	DG408	Room Full		-1 -100	1 100	-1 -20	1 20	nA
			DG409	Room Full		-1 -50	1 50	-1 -10	1 10	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 10\text{ V}$ Sequence Each Switch On	DG408	Room Full		-1 -100	1 100	-1 -20	1 20	
			DG409	Room Full		-1 -50	1 50	-1 -10	1 10	
<b>Digital Control</b>										
Logic High Input Voltage	$V_{INH}$			Full		2.4		2.4		V
Logic Low Input Voltage	$V_{INL}$			Full			0.8		0.8	
Logic High Input Current	$I_{AH}$	$V_A = 2.4\text{ V}, 15\text{ V}$		Full		-10	10	-10	10	$\mu\text{A}$
Logic Low Input Current	$I_{AL}$	$V_{EN} = 0\text{ V}, 2.4\text{ V}, V_A = 0\text{ V}$		Full		-10	10	-10	10	
Logic Input Capacitance	$C_{in}$	$f = 1\text{ MHz}$		Room	8					pF
<b>Dynamic Characteristics</b>										
Transition Time	$t_{TRANS}$	See Figure 2		Full	160		250		250	
Break-Before-Make Interval	$t_{OPEN}$	See Figure 4		Room		10		10		ns
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room Full	115		150 225		150	ns
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	105		150		150	
Charge Injection	Q	$C_L = 10\text{ nF}, V_S = 0\text{ V}$		Room	20					pC
Off Isolation <sup>h</sup>	OIRR	$V_{EN} = 0\text{ V}, R_L = 1\text{ k}\Omega, f = 100\text{ kHz}$		Room	-75					dB
Source Off Capacitance	$C_{S(off)}$	$V_{EN} = 0\text{ V}, V_S = 0\text{ V}, f = 1\text{ MHz}$		Room	3					
Drain Off Capacitance	$C_{D(off)}$	$V_{EN} = 0\text{ V}, V_D = 0\text{ V}$ $f = 1\text{ MHz}$	DG408	Room	26					pF
			DG409	Room	14					
Drain On Capacitance	$C_{D(on)}$		DG408	Room	37					
			DG409	Room	25					
<b>Power Supplies</b>										
Positive Supply Current	I+	$V_{EN} = V_A = 0\text{ V or } 5\text{ V}$		Full	10		75		75	$\mu\text{A}$
Negative Supply Current	I-			Full	1	-75		-75		
Positive Supply Current	I+	$V_{EN} = 2.4\text{ V}, V_A = 0\text{ V}$		Room Full	0.2		0.5 2		0.5 2	mA
Negative Supply Current	I-			Full		-500		-500		

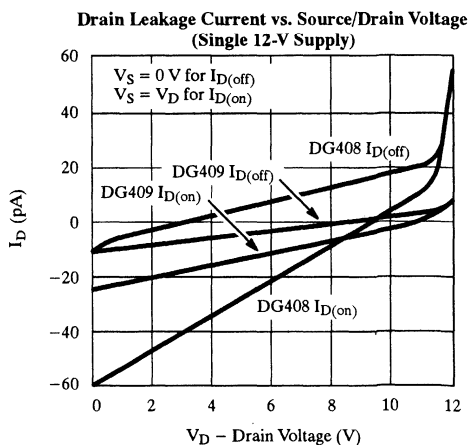
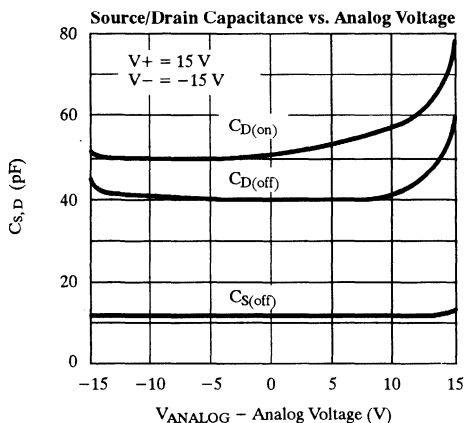
## Specifications<sup>a</sup> for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_{AL} = 0.8\text{ V}, V_{AH} = 2.4\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
					<b>Analog Switch</b>				
Drain-Source On-Resistance <sup>e, f</sup>	$r_{DS(on)}$	$V_D = 3\text{ V}, 10\text{ V}, I_S = -1\text{ mA}$	Room	90					$\Omega$
<b>Dynamic Characteristics</b>									
Switching Time of Multiplexer <sup>e</sup>	$t_{TRANS}$	$V_{S1} = 8\text{ V}, V_{S8} = 0\text{ V}, V_{IN} = 2.4\text{ V}$	Room	180					ns
Enable Turn On Time <sup>e</sup>	$t_{ON(EN)}$	$V_{INH} = 2.4\text{ V}, V_{INL} = 0\text{ V}$ $V_{S1} = 5\text{ V}$	Room	180					
Enable Turn Off Time <sup>e</sup>	$t_{OFF(EN)}$		Room	120					
Charge Injection <sup>e</sup>	Q	$C_L = 1\text{ nF}, V_S = 6\text{ V}, R_S = 0$	Room	5					pC

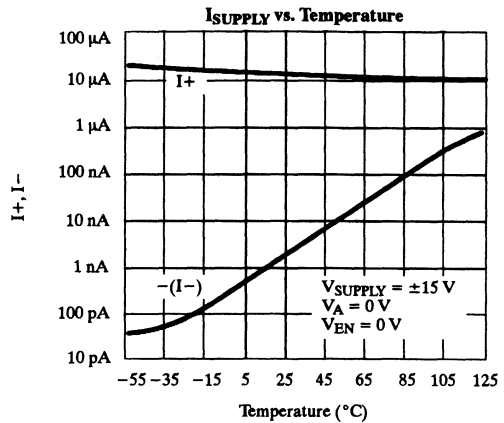
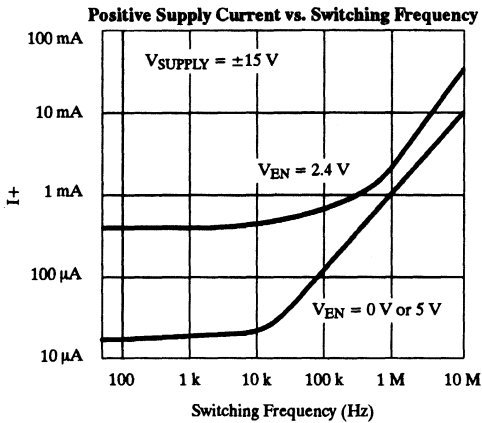
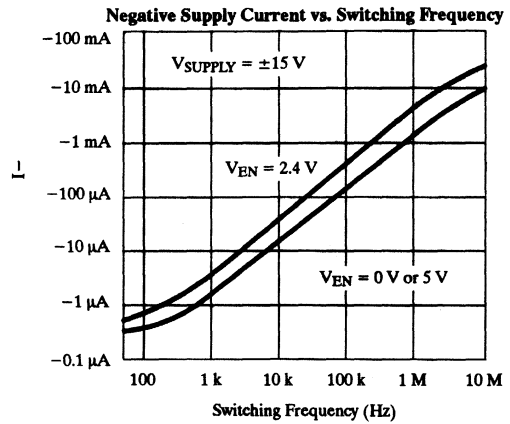
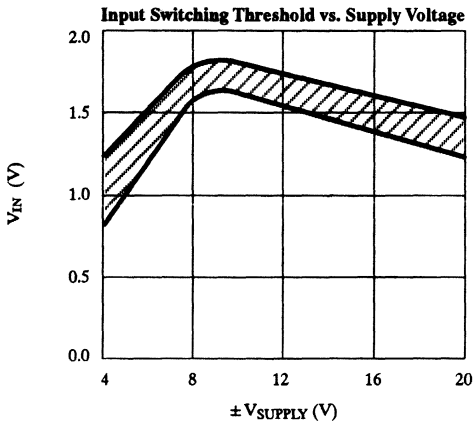
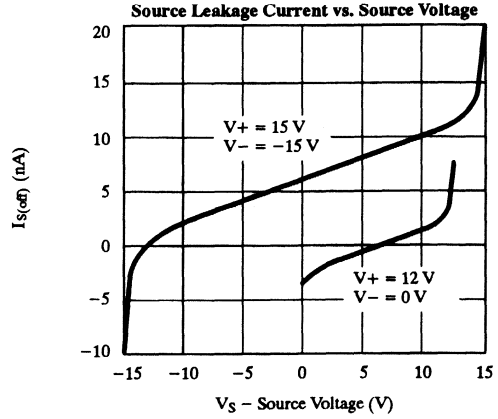
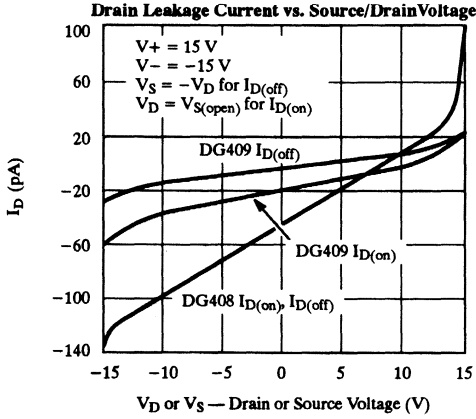
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.
- $\Delta r_{DS(on)} = r_{DS(on)} \text{ Max} - r_{DS(on)} \text{ Min}$ .
- Worst case isolation occurs on Channel 4 do to proximity to the drain pin.

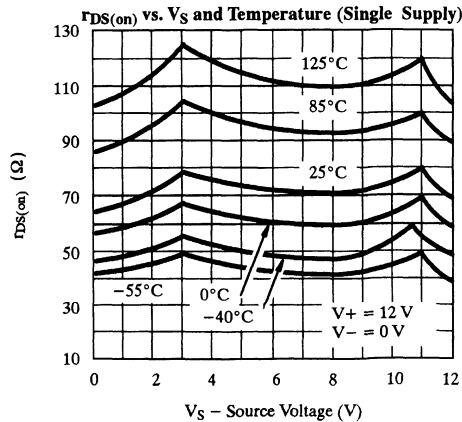
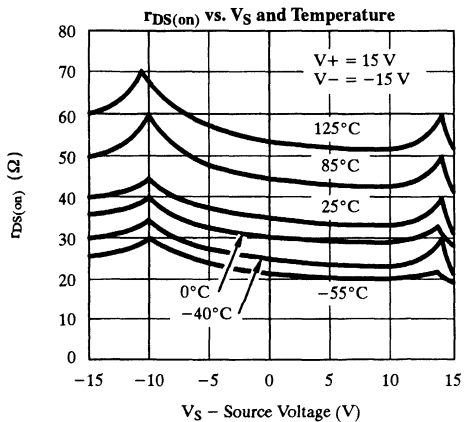
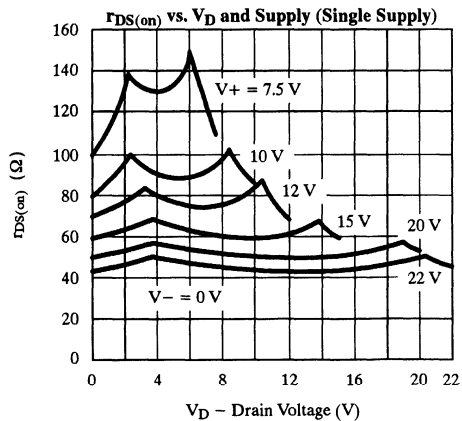
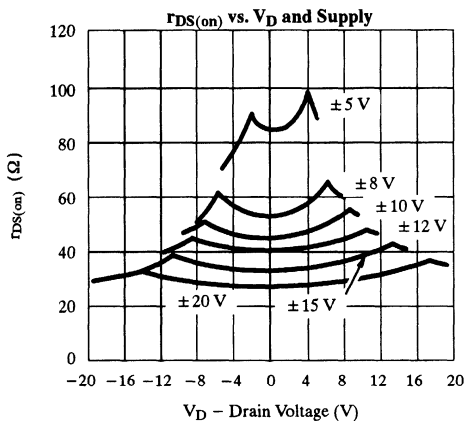
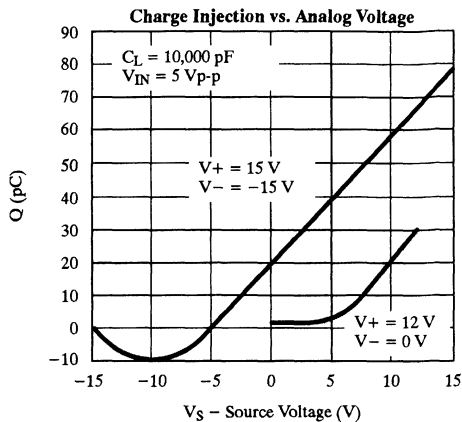
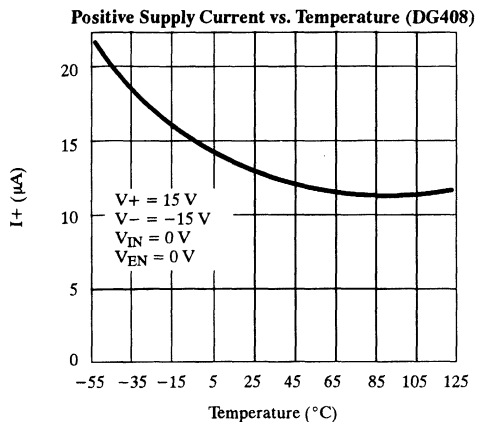
## Typical Characteristics



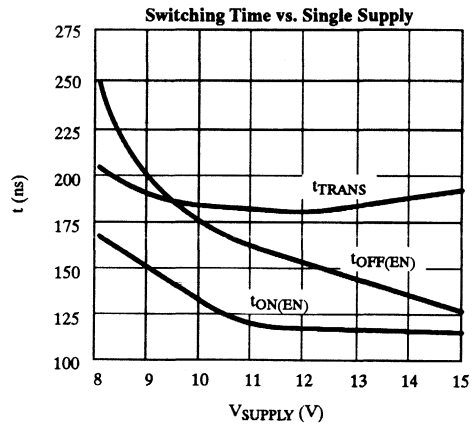
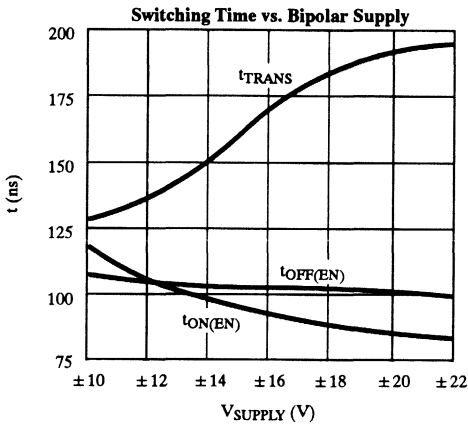
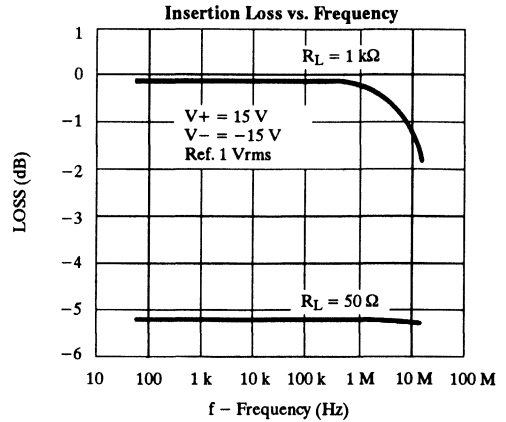
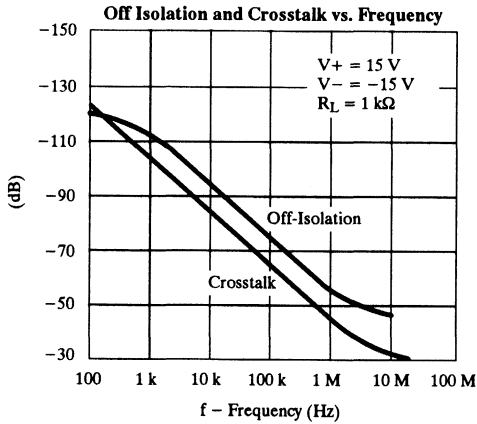
**Typical Characteristics (Cont'd)**



## Typical Characteristics (Cont'd)



**Typical Characteristics (Cont'd)**



**Schematic Diagram (Typical Channel)**

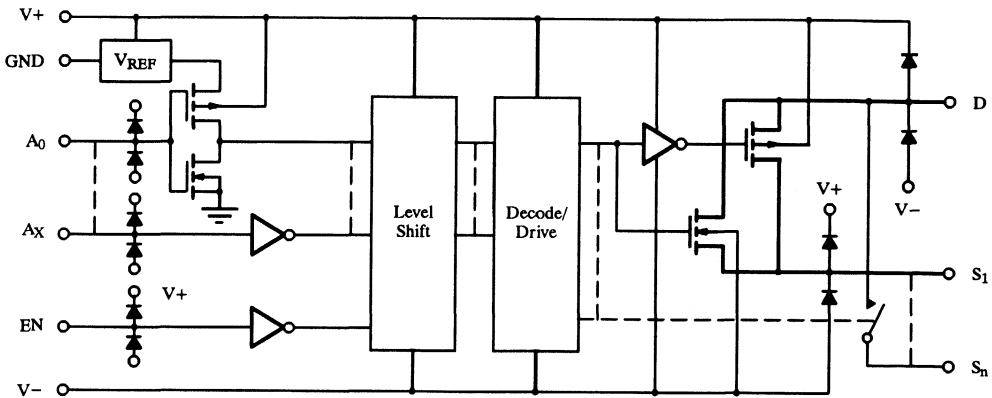


Figure 1.

## Test Circuits

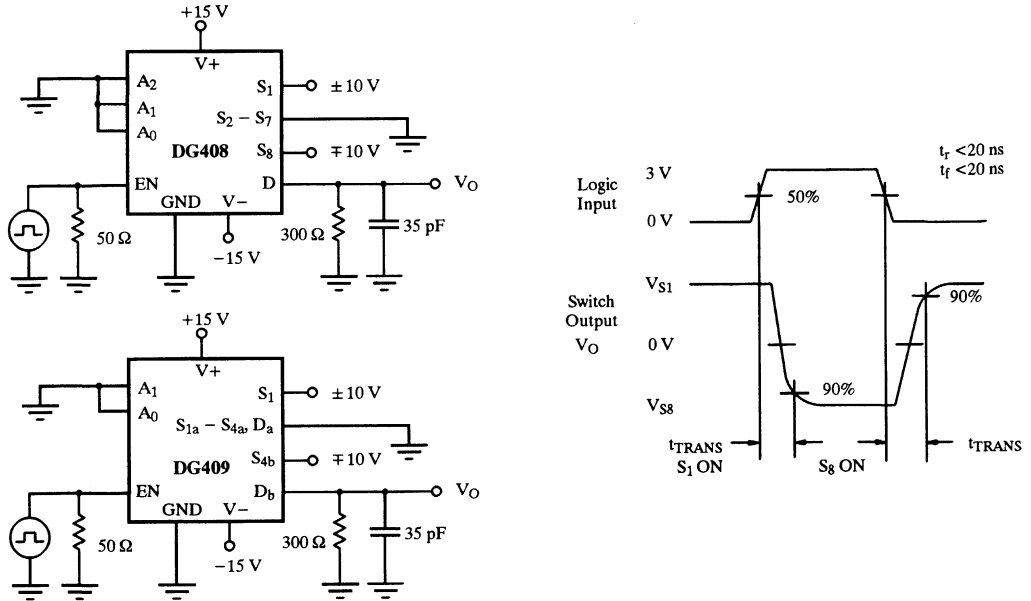


Figure 2. Transition Time

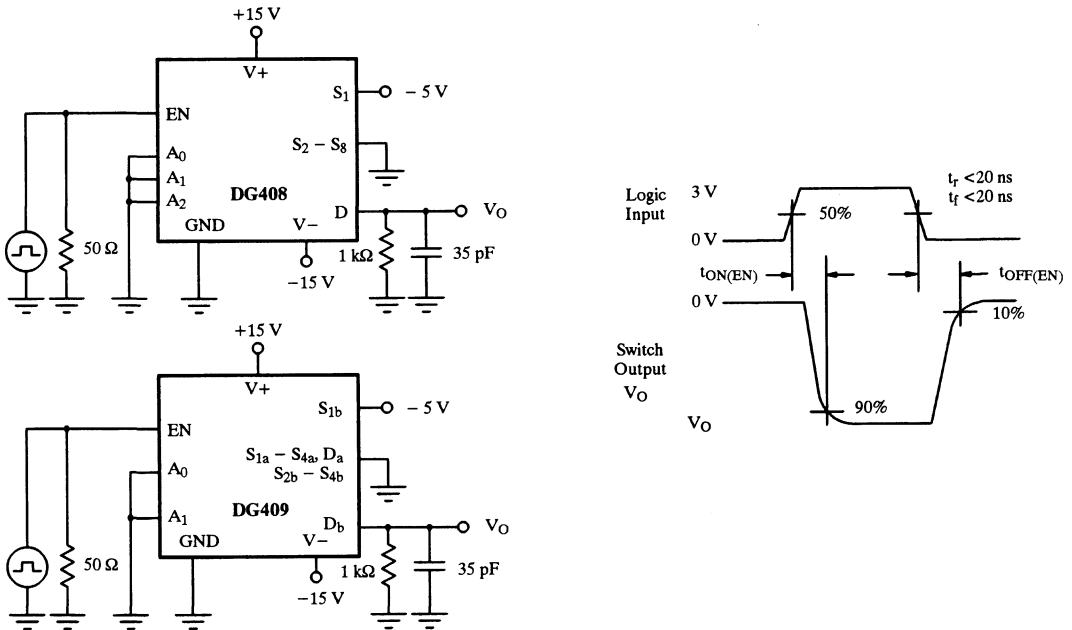
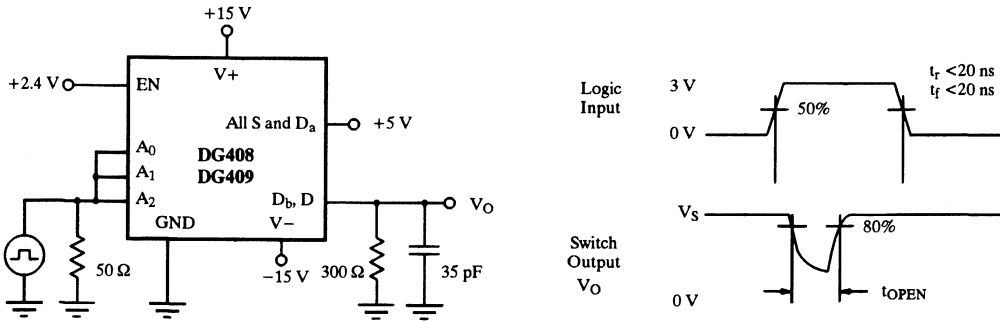


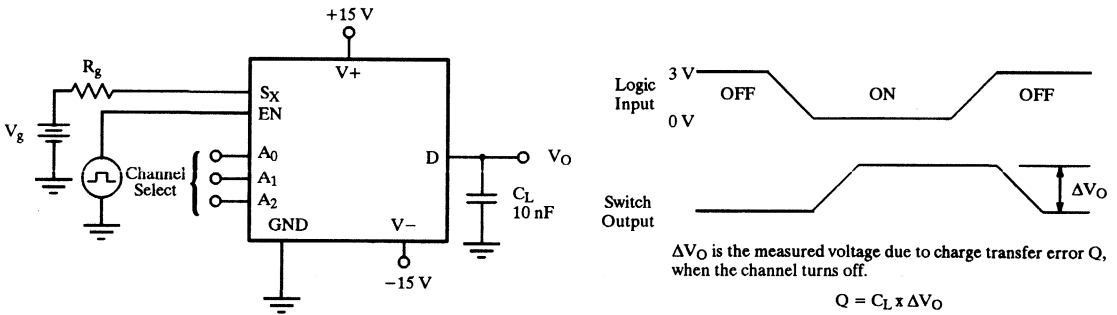
Figure 3. Enable Switching Time



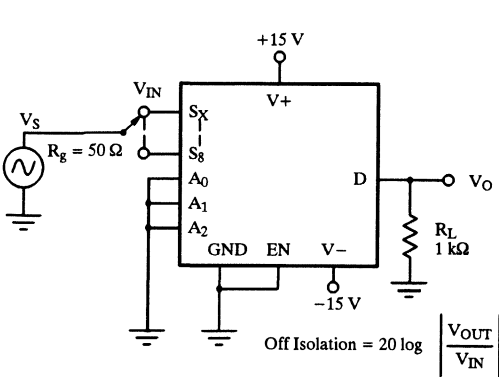
**Test Circuits (Cont'd)**



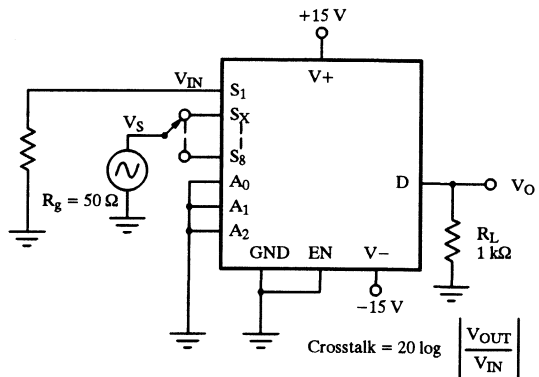
**Figure 4.** Break-Before-Make Interval



**Figure 5.** Charge Injection



**Figure 6.** Off Isolation



**Figure 7.** Crosstalk

## Test Circuits (Cont'd)

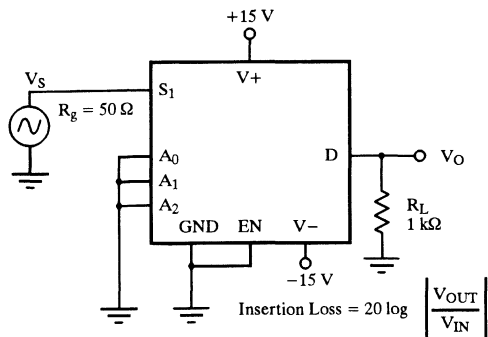


Figure 8. Insertion Loss

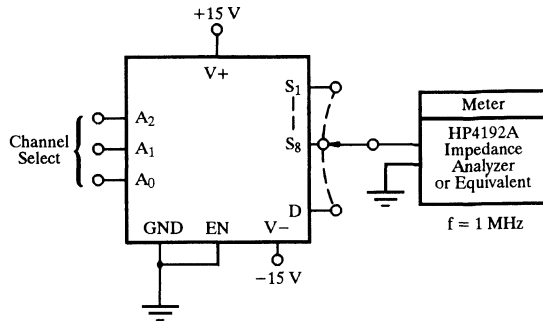


Figure 9. Source Drain Capacitance

## Application Hints

### Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 10). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+

or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference  $V_S - (V-)$  doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

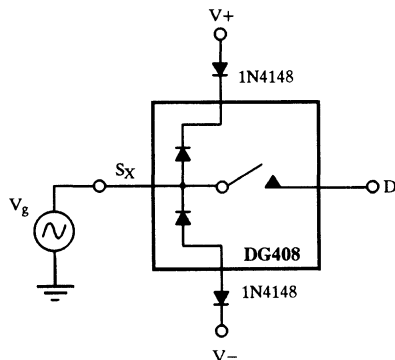


Figure 10. Overvoltage Protection Using Blocking Diodes

**Applications**

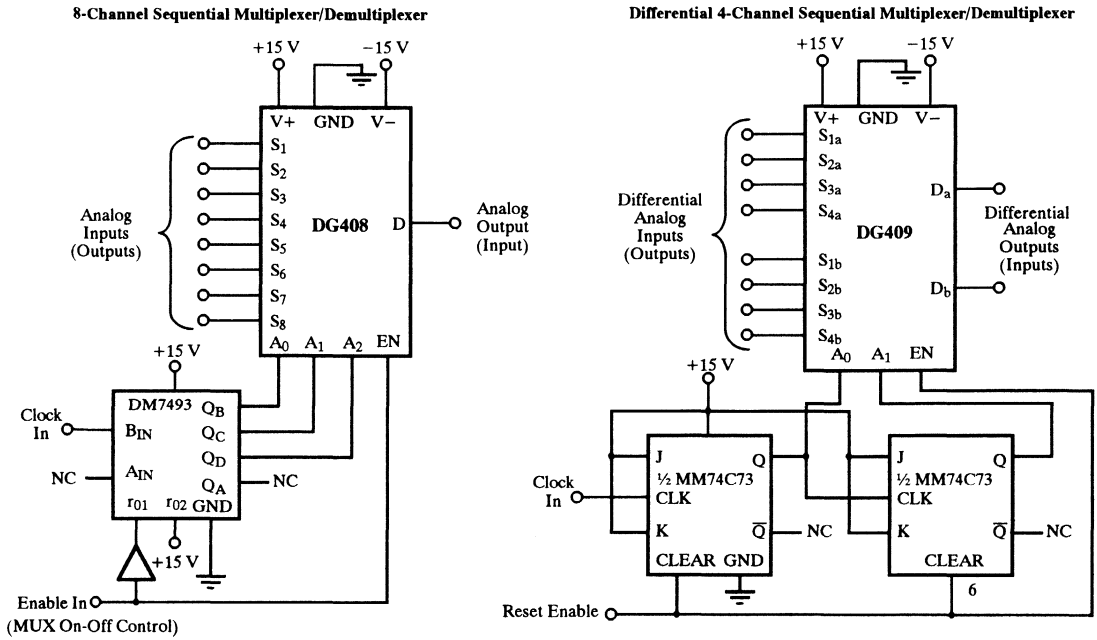


Figure 11.

## Single 8-Channel/Differential 4-Channel Latchable Analog Multiplexers

### Features

- Low  $r_{DS(on)}$ : 55  $\Omega$
- Low Charge Injection: 1 pC
- On-Board TTL Compatible Address Latches
- High Speed— $t_{TRANS}$ : 160 ns
- Break-Before-Make
- Low Power Consumption: 0.3 mW

### Benefits

- Improved System Accuracy
- Microprocessor Bus Compatible
- Easily Interfaced
- Reduced Crosstalk
- High Throughput
- Improved Reliability

### Applications

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Communication Systems
- Microprocessor Controlled Analog Systems
- Medical Instrumentation

### Description

The DG428/DG429 analog multiplexers have on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary crosstalk of adjacent input signals.

The DG428 selects one of eight single-ended inputs to a common output, while the DG429 selects one of four differential inputs to a common differential output.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all

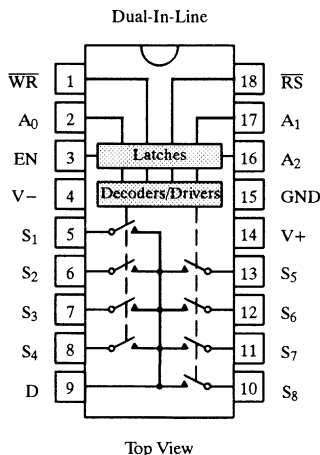
switches off for stacking several devices. All control inputs, address ( $A_x$ ) and enable (EN) are TTL compatible over the full specified operating temperature range.

The silicon-gate CMOS process enables operation over a wide range of supply voltages. The absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed and an epitaxial layer prevents latchup.

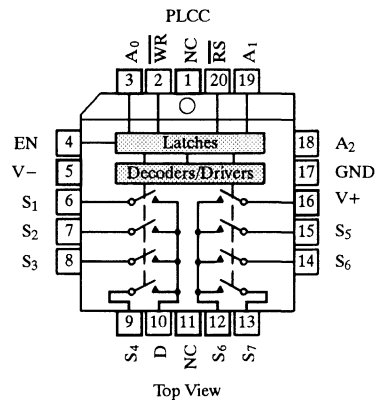
On-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE.

### Functional Block Diagrams and Pin Configurations

DG428

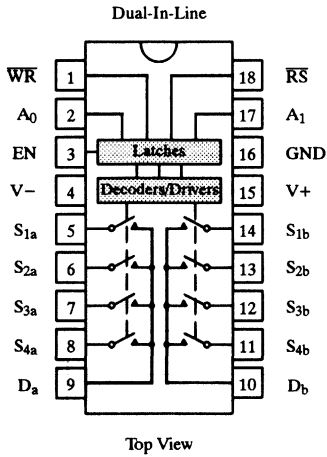


DG428

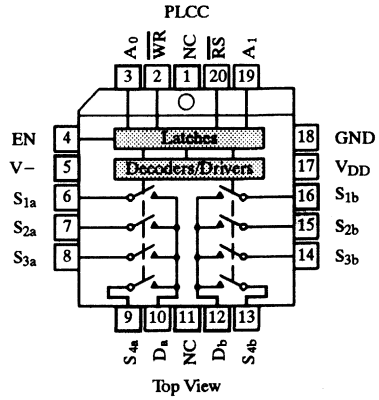


**Functional Block Diagrams and Pin Configurations (Cont'd)**

**DG429**



**DG429**



**Truth Table — DG428**  
8-Channel Single-Ended Multiplexer

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	WR	RS	On Switch
<b>Latching</b>						
X	X	X	X	$\overline{1}$	1	Maintains previous switch condition
<b>Reset</b>						
X	X	X	X	X	0	None (latches cleared)
<b>Transparent Operation</b>						
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

**Ordering Information — DG428**

Temp. Range	Package	Part Number
-40 to 85°C	18-Pin Plastic DIP	DG428DJ
	20-Pin PLCC	DG428DN
-55 to 125°C	18-Pin CerDIP	DG428AK
		DG428AK/883

**Truth Table — DG429**  
Differential 4-Channel Multiplexer

A <sub>1</sub>	A <sub>0</sub>	EN	WR	RS	On Switch
<b>Latching</b>					
X	X	X	$\overline{1}$	1	Maintains previous switch condition
<b>Reset</b>					
X	X	X	X	0	None (latches cleared)
<b>Transparent Operation</b>					
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "0" = V<sub>AL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>AH</sub> ≥ 2.4 V  
 X = Don't Care

**Ordering Information — DG429**

Temp. Range	Package	Part Number
-40 to 85°C	18-Pin Plastic DIP	DG429DJ
	20-Pin PLCC	DG429DN
-55 to 125°C	18-Pin CerDIP	DG429AK
		DG429AK/883

## Absolute Maximum Ratings

Voltage Referenced to V-	
V+ .....	44 V
GND .....	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub> .....	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Current (Any Terminal) .....	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max) .....	100 mA
Storage Temperature (AK Suffix) .....	-65 to 150°C
(DJ, DN Suffix) .....	-65 to 125°C

Power Dissipation (Package) <sup>b</sup>	
18-Pin Plastic DIP <sup>c</sup> .....	470 mW
18-Pin CerDIP <sup>d</sup> .....	900 mW
20-Pin PLCC <sup>e</sup> .....	800 mW

- Notes:
- Signals on S<sub>X</sub>, D<sub>X</sub> or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads soldered or welded to PC board.
  - Derate 6.3 mW/°C above 75°C.
  - Derate 12 mW/°C above 75°C.
  - Derate 10 mW/°C above 75°C.

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V WR = 0, RS = 2.4 V VIN = 2.4 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V	
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, V <sub>AL</sub> = 0.8 V I <sub>S</sub> = -1 mA, V <sub>AH</sub> = 2.4 V	Room Full	55		100 125		100 125	Ω	
Greatest Change in r <sub>DS(on)</sub> Between Channels <sup>f</sup>	Δr <sub>DS(on)</sub>	-10 V < V <sub>S</sub> < 10 V I <sub>S</sub> = -1 mA	Room	5					%	
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓10 V V <sub>EN</sub> = 0 V	Room Full	±0.03	-0.5 -50	0.5 50	-0.5 -50	0.5 50		
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = ±10 V V <sub>S</sub> = ∓10 V V <sub>EN</sub> = 0 V	DG428	Room Full	±0.07	-1 -100	1 100	-1 -100	1 100	nA
			DG429	Room Full	±0.05	-1 -50	1 50	-1 -50	1 50	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = ±10 V V <sub>EN</sub> = 2.4 V V <sub>AL</sub> = 0.8 V, V <sub>AH</sub> = 2.4 V	DG428	Room Full	±0.07	-1 -100	1 100	-1 -100	1 100	
			DG429	Room Full	±0.05	-1 -50	1 50	-1 -50	1 50	
<b>Digital Control</b>										
Logic Input Current Input Voltage High	I <sub>AH</sub>	V <sub>A</sub> = 2.4 V	Full	0.01		1		1	μA	
		V <sub>A</sub> = 15 V	Full	0.01		1		1		
Logic Input Current Input Voltage Low	I <sub>AL</sub>	V <sub>EN</sub> = 0 V, 2.4 V, V <sub>A</sub> = 0 V RS = 0 V, WR = 0 V	Full	-0.01	-1		-1			
Logic Input Capacitance	C <sub>in</sub>	f = 1 MHz	Room	8					pF	
<b>Dynamic Characteristics</b>										
Transition Time	t <sub>TRANS</sub>	See Figure 5	Room Full	150		250 300		250 300	ns	
Break-Before-Make Interval	t <sub>OPEN</sub>	See Figure 4	Full	30	10		10			
Enable and Write Turn-On Time	t <sub>ON(EN, WR)</sub>	See Figures 6 and 7	Room Full	90		150 225		150 225		
Enable and Reset Turn-Off Time	t <sub>OFF(EN, RS)</sub>	See Figures 6 and 8	Room Full	55		150 300		150 300		
Charge Injection	Q	V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω C <sub>L</sub> = 1 nF, See Figure 9	Room	1					pC	
Off Isolation	OIRR	V <sub>EN</sub> = 0 V, R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 15 pF V <sub>S</sub> = 7 V <sub>RMS</sub> , f = 100 kHz	Room	-75					dB	

**Specifications<sup>a</sup> (Cont'd)**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $WR = 0, RS = 2.4\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Dynamic Characteristics (Cont'd)</b>									
Source Off Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}, V_{EN} = 0\text{ V}, f = 1\text{ MHz}$	Room	11					pF
Drain Off Capacitance	$C_{D(off)}$	$V_D = 0\text{ V}, V_{EN} = 0\text{ V}$ $f = 1\text{ MHz}$	DG428	Room	40				
			DG429	Room	20				
Drain On Capacitance	$C_{D(on)}$		DG428	Room	54				
			DG429	Room	34				
<b>Minimum Input Timing Requirements</b>									
Write Pulse Width	$t_w$	See Figure 2	Full		100		100		ns
$A_X$ , EN Data Set Up time	$t_S$		Full		100		100		
$A_X$ , EN Data Hold Time	$t_H$		Full		10		10		
Reset Pulse Width	$t_{RS}$	$V_S = 5\text{ V}$ , See Figure 3	Full		100		100		
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_{EN} = 0\text{ V}, V_A = 0, \overline{RS} = 5\text{ V}$	Room	20		100		100	$\mu\text{A}$
Negative Supply Current	I-		Room	-0.00 1	-5		-5		

**Specifications<sup>a</sup> for Single Supply**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $WR = 0, RS = 2.4\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		0	12	0	12	V	
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = +10\text{ V}, V_{AL} = 0.8\text{ V}$ $I_S = -500\text{ }\mu\text{A}, V_{AH} = 2.4\text{ V}$	Room	80		150		150	$\Omega$	
$r_{DS(on)}$ Match <sup>g</sup>	$\Delta r_{DS(on)}$	$-10\text{ V} < V_S < 10\text{ V}$ $I_S = -1\text{ mA}$	Room	5					%	
Source Off Leakage Current	$I_{S(off)}$	$V_S = 0\text{ V}, 10\text{ V}, V_D = 10\text{ V}, 0\text{ V}$ $V_{EN} = 0\text{ V}$	Room Full	$\pm 0.03$	-0.5 -50	0.5 50	-0.5 -50	0.5 50	nA	
Drain Off Leakage Current	$I_{D(off)}$	$V_D = 0\text{ V}, 10\text{ V}$ $V_S = 10\text{ V}, 0\text{ V}$ $V_{EN} = 0\text{ V}$	DG428	Room Full	$\pm 0.07$	-1 -100	1 100	-1 -100		1 100
			DG429	Room Full	$\pm 0.05$	-1 -50	1 50	-1 -50		1 50
Drain On Leakage Current	$I_{D(on)}$		DG428	Room Full	$\pm 0.07$	-1 -100	1 100	-1 -100		1 100
			DG429	Room Full	$\pm 0.05$	-1 -50	1 50	-1 -50	1 50	
<b>Digital Control</b>										
Logic Input Current Input Voltage High	$I_{AH}$	$V_A = 2.4\text{ V}$	Full			1		1	$\mu\text{A}$	
		$V_A = 12\text{ V}$	Full			1		1		
Logic Input Current Input Voltage Low	$I_{AL}$	$V_{EN} = 0\text{ V}, 2.4\text{ V}, V_A = 0\text{ V}$ $RS = 0\text{ V}, WR = 0\text{ V}$	Full		-1		-1			

## Specifications<sup>a</sup> for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $WR = 0, \overline{RS} = 2.4\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Dynamic Characteristics</b>									
Transition Time	t <sub>TRANS</sub>	See Figure 5	Room Full	160		280 350		280 350	ns
Break-Before-Make Interval	t <sub>OPEN</sub>	See Figure 4	Room Full	40	25 10		25 10		
Enable and Write Turn-On Time	t <sub>ON(EN, WR)</sub>	See Figures 6 and 7	Room Full	110		300 400		300 400	
Enable and Reset Turn-Off Time	t <sub>OFF(EN, RS)</sub>	See Figures 6 and 8	Room Full	70		300 400		300 400	
Charge Injection	Q	$V_{GEN} = 6\text{ V}, R_{GEN} = 0\ \Omega$ $C_L = 1\text{ nF}$ , See Figure 9	Room	4					pC
Off Isolation	OIRR	$V_{EN} = 0\text{ V}, R_L = 300\ \Omega, C_L = 15\text{ pF}$ $V_S = 7\text{ V}_{RMS}, f = 100\text{ kHz}$	Room	-75					dB
<b>Minimum Input Timing Requirements</b>									
Write Pulse Width	t <sub>w</sub>	See Figure 2	Full		100		100		ns
A <sub>X</sub> , EN Data Set Up Time	t <sub>s</sub>		Full		100		100		
A <sub>X</sub> , EN Data Hold Time	t <sub>h</sub>		Full		10		10		
Reset Pulse Width	t <sub>RS</sub>	$V_S = 5\text{ V}$ , See Figure 3	Full		100		100		
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_{EN} = 0\text{ V}, V_A = 0, \overline{RS} = 5\text{ V}$	Room	20		100		100	μA

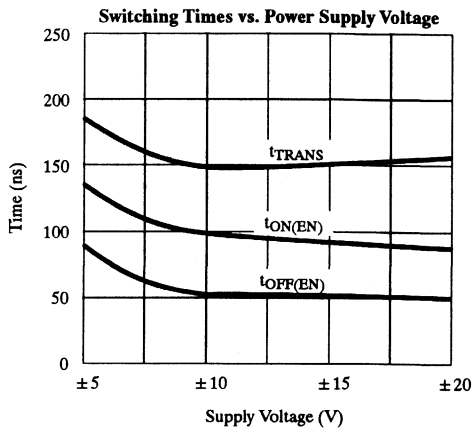
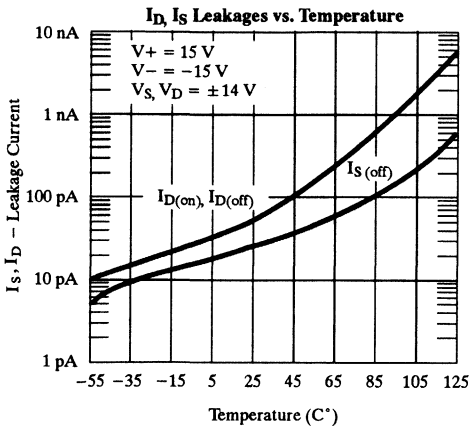
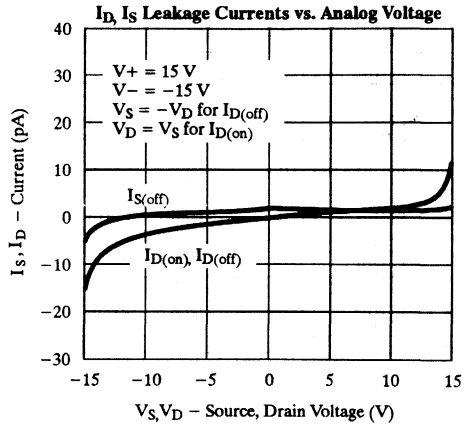
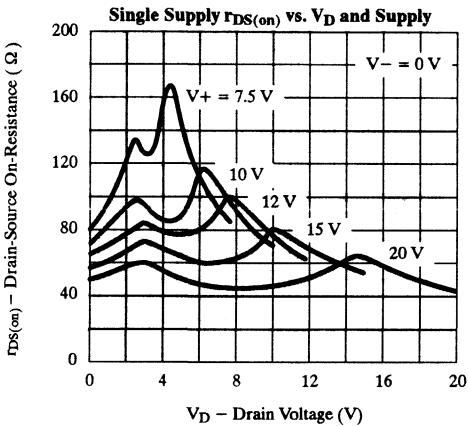
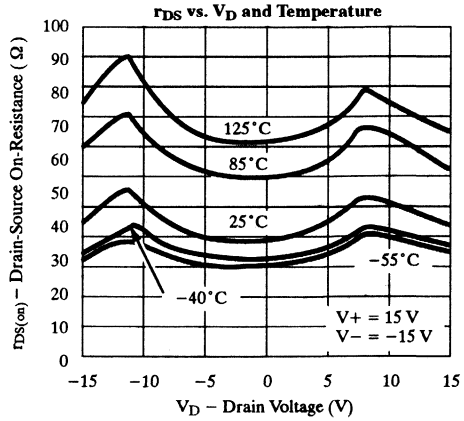
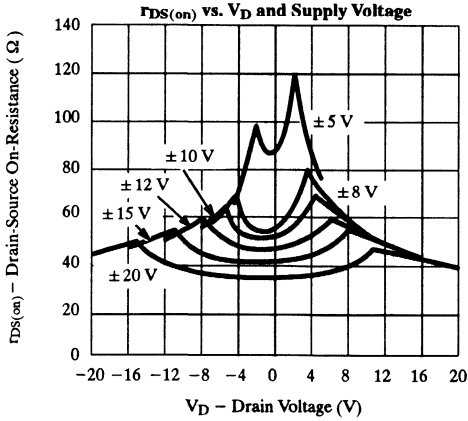
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

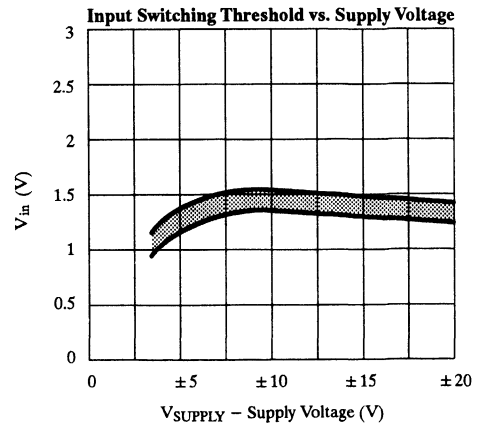
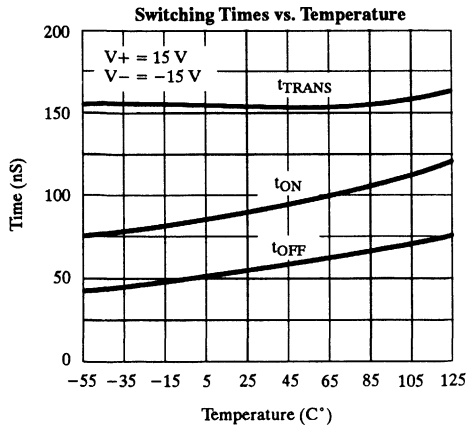
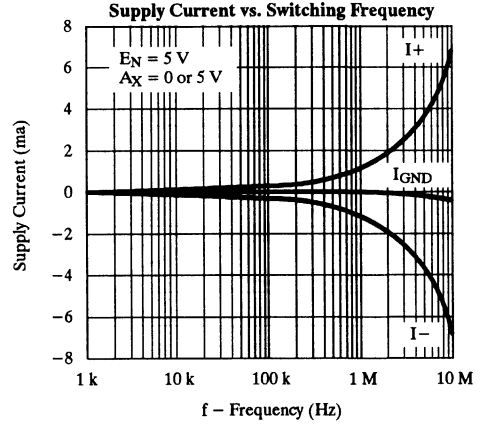
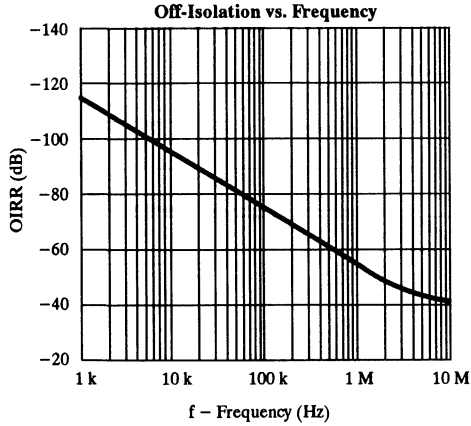
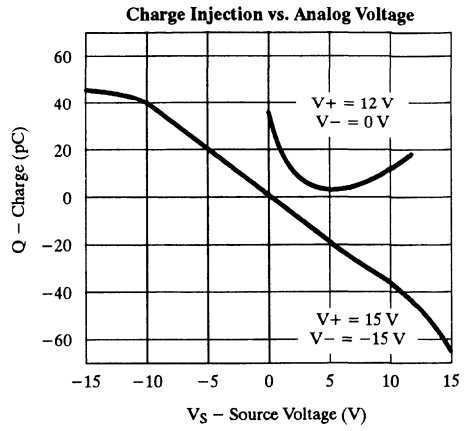
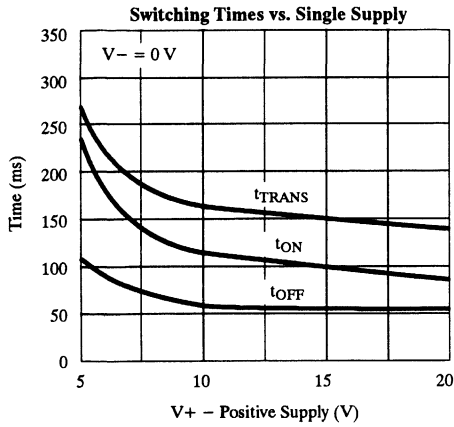
$$g. \Delta r_{DS(on)} = \left( \frac{r_{DS(on) \text{ MAX}} - r_{DS(on) \text{ MIN}}}{r_{DS(on) \text{ AVE}}} \right) \times 100\%$$



**Typical Characteristics**



## Typical Characteristics (Cont'd)



**Schematic Diagram (Typical Channel)**

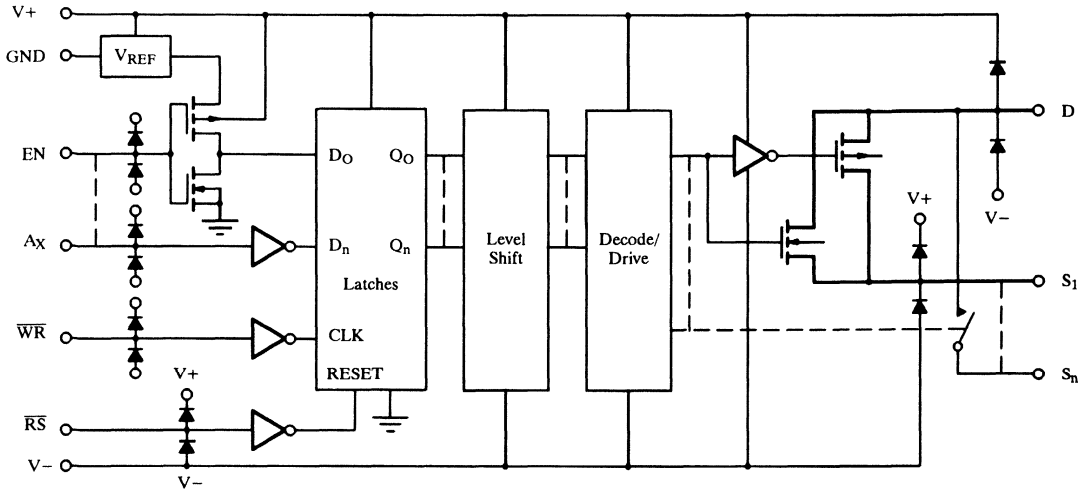


Figure 1.

**Detailed Description**

The internal structure of the DG428/DG429 includes a 5-V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel n- and p-channel MOSFETs (see Figure 1).

The input protection on the logic lines  $A_0$ ,  $A_1$ ,  $A_2$ , EN and control lines  $\overline{WR}$ ,  $\overline{RS}$  shown in Figure 1 minimizes susceptibility to ESD that may be encountered during handling and operational transients.

The logic interface is a CMOS logic input with its supply voltage from an internal +5 V reference voltage. The output of the input inverter feeds the data input of a D type latch. The level sensitive D latch continuously places the  $D_x$  input signal on the  $Q_x$  output when the  $\overline{WR}$  input is low, resulting in transparent latch operation. As soon as  $\overline{WR}$  returns high the latch holds the data last present on the  $D_n$

input, subject to the “Minimum Input Timing Requirements” table.

Following the latches the  $Q_n$  signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting ensures full on/off switch operation for any analog signal level between the  $V+$  and  $V-$  supply rails.

The EN pin is used to enable the address latches during the  $\overline{WR}$  pulse. It can be hard wired to the logic supply or to  $V+$  if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The  $\overline{RS}$  pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The  $\overline{WR}$  pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

## Timing Diagrams

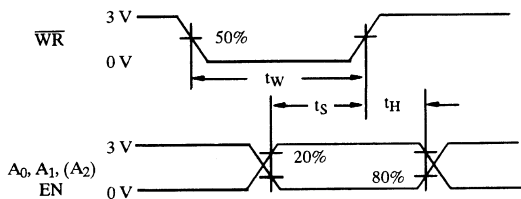


Figure 2.

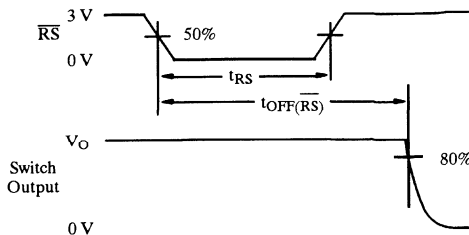


Figure 3.

## Test Circuits

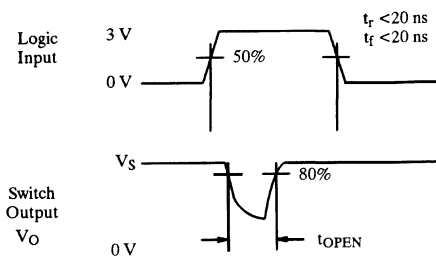
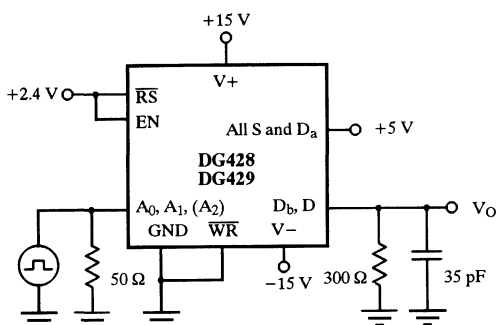


Figure 4. Break-Before-Make

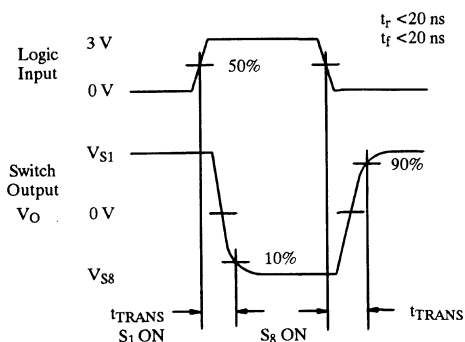
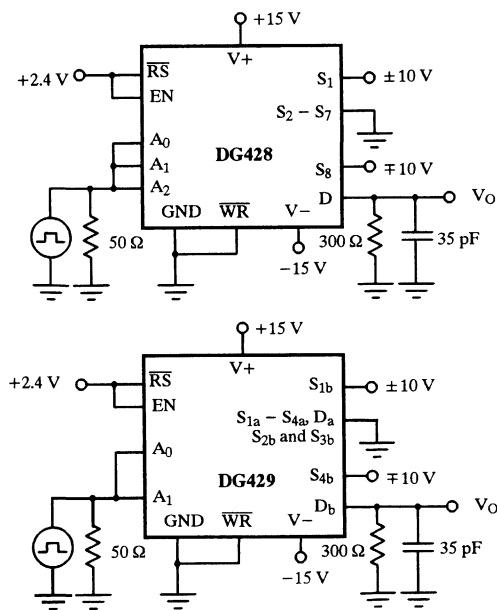
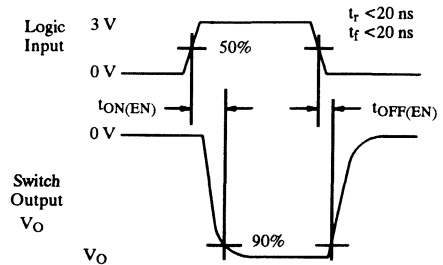
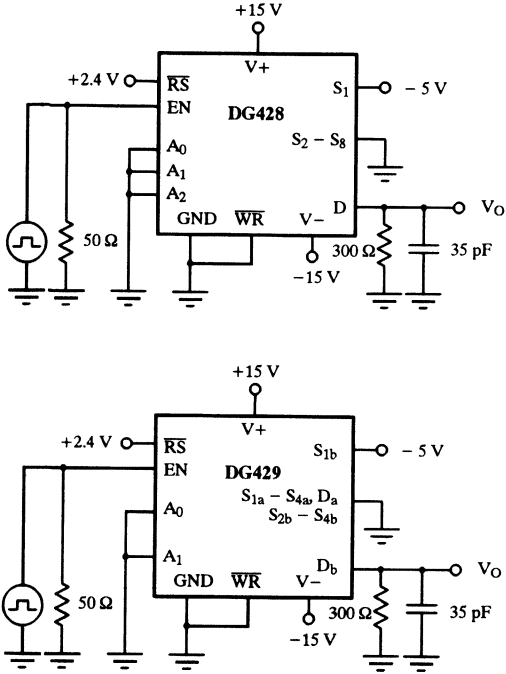
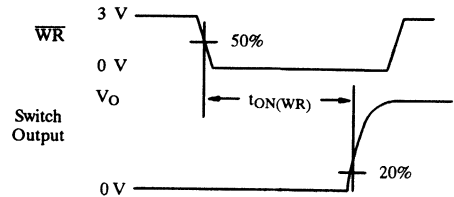
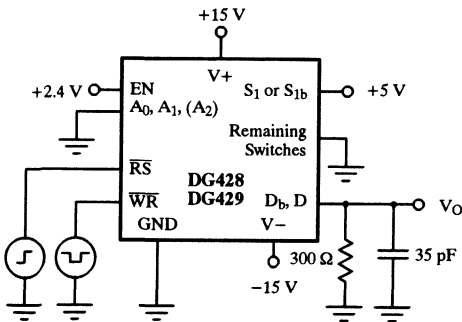


Figure 5. Transition Time

**Test Circuits (Cont'd)**

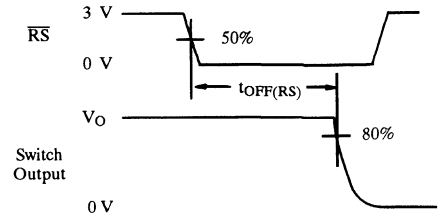
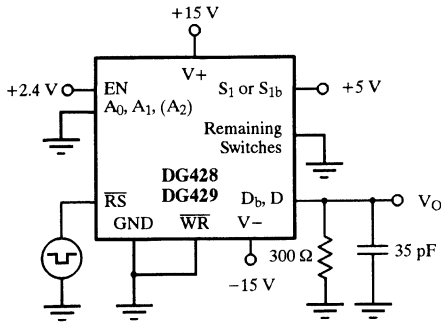


**Figure 6.** Enable  $t_{ON}/t_{OFF}$  Time

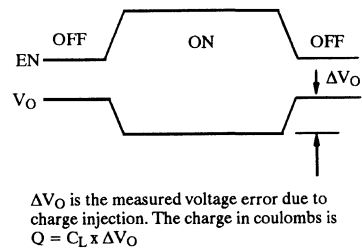
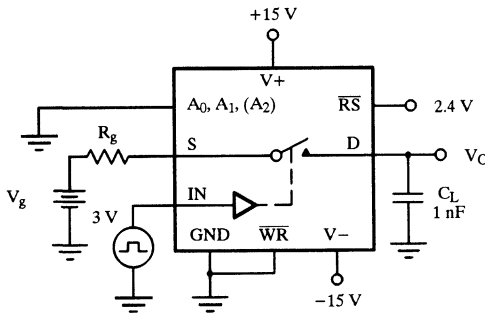


**Figure 7.** Write Turn-On Time  $t_{ON}(WR)$

## Test Circuits (Cont'd)



**Figure 8.** Reset Turn-Off Time  $t_{OFF(RS)}$



**Figure 9.** Charge Injection

## Applications

### Bus Interfacing

The DG428/DG429 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 on) until the microprocessor determines it is necessary to turn different switches on or turn all switches off (see Figure 10).

The input latches become transparent when  $\overline{WR}$  is held low; therefore, these multiplexers operate by direct command of the coded switch state on  $A_2, A_1, A_0$ . In this mode the DG428 is identical to the popular DG408. The same is true of the DG429 versus the popular DG409.

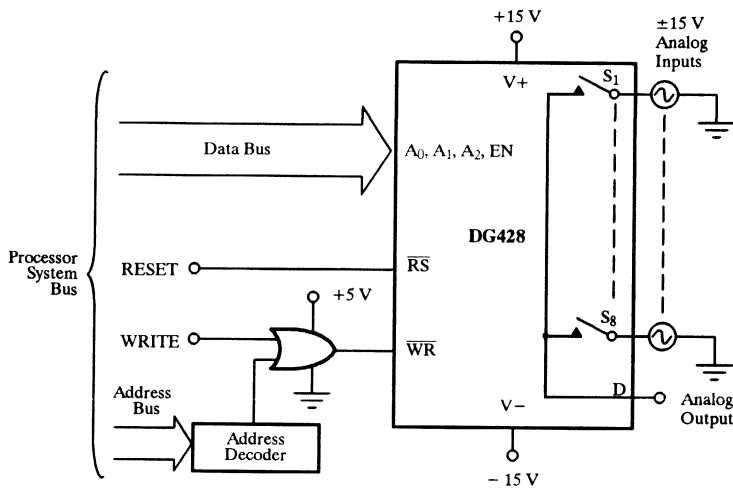
During system power-up,  $\overline{RS}$  would be low, maintaining all eight switches in the off state. After  $\overline{RS}$  returned high the DG428 maintains all switches in the off state.

**Applications (Cont'd)**

When the system program performs a write operation to the address assigned to the DG428, the address decoder provides a  $\overline{CS}$  active low signal which is gated with the WRITE ( $\overline{WR}$ ) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the  $\overline{WR}$  signal returns to the high state, (positive edge) the input latches of the DG428 save the data from the DATA BUS. The coded information in the  $A_0, A_1,$

$A_2$  and EN latches is decoded and the appropriate switch is turned on.

The EN latch allows all switches to be turned off under program control. This becomes useful when two or more DG428s are cascaded to build 16-line and larger multiplexers.



**Figure 10.** Bus Interface

## Fault Protected Single 8-Channel/Differential 4-Channel Analog Multiplexers

### Features

- Fault and Overvoltage Protection
- All Channels Off When Power Off
- Latchup-Proof
- Fast Switching— $T_A$ : 200 ns
- Break-Before-Make Switching
- Low On-Resistance: 180  $\Omega$
- Low Power Consumption: 3 mW
- TTL and CMOS Compatible Inputs

### Benefits

- Improved Ruggedness
- Power Loss Protection
- Prevents Adjacent Channel Crosstalk
- Standard Logic Interface
- Superior Accuracy
- Fast Settling Time

### Applications

- Data Acquisition Systems
- Industrial Process Control Systems
- Avionics Test Equipment
- High-Rel Control Systems
- Telemetry

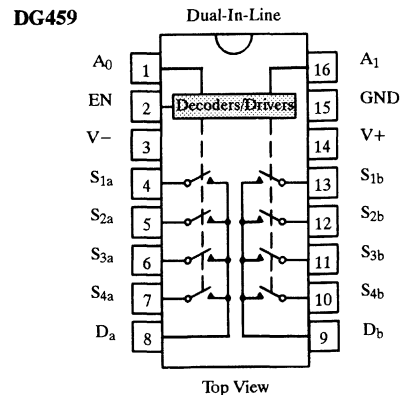
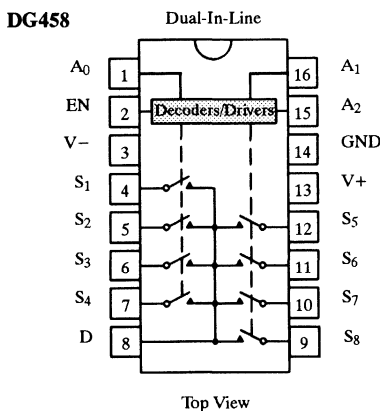
### Description

The DG458 and DG459 are 8-channel single-ended and 4-channel differential analog multiplexers, respectively, incorporating fault protection. A series n-p-n MOSFET structure provides device and signal-source protection in the event of power loss or overvoltages. Under fault conditions the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry following it, but also protects the sensors or signal sources which drive the multiplexer.

The DG458 and DG459 can withstand continuous overvoltage inputs up to  $\pm 35$  V. All digital inputs have TTL compatible logic thresholds. Break-before-make operation prevents channel-to-channel interference.

The DG458 and DG459 are improved pin-compatible replacements for HI-508A/509A and MAX358/359 multiplexers.

### Functional Block Diagrams and Pin Configurations





**Truth Tables and Ordering Information**

Truth Table — DG458

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Truth Table — DG459

A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = V<sub>AL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>AH</sub> ≥ 2.4 V  
 X = Don't Care

**Ordering Information**

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG458DJ
		DG459DJ
-55 to 125°C	16-Pin CerDIP	DG458AK/883
		DG459AK/883
	LCC-20	DG458AZ/883
		DG459AZ/883

\*Block Diagram and Pin Configuration not shown.

**Absolute Maximum Ratings**

V <sub>+</sub> to V <sub>-</sub> .....	44 V
V <sub>+</sub> to GND .....	22 V
V <sub>-</sub> to GND .....	-25 V
V <sub>EN</sub> , V <sub>A</sub> Digital Input .....	(V <sub>-</sub> ) -4 V to (V <sub>+</sub> ) +4 V
V <sub>S</sub> , Analog Input Overvoltage with Power On .....	(V <sub>-</sub> ) -20 V to (V <sub>+</sub> ) +20 V
V <sub>S</sub> , Analog Input Overvoltage with Power Off .....	-35 V to +35 V
Continuous Current, S or D .....	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max) .....	40 mA

Storage Temperature (AK Suffix) .....	-65 to 150°C
(DJ Suffix) .....	-65 to 125°C

Power Dissipation (Package) <sup>a</sup>	
16-Pin Plastic DIP <sup>b</sup> .....	600 mW
16-Pin CerDIP <sup>c</sup> .....	1000 mW
LCC-20 <sup>d</sup> .....	1000 mW

Notes:

- All leads soldered or welded to PC board.
- Derate 6.3 mW/°C above 25°C.
- Derate 12 mW/°C above 75°C.
- Derate 10 mW/°C above 75°C.

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{AL} = 0.8\text{ V}$ , $V_{AH} = 2.4\text{ V}^f$		Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
						Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>										
Analog Signal Range <sup>g</sup>	$V_{ANALOG}$			Full		-10	10	-10	10	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 9.5\text{ V}$ , $I_S = -400\text{ }\mu\text{A}$		Room	0.45		1.2		1.5	k $\Omega$
		$V_D = \pm 5\text{ V}$ , $I_S = -400\text{ }\mu\text{A}$		Room	180		400		400	$\Omega$
$r_{DS(on)}$ Matching Between Channels <sup>h</sup>	$\Delta r_{DS(on)}$	$V_D = 0\text{ V}$ , $I_S = -400\text{ }\mu\text{A}$		Room	6					%
Source Off Leakage Current	$I_{S(off)}$	$V_{EN} = 0\text{ V}$ $V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$		Room Full	0.03	-0.5 -50	0.5 50	-1 -20	1 20	
Drain Off Leakage Current	$I_{D(off)}$	$V_{EN} = 0\text{ V}$ $V_D = \pm 10\text{ V}$ $V_S = \mp 10\text{ V}$	DG458	Room Full	0.1	-1 -200	1 200	-1 -50	1 50	nA
			DG459	Room Full	0.1	-1 -100	1 100	-2 -25	2 25	
Differential Off Drain Leakage Current	$I_{DIFF}$	DG459 Only		Room		-50	50	-20	20	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 10\text{ V}$	DG458	Room Full	0.1	-2 -200	2 200	-5 -50	5 50	
			DG459	Room Full	0.05	-2 -100	2 100	-5 -25	5 25	
<b>Fault</b>										
Output Leakage Current (with Overvoltage)	$I_{D(off)}$	$V_S = \pm 33\text{ V}$ , $V_D = 0\text{ V}$ See Figure 1		Room	0.02					nA
Input Leakage Current (with Overvoltage)	$I_{S(off)}$	$V_S = \pm 25\text{ V}$ , $V_D = \pm 10\text{ V}$ , See Figure 1		Room	0.005	-5	5	-10	10	$\mu\text{A}$
Input Leakage Current (with Power Supplies Off)		$V_S = \pm 25\text{ V}$ , $V_{SUPS} = 0\text{ V}$ $V_D = A_0, A_1, A_2$ , $EN = 0\text{ V}$		Room	0.001	-2	2	-5	5	
<b>Digital Control</b>										
Input Low Threshold	$V_{AL}$			Full			0.8		0.8	V
Input Low Threshold	$V_{AL}$			Full		2.4		2.4		
Logic Input Control	$I_A$	$V_A = 2.4\text{ V}$ or $0.8\text{ V}$		Full		-1	1	-1	1	$\mu\text{A}$
<b>Dynamic Characteristics</b>										
Transition Time	$t_A$	See Figure 2		Room	200		500		500	ns
Break-Before-Make Time	$t_{OPEN}$	See Figure 3		Room	45	10		10		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 4		Room Full	140		250 500		250 500	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room Full	50		250 500		250 500	
Settling Time	$t_s$	$T_D$ 0.1 %		Room	0.5					$\mu\text{s}$
		$T_D$ 0.01 %		Room	1.5					
Off Isolation	OIRR	$V_{EN} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ $V_S = 3\text{ V}_{RMS}$ , $f = 100\text{ kHz}$		Room	90					dB
Logic Input Capacitance	$C_{in}$	$f = 1\text{ MHz}$		Room	5					pF
Source Off Capacitance	$C_{S(off)}$			Room	5					
Drain Off Capacitance	$C_{D(off)}$			Room	15					
				DG459	Room	10				
Drain On Capacitance	$C_{D(on)}$			DG458	Room	40				
				DG459	Room	35				

**Specifications<sup>a</sup>**

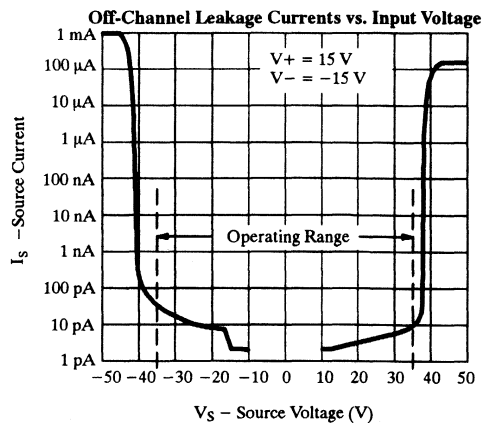
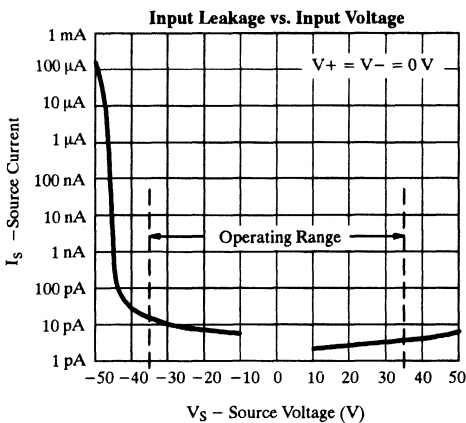
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					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_{EN} = 5.0\text{ or }0\text{ V}, V_A = 0\text{ V}$	Room Full	0.05		0.1 0.2		0.1 0.2	mA
Negative Supply Current	I-		Room Full	-0.01	-0.1 -0.2		-0.1 -0.2		
Power Supply Range for Continuous Operation			Room		±4.5	±18	±4.5	±18	V

**Notes:**

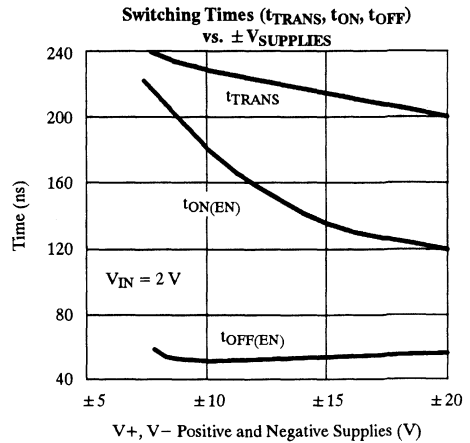
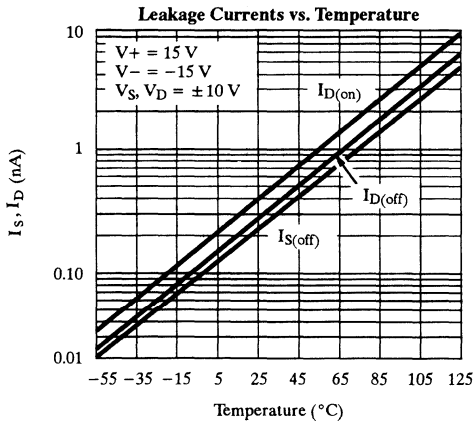
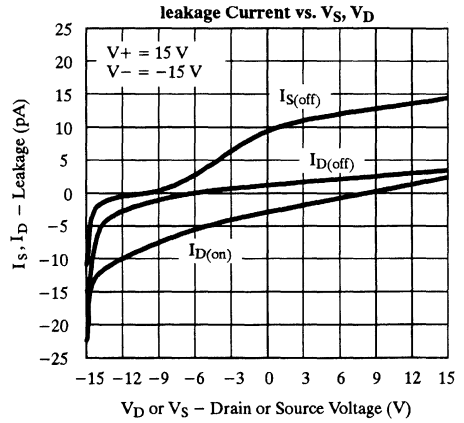
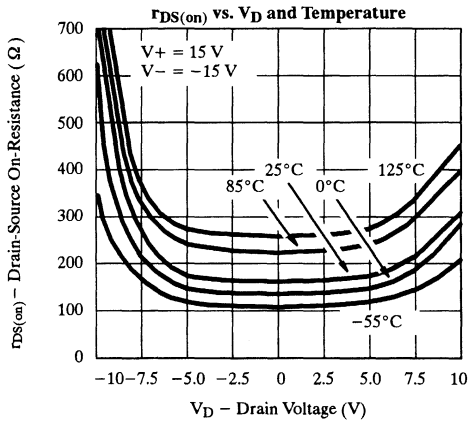
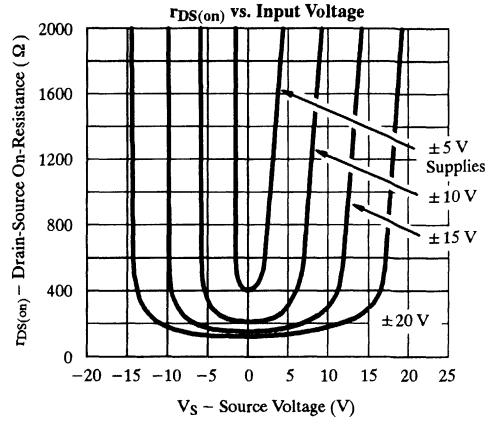
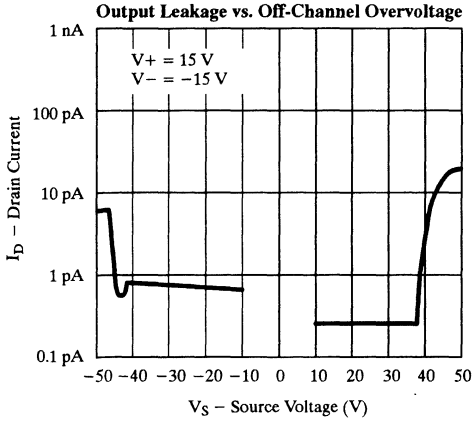
- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.
- g. When the analog signal exceeds the +13.5 V or -12 V,  $r_{DS(on)}$  starts to rise until only leakage currents flow.

h. 
$$\Delta r_{DS(on)} = \left( \frac{r_{DS(on) \text{ MAX}} - r_{DS(on) \text{ MIN}}}{r_{DS(on) \text{ AVE}}} \right) \times 100\%$$

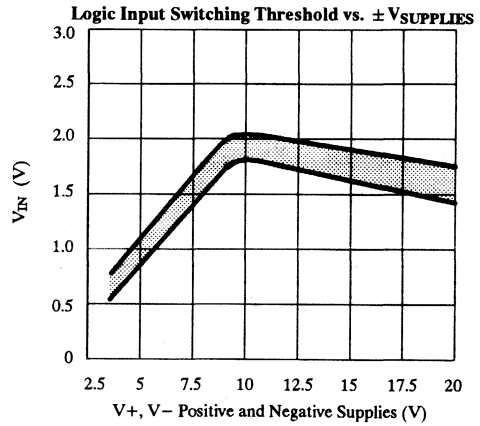
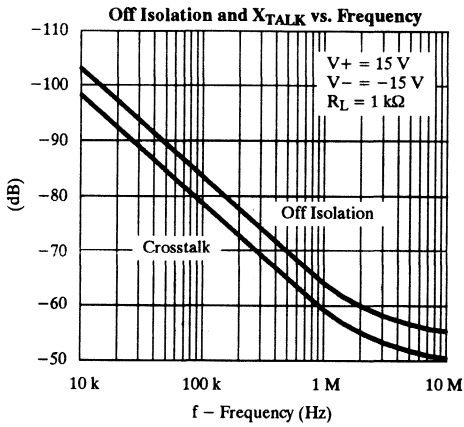
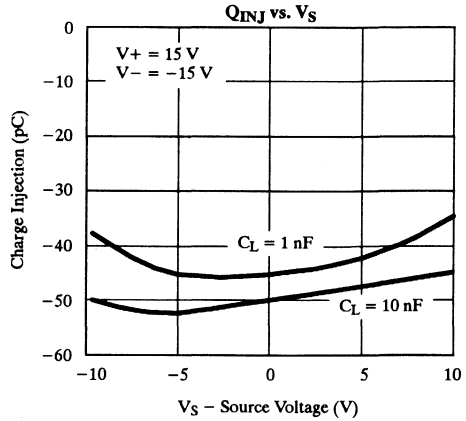
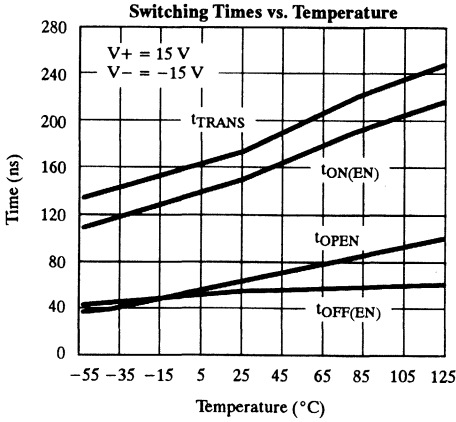
**Typical Characteristics**



## Typical Characteristics (Cont'd)



**Typical Characteristics (Cont'd)**



**Schematic Diagram (Typical Channel)**

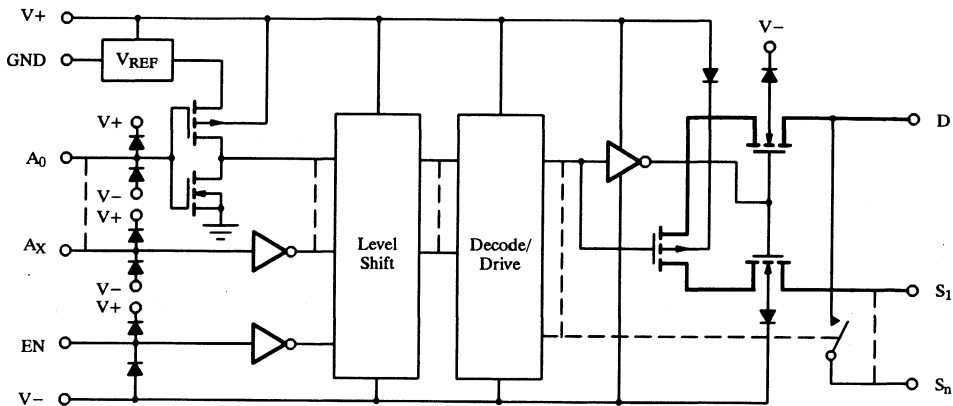


Figure 1.

## Test Circuits

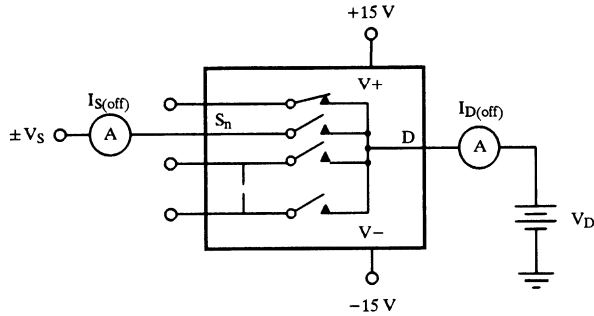
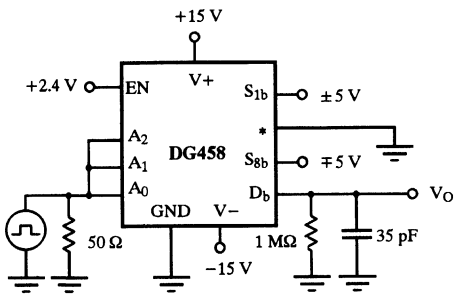


Figure 2. Analog Input Overvoltage



\* = S<sub>1a</sub> - S<sub>8a</sub>, S<sub>2b</sub> - S<sub>7b</sub>, D<sub>a</sub>

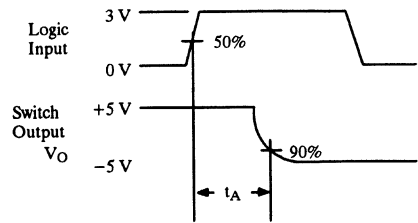


Figure 3. Transition Time

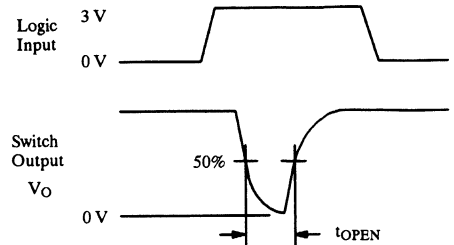
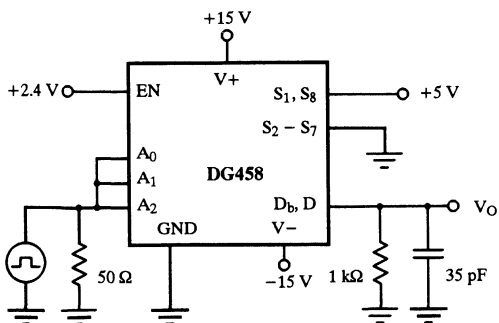


Figure 4. Break-Before-Make Time

**Test Circuits (Cont'd)**

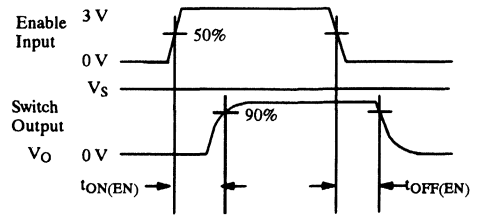
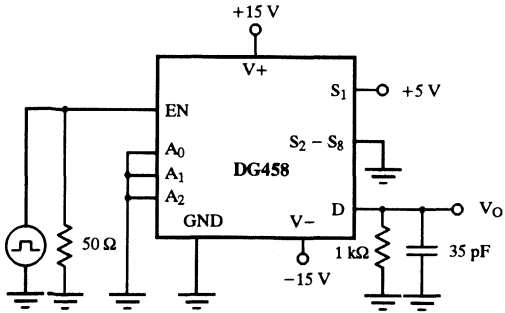


Figure 5. Enable Delay

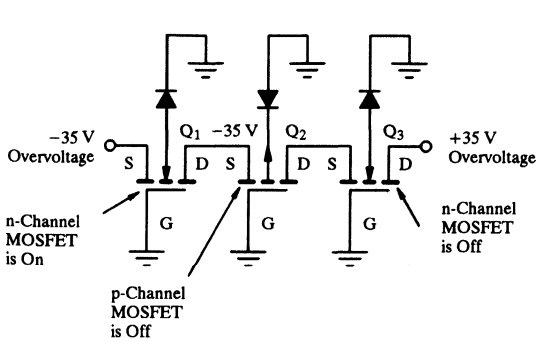
**Detailed Description**

The Siliconix DG458 and DG459 multiplexers are fully fault- and overvoltage-protected for continuous input voltages up to  $\pm 35$  V whether or not voltage is applied to the power supply pins (V+, V-). These multiplexers are built on a high-voltage junction-isolated silicon-gate CMOS process. Two n-channel and one p-channel MOSFETs are connected in series to form each channel (Figure 17).

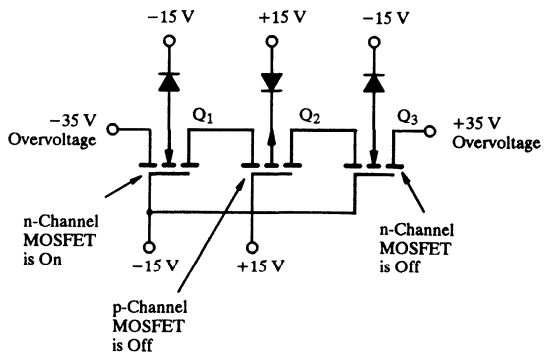
Within the normal analog signal range ( $\pm 10$  V), the  $r_{DS(on)}$  variation as a function of analog signal voltage is comparable to that of the classic parallel N-MOS and P-MOS switches.

When the analog signal approaches or exceeds either

supply rail, even for an on-channel, one of the three series MOSFETs gets cut-off, providing inherent protection against overvoltages even if the multiplexer power supply voltages are lost. This protection is good up to the breakdown voltage of the respective series MOSFETs. Under fault conditions only sub microamp leakage currents can flow in or out of the multiplexer. This not only provides protection for the multiplexer and succeeding circuitry, but it allows normal, undisturbed operation of all other channels. Additionally, in case of power loss to the multiplexer, the loading caused on the transducers and signal sources is insignificant, therefore redundant multiplexers can be used on critical applications such as telemetry and avionics.



(a) Overvoltage with Multiplexer Power Off



(b) Overvoltage with Multiplexer Power On

Figure 6. Overvoltage Protection

## Octal Analog Switch Array

### Features

- Low On-Resistance: 55  $\Omega$
- Rail-to-Rail Analog Input Range
- Serial Interface
- Low-Power— $P_D$ : 35 nW
- TTL and CMOS Compatible
- Any Combination of 8 SPST to the Output
- High Speed— $t_{ON}$ : 170 ns

### Benefits

- Low Signal Distortion
- Devices Can Be Chained for System Expansion
- Reduced Board Space
- Reduced Switch Errors
- Reduced Power Supply Requirements
- Simple Interfacing

### Applications

- Audio Switching and Routing
- Audio Teleconferencing
- Data Acquisition and Industrial Process Control
- Battery Powered Remote Systems
- Automotive, Avionics and ATE Systems
- Summing Amplifiers

## Description

The DG485 is an analog switch array consisting of eight SPST switches connected to a common output. This device may be used as an 8-channel multiplexer in serial control applications. Any, all or none of the eight switches may be closed at any given time. Combining low on-resistance ( $r_{DS(on)}$  55  $\Omega$ , typ.) and fast switching ( $t_{ON}$ : 170 ns, typ.), the DG485 is ideally suited for data acquisition, process control, communication, and avionic applications.

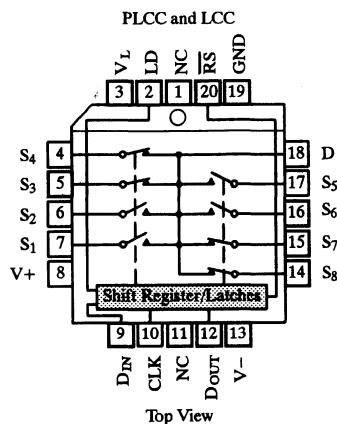
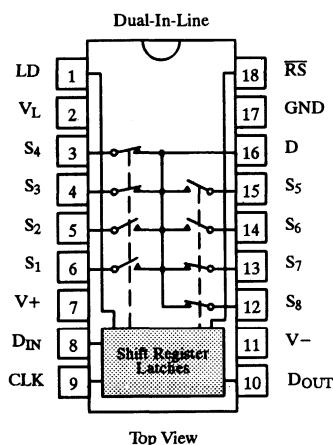
(via LD) at any point into an octal latch which in turn controls all switches.  $\overline{RS}$  resets the shift register, forcing all latch inputs to a low condition (all switches off). The serial input ( $D_{IN}$ ) and serial output ( $D_{OUT}$ ) allow daisy chaining of multiple arrays for large systems.

Built on the Siliconix high voltage silicon gate process the DG485 has a wide 44-V power supply voltage rating. An epitaxial layer prevents latchup.

Control data is input serially into the shift register with each clock pulse. The shift register contents can be latched-in

Each channel conducts equally well in either direction when on and blocks up to rail-to-rail voltages when off.

## Functional Block Diagrams and Pin Configurations





**Truth Tables and Ordering Information**

$\overline{RS}$	CLK*	$D_{IN}$	$D_1$	$D_n$
1		0	0	$D_{n-1}$
1		1	1	$D_{n-1}$
1		X	$D_1$	$D_n$ (No Change)
0	X	X	0	0

\*CLK Input Edge Triggered

LD*	$D_n$	$L_n$	$SW_n$
	0	0	OFF
	1	1	ON
	$D_n$	$L_n$	(No Change)

\*LD Input Level Triggered

**Ordering Information**

Temp Range	Package	Part Number
-40 to 85°C	18-Pin Plastic DIP	DG485DJ
	20-Pin PLCC	DG485DN
-55 to 125°C	LCC-20	DG485AZ/883

**Absolute Maximum Ratings**

Voltages Referenced to V-

V+	44 V
GND	25 V
Digital Inputs <sup>a</sup> $V_S, V_D$	(V-) -2 V to (V+) + 2 V or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle)	100 mA
Storage Temperature (AZ Suffix)	-65 to 150°C
(DJ, DN Suffix)	-65 to 125°C

Power Dissipation (Package)<sup>b</sup>

18-Pin Plastic DIP <sup>c</sup>	470 mW
20-Pin PLCC, LCC <sup>d</sup>	800 mW

Notes:

- Signals on  $S_X, D_X$  or  $IN_X$  exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 6 mW/°C above 75°C.
- Derate 10 mW/°C above 75°C.

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified  V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V, V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
					<b>Analog Switch</b>				
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>+</sub> = 13.5 V, V <sub>-</sub> = -13.5 V I <sub>S</sub> = -5 mA, V <sub>D</sub> = ±10 V	Room Full	55		85 125		85 125	Ω
Delta Drain-Source On-Resistance <sup>g</sup>	Δr <sub>DS(on)</sub>		Room	6					%
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ±15.5 V	Room Full	0.01	-1 -20	1 20	-1 -10	1 10	nA
	I <sub>D(off)</sub>		Room Full	0.1	-10 -200	10 200	-10 -50	10 50	
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>±</sub> = ±16.5 V, V <sub>S</sub> = V <sub>D</sub> = ±15.5 V One Switch At A Time	Room Full	0.11	-20 -500	20 500	-20 -50	20 50	nA
			Room	0.2					
<b>Input</b>									
Input Current with V <sub>IN</sub> Low	I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0.8 V All Other = 2.4 V	Room Full	-0.0001	-1 -5	1 5	-1 -5	1 5	μA
Input Current with V <sub>IN</sub> High	I <sub>IH</sub>	V <sub>IN</sub> Under Test = 2.4 V All Other = 0.8 V	Room Full	0.0001	-1 -5	1 5	-1 -5	1 5	
<b>Serial Data Output</b>									
Output Voltage with V <sub>IN</sub> Low - D <sub>OUT</sub>	V <sub>OL</sub>	I <sub>O</sub> = 1.6 mA, V <sub>+</sub> = 4.5 V	Full	0.25		0.4		0.4	V
Output Voltage with V <sub>IN</sub> High - D <sub>OUT</sub>	V <sub>OH</sub>	I <sub>O</sub> = -80 μA, V <sub>+</sub> = 16.5 V V <sub>L</sub> = 4.75 V	Full	4.4	2.7		2.7		
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	V <sub>S</sub> = ±10 V See Figures 1, 8	Room Full	170		200 275		200 275	ns
Turn-Off Time	t <sub>OFF</sub>	V <sub>S</sub> = ±10 V See Figures 2, 3, 8	Room Full	150		200 275		200 276	
Data Setup Time	t <sub>DS</sub>	See Figures 4, 8	Room Full		40 60		40 60		
Data Hold Time	t <sub>DH</sub>		Room Full		40 60		40 60		
LOAD Hold Time	t <sub>LH</sub>	See Figures 5, 8	Room Full		100 150		100 150		
RESET Hold Time	t <sub>RH</sub>		Room Full		100 150		100 150		
RESET ↑ to CLOCK ↑ Delay	t <sub>DRC</sub>		Room Full		40 60		40 60		
Charge Injection	Q	V <sub>S</sub> = 0 V, C <sub>L</sub> = 1,000 pF Any One Channel	Room	17					pC
Off Isolation <sup>e</sup>	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz See Figure 9	Room	-75					dB

**Specifications<sup>a</sup>**

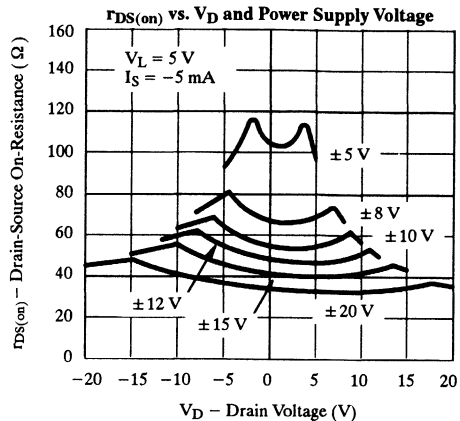
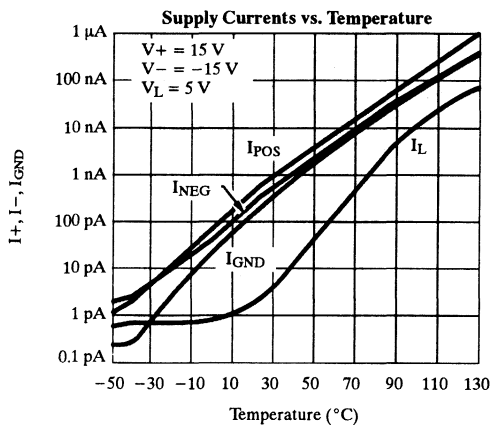
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Dynamic Characteristics (Cont'd)</b>									
Maximum Clock Frequency	$f_{CLK}$		Room	10					MHz
Source Off Capacitance <sup>e</sup>	$C_{S(off)}$	$V_{gen} = 0\text{ V}, R_{gen} = 0\ \Omega, f = 1\text{ MHz}$	Room	7					pF
Drain Off Capacitance <sup>e</sup>	$C_{D(off)}$		Room	43					
On-State Capacitance <sup>e</sup>	$C_{D(on)}$	$V_{gen} = 0\text{ V}, R_{gen} = 0\ \Omega, f = 1\text{ MHz}$ One Channel On	Room	53					
		$V_{gen} = 0\text{ V}, R_{gen} = 0\ \Omega, f = 1\text{ MHz}$ All Channels On	Room	122					
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}, V_L = 5.25\text{ V}$ D <sub>OUT</sub> Open	Room Full	0.001		3 10		3 10	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Full	-0.001	-3 -10		-3 -10		
Logic Supply Current	$I_L$		Room Full	0.001		3 10		3 10	
Ground Current	$I_{GND}$		Room Full	-0.001	-3 -10		-3 -10		

Notes:

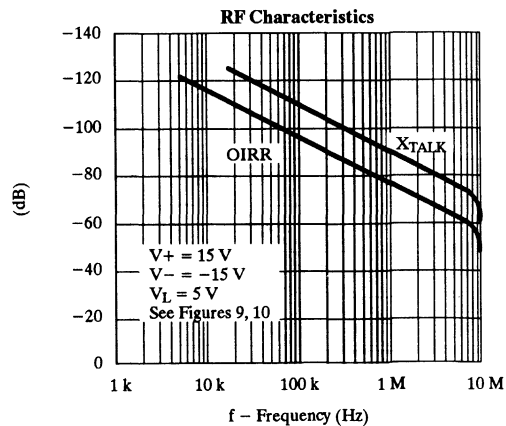
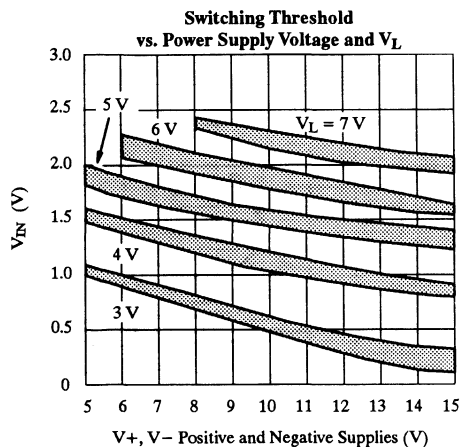
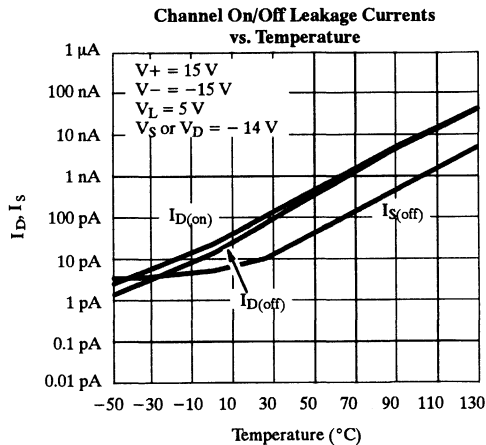
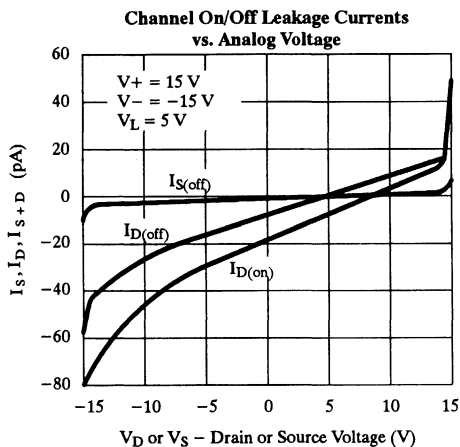
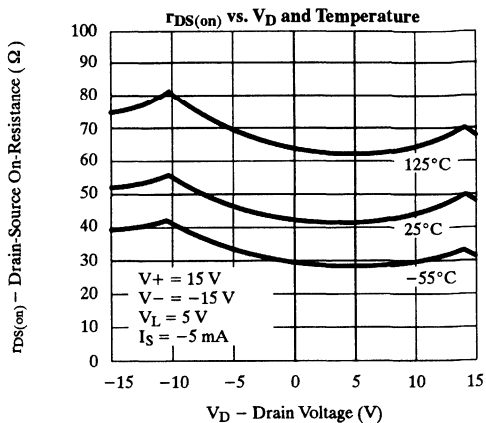
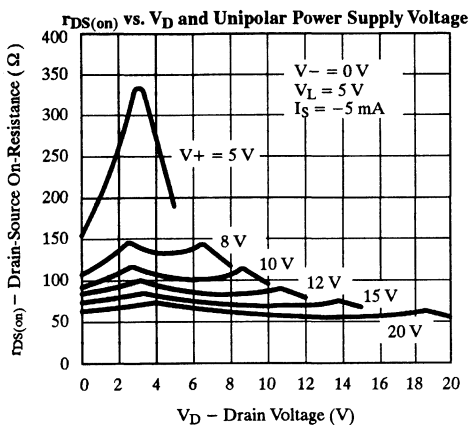
- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

g. For each  $V_D$ :  $\Delta r_{DS(on)} = \left( \frac{r_{DS(on)\text{ MAX}} - r_{DS(on)\text{ MIN}}}{r_{DS(on)\text{ AVE}}} \right)$

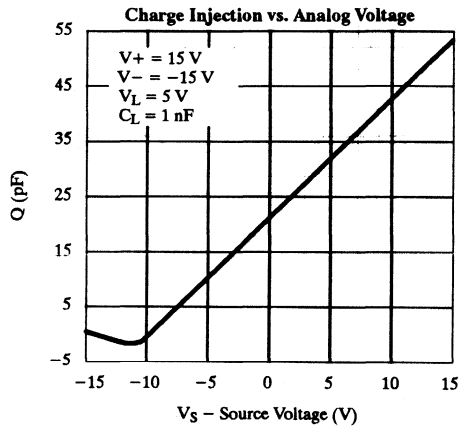
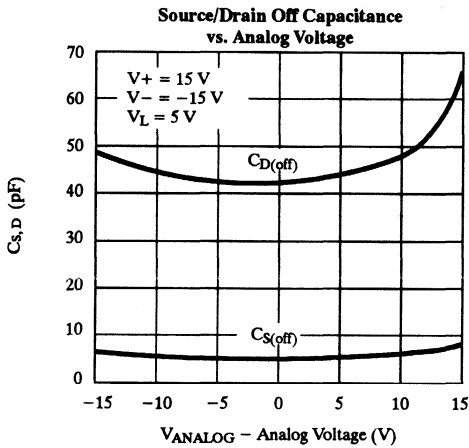
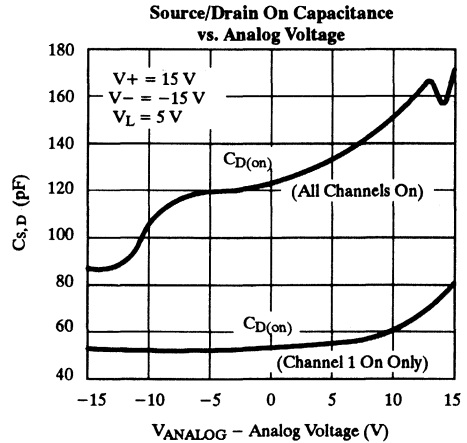
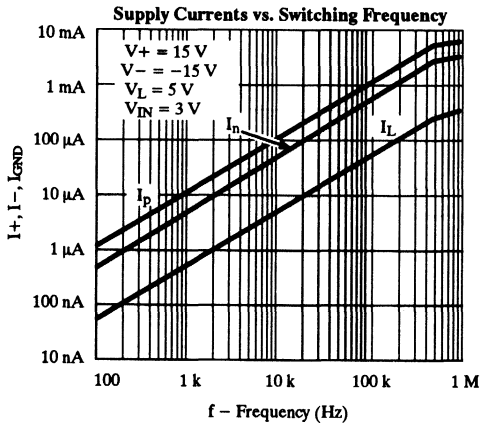
**Typical Characteristics**



## Typical Characteristics (Cont'd)



**Typical Characteristics (Cont'd)**



**Timing Diagrams**

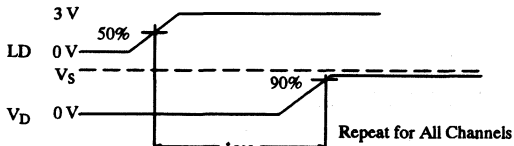


Figure 1.  $t_{ON}$  from LD

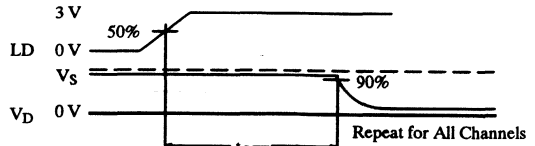


Figure 2.  $t_{OFF}$  from LD

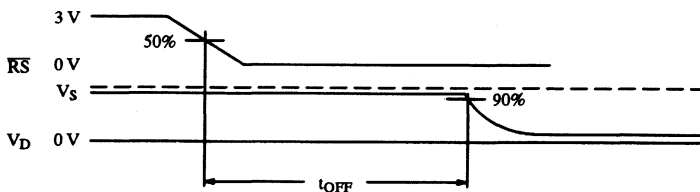


Figure 3.  $t_{OFF}$  from  $\overline{RS}$

## Timing Diagrams (Cont'd)

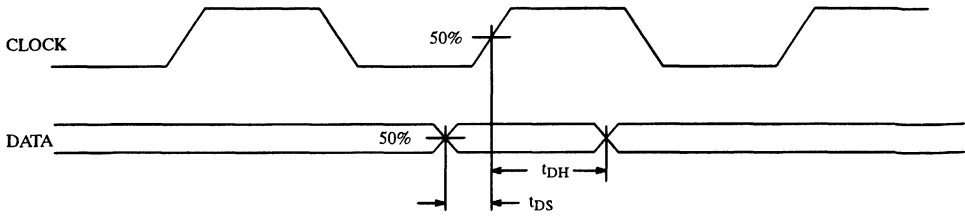


Figure 4. Data Setup and Hold Time

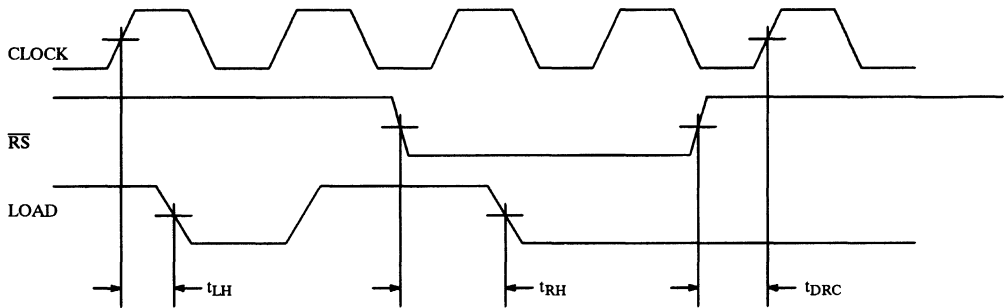
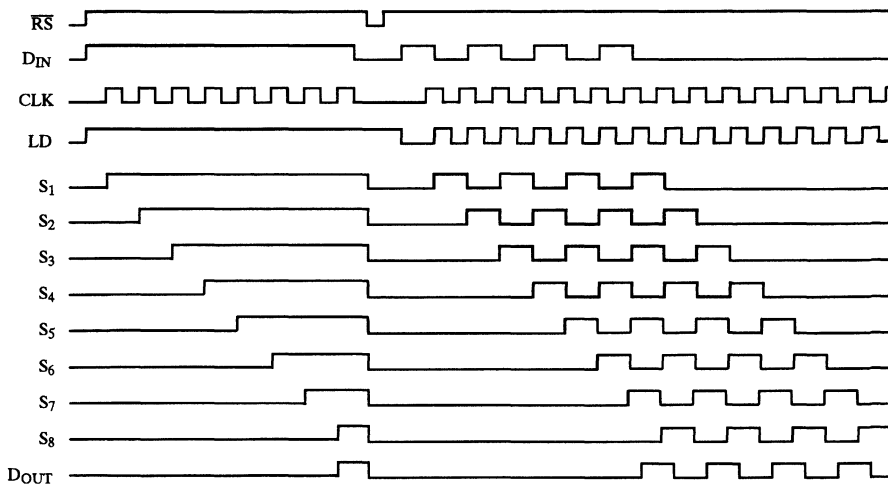


Figure 5. Timing Relationships



$S_1 - S_8$  and  $D_{OUT}$  are expected output with the drain connected high. The sources require pull-down of  $1\text{ k}\Omega$

Figure 6.

**Schematic Diagram (Typical Channel)**

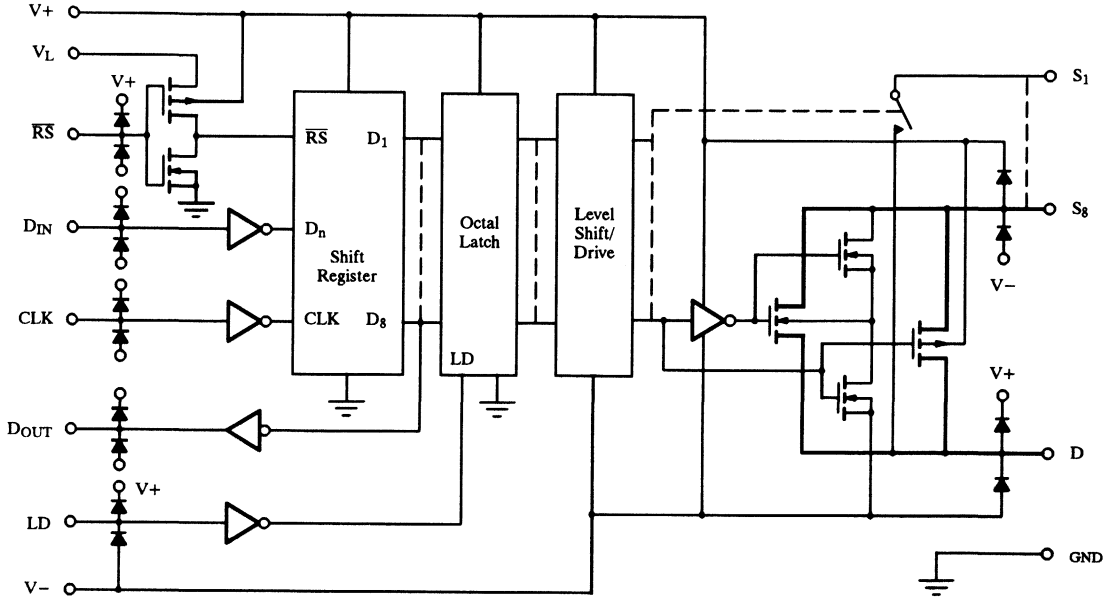


Figure 7.

**Test Circuits**

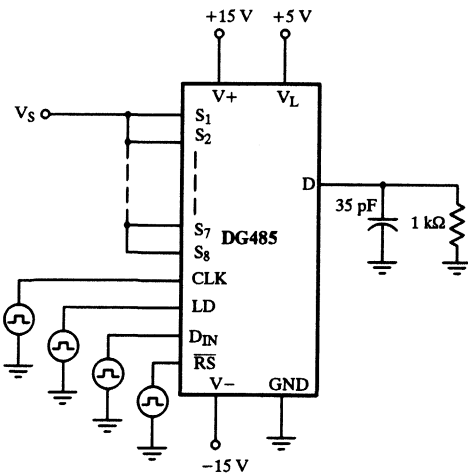


Figure 8. Switching Time Test Circuit

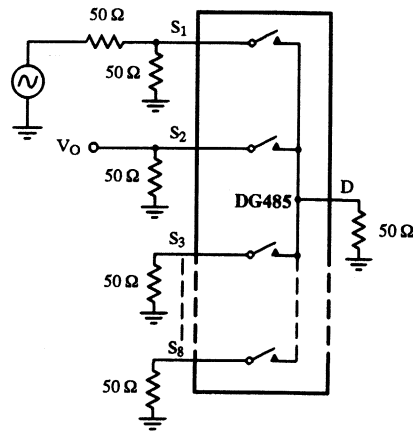
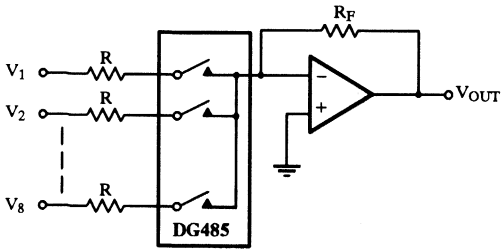


Figure 9. Adjacent Input Crosstalk

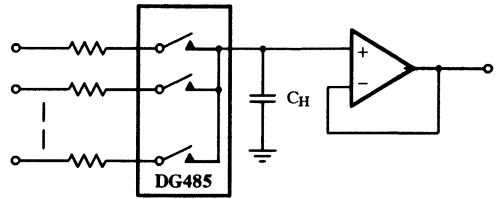




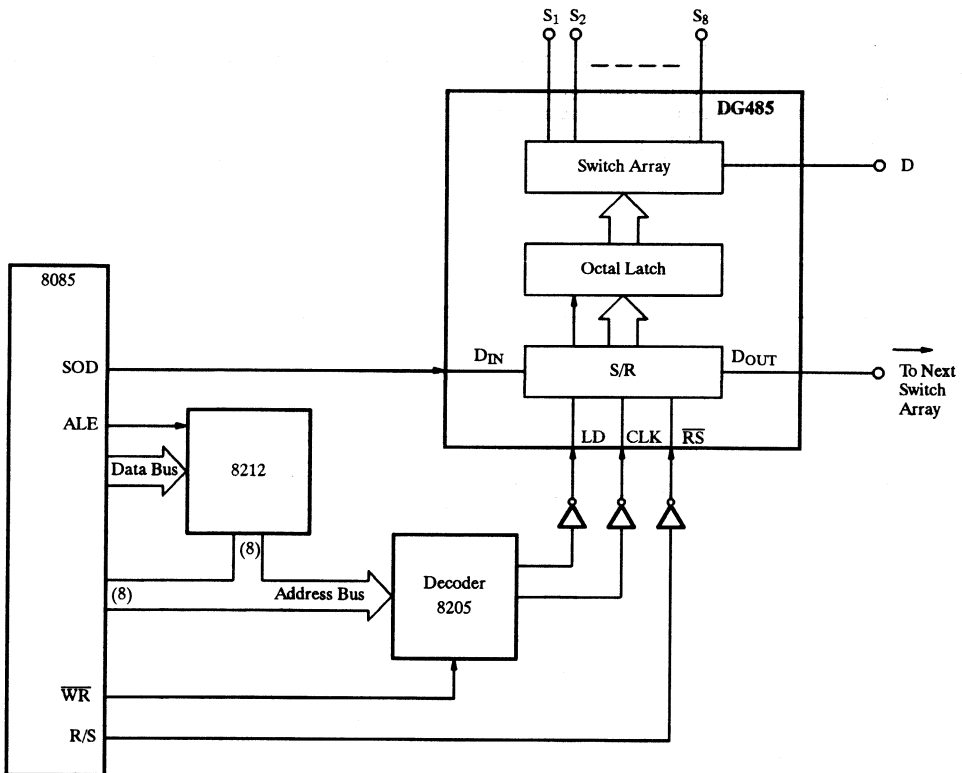
**Applications (Cont'd)**



**Figure 14.** Summing Node Mixer



**Figure 15.** Multiplexing, Sampling Application



**Figure 16.** Direct Serial Interface (8085)

## Single 16-Channel/Differential 8-Channel CMOS Analog Multiplexers

### Features

- Low On-Resistance: 240  $\Omega$
- TTL and CMOS Logic Compatible
- Low Power: 30 mW
- Break-Before-Make Switching
- 44-V Power Supply Rating
- Transition Time: 600 ns

### Benefits

- Easily Interfaced
- Low Power Consumption
- Low System Crosstalk
- Wide Analog Signal Range

### Applications

- Communication Systems
- ATE
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing
- Medical Instrumentation

### Description

The DG506A, a 16-channel single-ended analog multiplexer, is designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address ( $A_0, A_1, A_2, A_3$ ). The DG507A, a differential 8-channel analog multiplexer, is designed to connect one of eight differential inputs to a common differential outputs as determined by its 3-bit binary address ( $A_0, A_1, A_2$ ) logic. Break-before-make switching action protects against momentary shorting of the input signals.

voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows for device selection when several multiplexers are used. All control inputs, address ( $A_x$ ) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

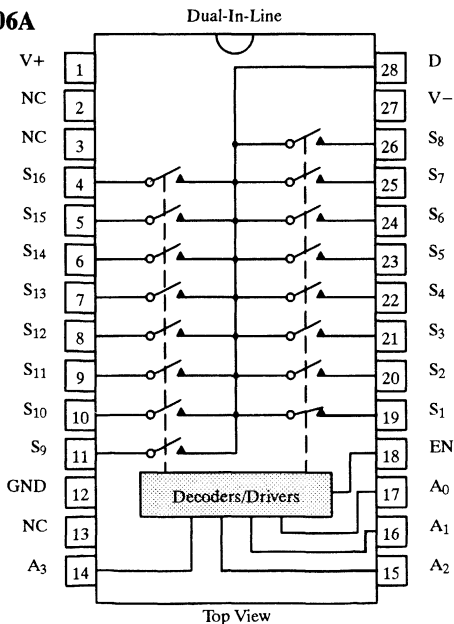
The DG506A/507A are fabricated in the Siliconix PLUS-40 process, which includes improved ESD protection for ruggedness. An epitaxial layer prevents latch up.

A channel in the on state conducts current equally well in both directions. In the off state each channel blocks

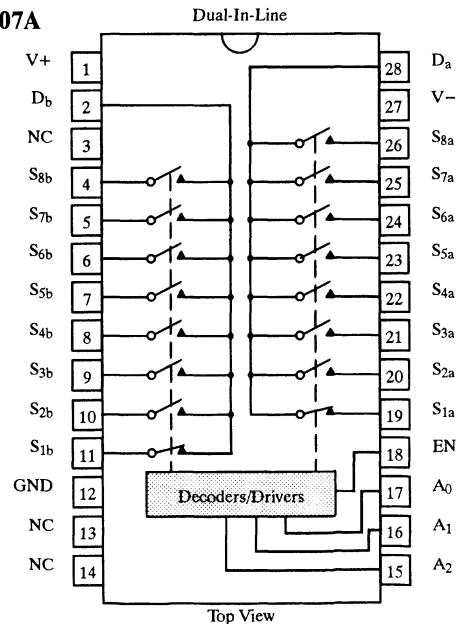
For wideband/video multiplexing, the DG536 is recommended.

### Functional Block Diagrams and Pin Configurations

**DG506A**



**DG507A**



## Functional Block Diagrams and Pin Configurations

Truth Table — DG506A

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Truth Table — DG507A

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" =  $V_{AL} \leq 0.8\text{ V}$   
 Logic "1" =  $V_{AH} \geq 2.4\text{ V}$   
 X = Don't Care

Ordering Information — DG506A

Temp Range	Package	Part Number
0 to 70°C	28-Pin Plastic DIP	DG506ACJ
	28-Pin CerDIP	DG506ACK
		DG506ABK
-25 to 85°C	28-Pin PLCC	DG506ADN
-40 to 85°C		DG506AAK
-55 to 125°C	28-Pin CerDIP	DG506AAK/883
		28-Pin Sidebrazed
	LCC-20*	DG506AAZ/883

Ordering Information — DG507A

Temp Range	Package	Part Number
0 to 70°C	28-Pin Plastic DIP	DG507ACJ
-55 to 125°C	28-Pin CerDIP	DG507AAK
		DG507AAK/883
	28-Pin Sidebrazed	JM38510/19003BXC
	28-Pin LCC	DG507AAZ/883

\*Block Diagram and Pin Configuration not shown.

## Absolute Maximum Ratings

Voltage Referenced to V-

V+	44 V
GND	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal, Except S or D)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Storage Temperature (CerDIP)	-65 to 150°C
(Plastic DIP)	-65 to 125°C

Power Dissipation (Package)<sup>b</sup>

28-Pin Plastic DIP <sup>c</sup>	625 mW
28-Pin CerDIP and Sidebrazed	1200 mW
28-Pin PLCC <sup>c</sup>	1200 mW
LCC-20,28 <sup>d</sup>	1000 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub> or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 8.3 mW/°C above 75°C.
- Derate 14 mW/°C above 75°C.

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified  $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C, D Suffix 0 to 70°C -25 to 85°C -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-15	15	-15	15	V	
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}, I_S = -200\ \mu\text{A}$	Room Full	240		400 500		450 550	$\Omega$	
$r_{DS(on)}$ Matching <sup>g</sup>	$\Delta r_{DS(on)}$	$-10\text{ V} < V_S < 10\text{ V}$	Room	6					%	
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 10\text{ V}, V_D = \mp 10\text{ V}$ $V_{EN} = 0\text{ V}$	Room Full		-1 -50	1 50	-5 -50	5 50		
Drain Off Leakage Current	$I_{D(off)}$	$V_D = \mp 10\text{ V}$ $V_S = \pm 10\text{ V}$ $V_{EN} = 0\text{ V}$	DG506A	Room Full		-10 -300	10 300	-20 -300	20 300	nA
			DG507A	Room Full		-5 -200	5 200	-10 -200	10 200	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 10\text{ V}$	DG506A	Room Full		-10 -300	10 300	-20 -300	20 300	
			DG507A	Room Full		-5 -200	5 200	-10 -200	10 200	
<b>Digital Control</b>										
Logic Input Current Input Voltage High	$I_{AH}$	$V_A = 2.4\text{ V}$	Room Full		-10 -30		-10 -30		$\mu\text{A}$	
		$V_A = 15\text{ V}$	Room Full			10 30		10 30		
Logic Input Current Input Voltage Low	$I_{AL}$	$V_{EN} = 0\text{ V}, 2.4\text{ V}, V_A = 0\text{ V}$	Room Full		-10 -30		-10 -30			
<b>Dynamic Characteristics</b>										
Transition Time	$t_{TRANS}$	See Figure 2	Room	0.6		1			$\mu\text{s}$	
Break-Before-Make Time	$t_{OPEN}$	See Figure 4	Room	0.2						
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3	Room	1						
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	0.4						
Charge Injection	Q		Room	6					pC	
Off Isolation <sup>h</sup>	OIRR	$V_{EN} = 0\text{ V}, R_L = 1\text{ k}\Omega, C_L = 15\text{ pF}$ $V_S = 7\text{ V}_{RMS}, f = 500\text{ kHz}$	Room	68					dB	
Source Off Capacitance	$C_{S(off)}$	$V_{EN} = 0\text{ V}, V_S = 0\text{ V}, f = 140\text{ kHz}$	Room	6					pF	
Drain Off Capacitance	$C_{D(off)}$	$V_{EN} = 0\text{ V}, V_D = 0\text{ V}$ $f = 140\text{ kHz}$	DG506A	Room	45					
			DG507A	Room	23					
<b>Power Supplies</b>										
Positive Supply Current	I+	$V_{EN} = 0\text{ V}, V_A = 0\text{ V}$	Room	1.3		2.4		2.4	mA	
Negative Supply Current	I-		Room	-0.7	-1.5		-1.5			

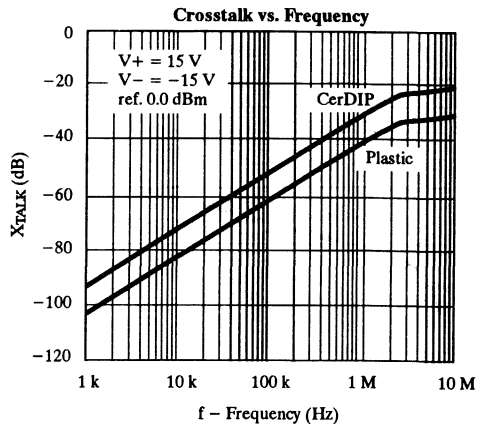
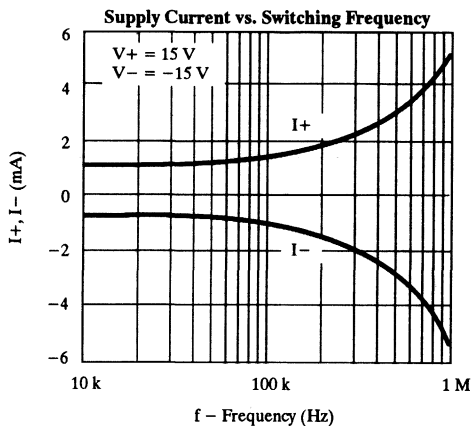
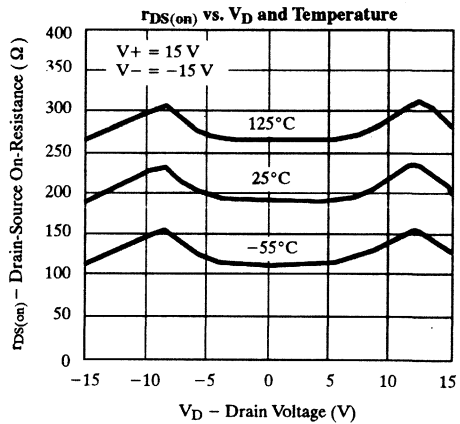
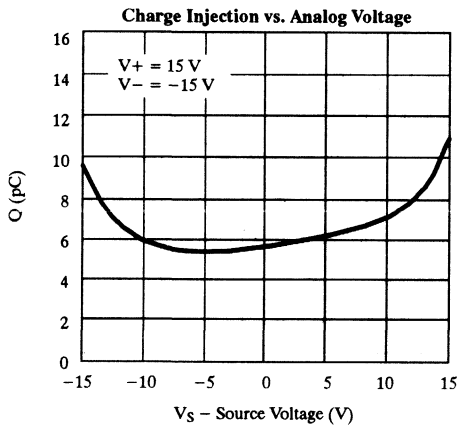
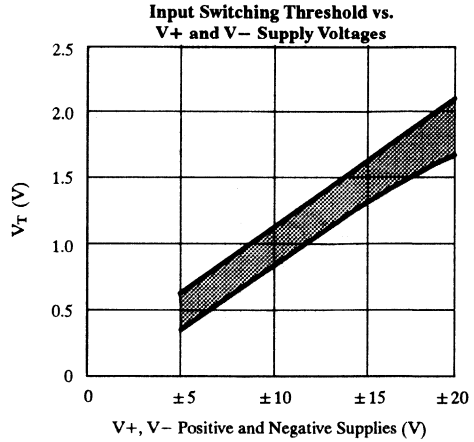
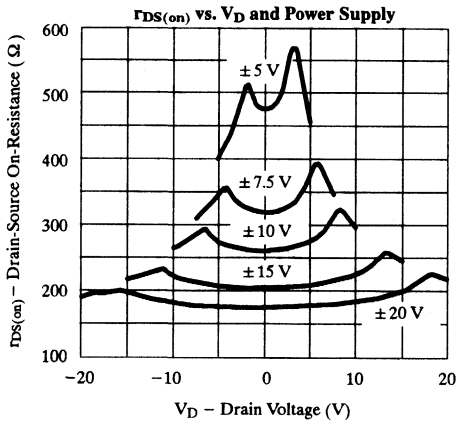
**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

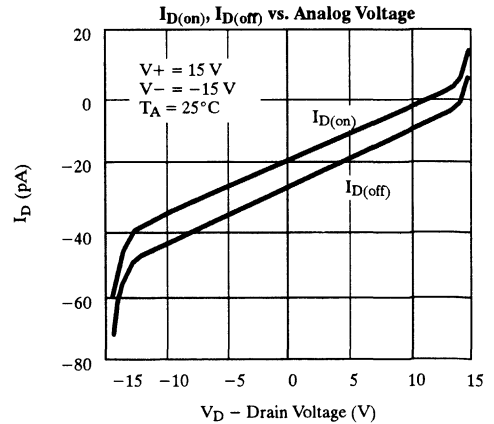
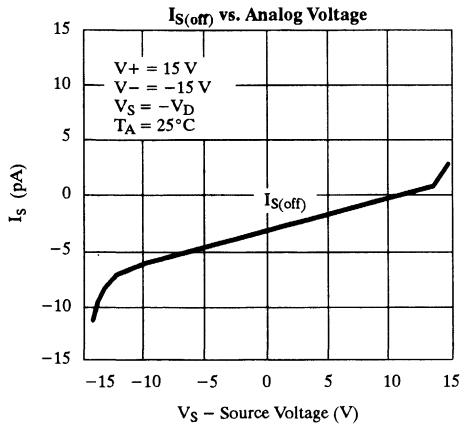
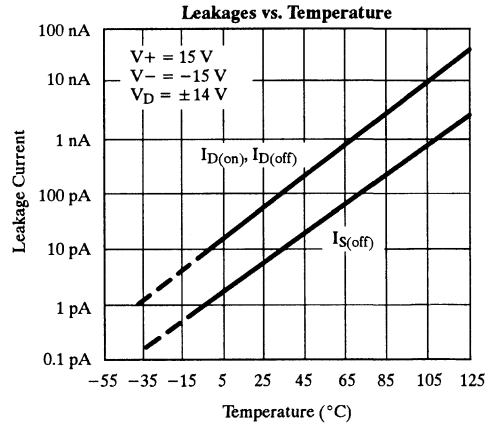
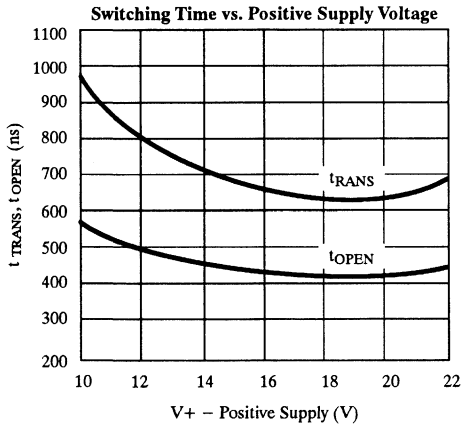
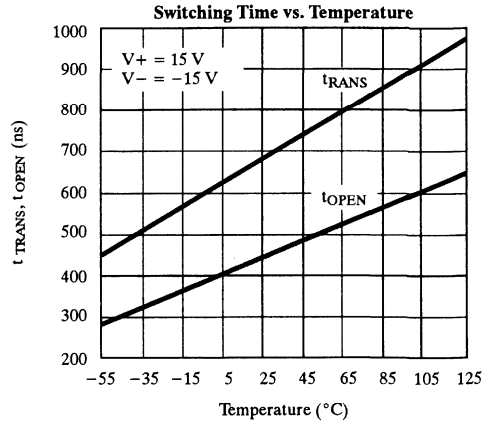
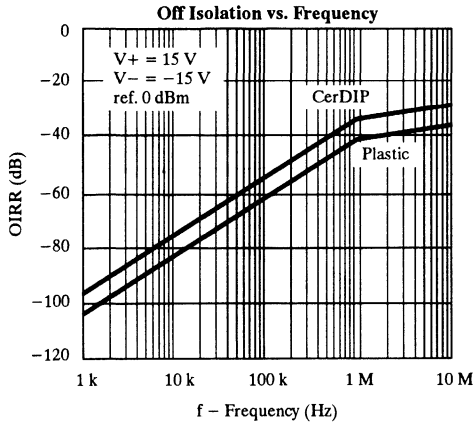
$$g. \Delta r_{DS(on)} = \left( \frac{r_{DS(on)MAX} - r_{DS(on)MIN}}{r_{DS(on)AVE}} \right)$$

- Off isolation =  $20 \log \frac{V_D}{V_S}$ ,  $V_S$  = input to off switch,  $V_D$  = output due to  $V_S$ .

**Typical Characteristics**



## Typical Characteristics (Cont'd)



**Schematic Diagram (Typical Channel)**

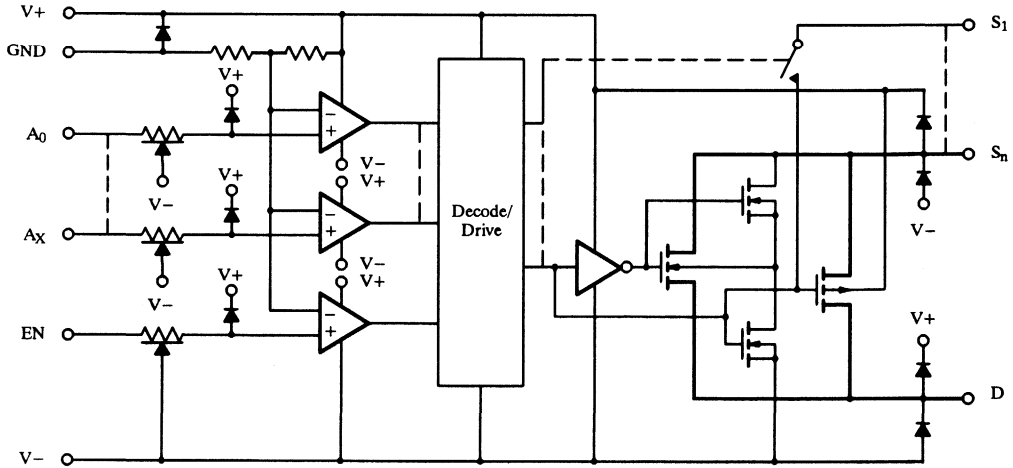
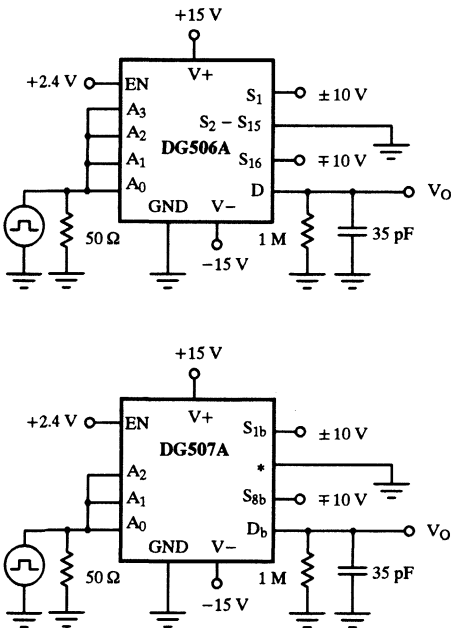


Figure 1.

**Test Circuits**



\* = S<sub>1a</sub> - S<sub>8a</sub>, S<sub>2b</sub> - S<sub>7b</sub>, D<sub>a</sub>

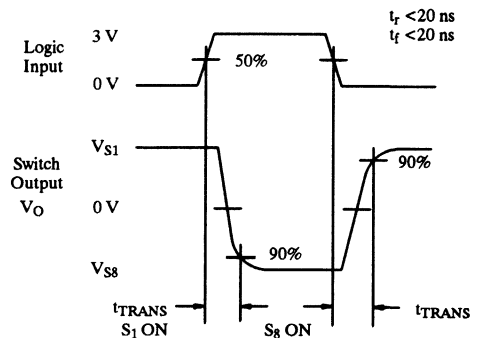


Figure 2. Transition Time

## Test Circuits (Cont'd)

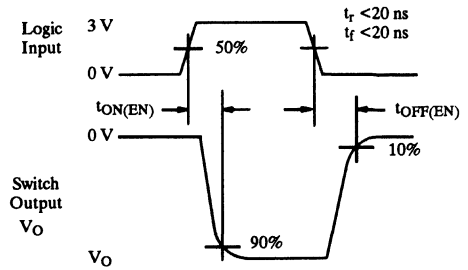
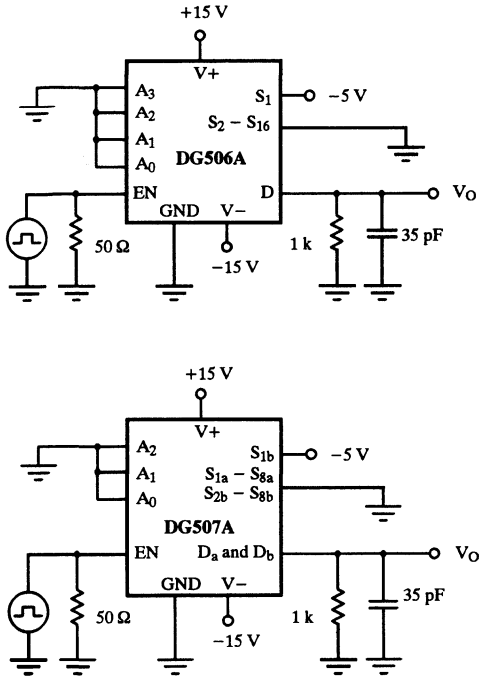


Figure 3. Enable Switching Time

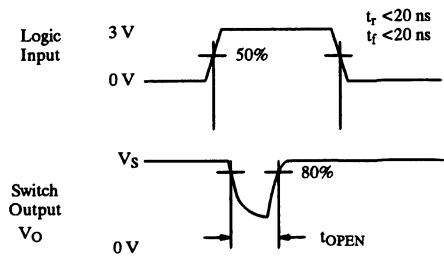
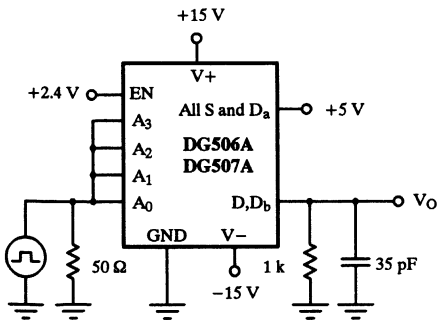


Figure 4. Break-Before-Make Interval



**Application Hints<sup>a</sup>**

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15 <sup>b</sup>	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.8	-12 to 12
10	-10	2.2/0.6	-10 to 10
8 <sup>c</sup>	-8	2.0/0.5	-8 to 8

Notes:

- a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- b. Electrical Parameter Chart based on V+ = 15 V, V- = -15 V.
- c. Operation below ± 8 V is not recommended due to shift in V<sub>INL(MAX)</sub>.

**Applications**

**Overvoltage Protection**

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 5). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V<sub>S</sub> and the V- rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

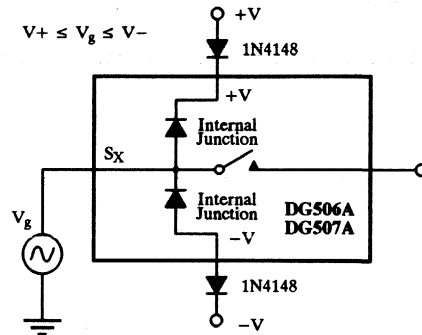


Figure 5. Overvoltage Protection Using Blocking Diodes

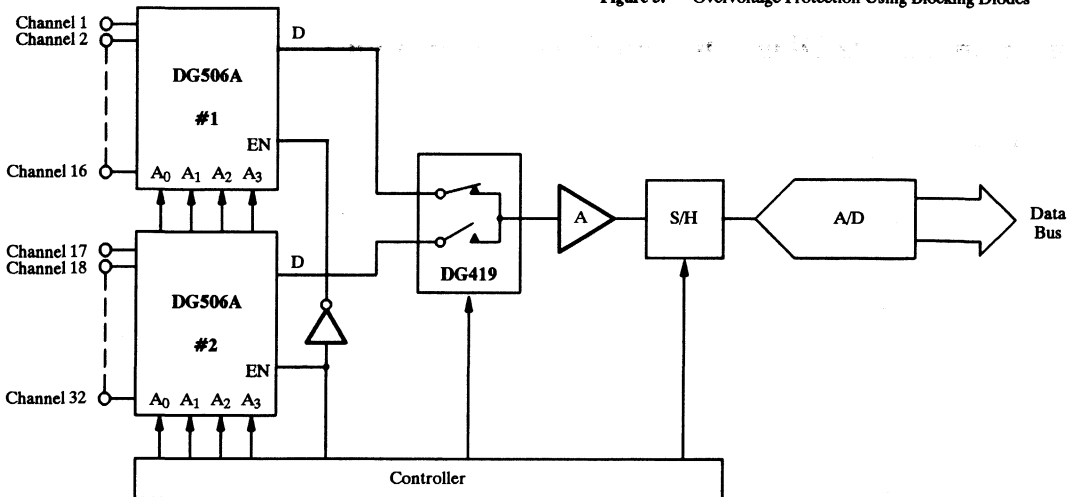


Figure 6. A 32-Channel Data Acquisition System

## Single 8-Channel/Differential 4-Channel CMOS Analog Multiplexers

### Features

- Low On-Resistance: 240  $\Omega$
- TTL and CMOS Logic Compatible
- Low Power: 30 mW
- Break-Before-Make Switching
- 44-V Power Supply Rating
- Transition Time: 600 ns

### Benefits

- Easily Interfaced
- Low Power Consumption
- Low System Crosstalk
- Wide Analog Signal Range

### Applications

- Communication Systems
- ATE
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing
- Medical Instrumentation

### Description

The DG508A, an 8-channel single-ended analog multiplexer, is designed to connect one of eight inputs to a common output as determined by a 3-bit binary address ( $A_0, A_1, A_2$ ).

The DG509A, a dual 4-channel analog multiplexer, is designed to connect one of four differential inputs to a common output as determined by its 2-bit binary address ( $A_0, A_1$ ) logic. Break-before-make switching action protects against momentary shorting of the input signals.

A channel in the on state conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows for device

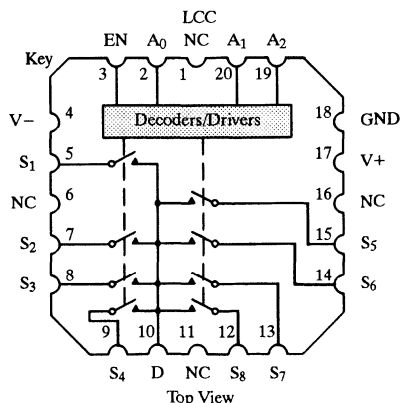
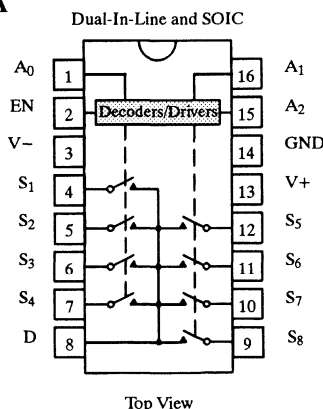
selection when several multiplexers are used. All control inputs, address ( $A_X$ ) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

Fabricated in the Siliconix Plus-40 process, the absolute maximum voltage rating is extended to 44 V, allowing increased operating headroom for standard  $\pm 15$ -V signal swings and operation with  $\pm 20$ -V supplies. An epitaxial layer prevents latch up.

For applications requiring address data latching, the DG528/529 is recommended. DG408/409 is recommended for higher precision applications. For wideband/video routing and multiplexing, the DG538A is recommended.

## Functional Block Diagrams and Pin Configurations

### DG508A



## Functional Block Diagrams and Pin Configurations (Cont'd)

Ordering Information – DG508A

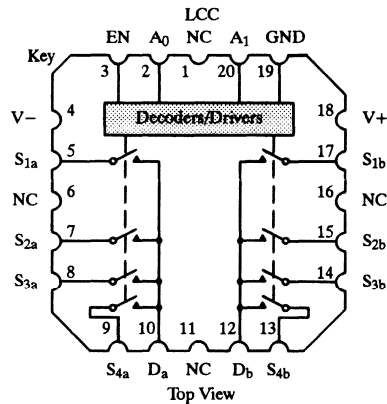
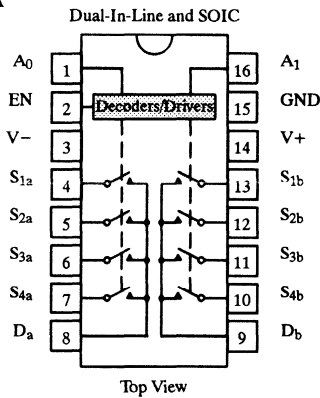
Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG508ACJ
-25 to 85°C	16-Pin CerDIP	DG508ABK
-40 to 85°C	16-Pin Narrow SOIC	DG508ADY
-55 to 125°C	16-Pin CerDIP	DG508AAK
		DG508AAK/883
	LCC-20	DG508AAZ/883
	16-Pin Sidebrazed	7705201EA
		7705201EC
	16-Pin Flat Pack	7705201FA
		7705201FC
	16-Pin Sidebrazed	JM38510/19007BEA
JM38510/19007BEC		

Truth Table — DG508A

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = V<sub>AL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>AH</sub> ≥ 2.4 V  
 X = Don't Care

### DG509A



Ordering Information – DG509A

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG509ACJ
-25 to 85°C	16-Pin CerDIP	DG509ABK
-40 to 85°C	16-Pin Narrow SOIC	DG509ADY
-55 to 125°C	16-Pin CerDIP	DG509AAK
		DG509AAK/883
	LCC-20	DG509AAZ/883
	16-Pin Sidebrazed	JM38510/19008BEA
		JM38510/19008BEC

Truth Table — DG509A

A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = V<sub>AL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>AH</sub> ≥ 2.4 V  
 X = Don't Care

## Absolute Maximum Ratings

Voltage Referenced to V-	
V+	44 V
GND	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal, Except S or D)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Storage Temperature (K Suffix)	-65 to 150°C
(J and Y Suffix)	-65 to 125°C

Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup>	470 mW
16-Pin Narrow SOIC <sup>c</sup>	600 mW
16-Pin CerDIP <sup>d</sup>	900 mW
LCC-20 <sup>d</sup>	900 mW

**Notes:**

- Signals on S<sub>X</sub>, D<sub>X</sub> or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 6.3 mW/°C above 75°C.
- Derate 12 mW/°C above 75°C.

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup>		Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
						Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>			Full		-15	15	-15	15	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>D</sub> = ±10 V, I <sub>S</sub> = -200 μA		Room Full	240		400 500		450 550	Ω
r <sub>DS(on)</sub> Match	Δr <sub>DS(on)</sub>	-10 V < V <sub>S</sub> < 10 V		Room	6					%
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>EN</sub> = 0 V, V <sub>S</sub> = ±10 V V <sub>D</sub> = ∓10 V		Room Full		-1 -50	1 50	-5 -50	5 50	
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>EN</sub> = 0 V V <sub>D</sub> = ±10 V V <sub>S</sub> = ∓10 V	DG508A	Room Full		-10 -200	10 200	-20 -200	20 200	nA
			DG509A	Room Full		-10 -100	10 100	-20 -100	20 100	
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = ±10 V	DG508A	Room Full		-10 -200	10 200	-20 -200	20 200	
			DG509A	Room Full		-10 -100	10 100	-20 -100	20 100	
<b>Digital Control</b>										
Logic Input Current Input Voltage High	I <sub>AH</sub>	V <sub>A</sub> = 2.4 V		Room Full	-0.002	-10 -30		-10 -30		μA
		V <sub>A</sub> = 15 V		Room Full	0.006		10 30		10 30	
Logic Input Current Input Voltage Low	I <sub>AL</sub>	V <sub>EN</sub> = 0 V, 2.4 V, V <sub>A</sub> = 0 V		Room Full	-0.002	-10 -30		-10 -30		
<b>Dynamic Characteristics</b>										
Transition Time	t <sub>TRANS</sub>	See Figure 2		Room	0.6		1			μs
Break-Before-Make Time	t <sub>OPEN</sub>	See Figure 4		Room	0.2					
Enable Turn-On Time	t <sub>ON(EN)</sub>	See Figure 3		Room	1		1.5			
Enable Turn-Off Time	t <sub>OFF(EN)</sub>		Room	0.4		1.0				
Charge Injection	Q	See Figure 5		Room	6					pC
Off Isolation	OIRR	V <sub>EN</sub> = 0 V, R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 15 pF V <sub>S</sub> = 7 V <sub>RMS</sub> , f = 500 kHz		Room	68					dB
Logic Input Capacitance	C <sub>in</sub>	f = 1 MHz		Room	8					pF
Source Off Capacitance	C <sub>S(off)</sub>	V <sub>EN</sub> = 0 V, V <sub>S</sub> = 0 V, f = 140 kHz		Room	6					
Drain Off Capacitance	C <sub>D(off)</sub>	V <sub>EN</sub> = 0 V, V <sub>D</sub> = 0 V f = 140 kHz	DG508A	Room	25					
			DG509A	Room	12					

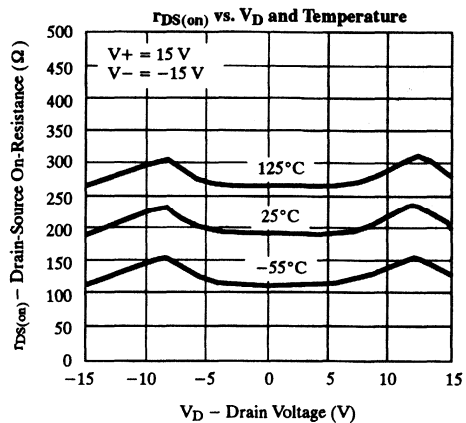
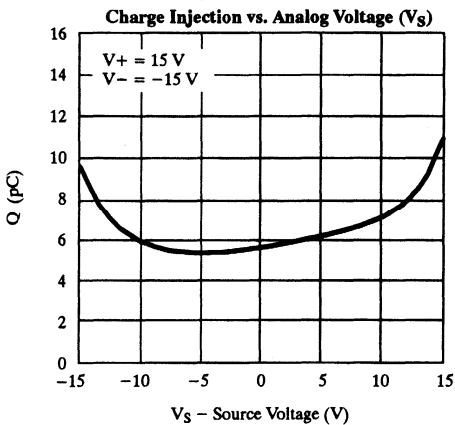
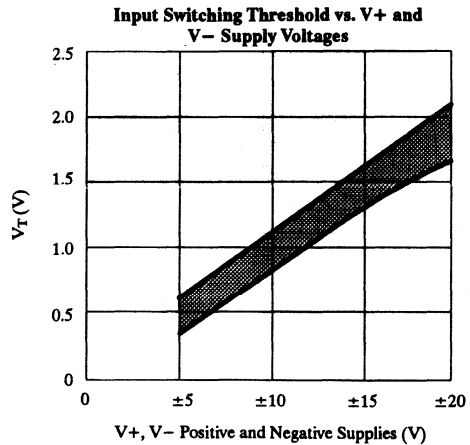
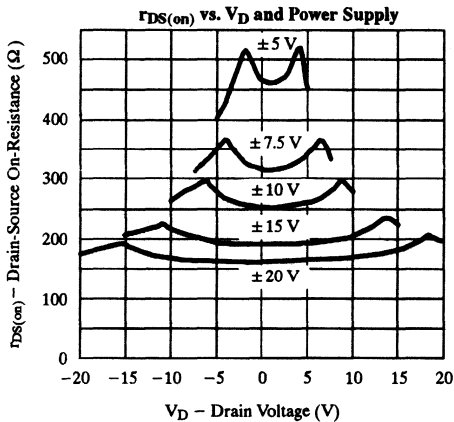
**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V+ = 15\text{ V}, V- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_{EN} = 0\text{ V or } 2.4\text{ V}$	Room	1.3		2.4		2.4	mA
Negative Supply Current	I-		Room	-0.7	-1.5		-1.5		

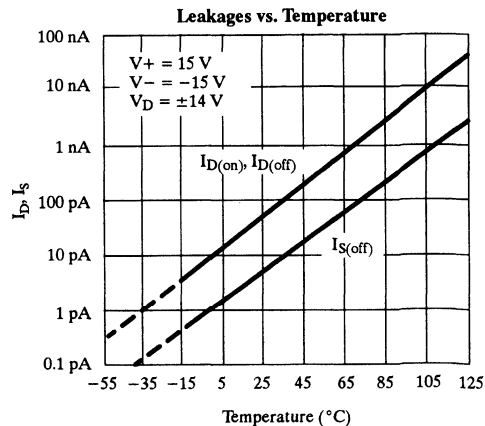
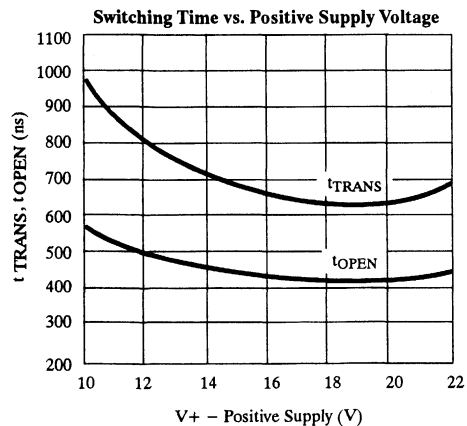
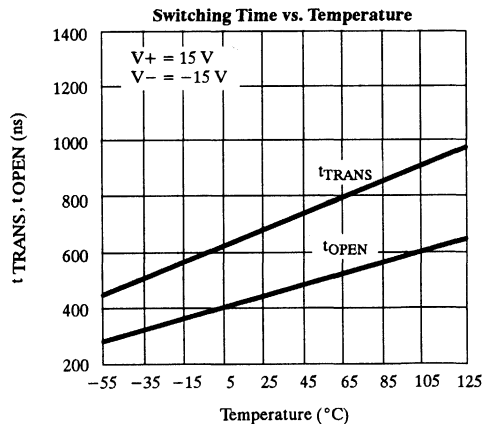
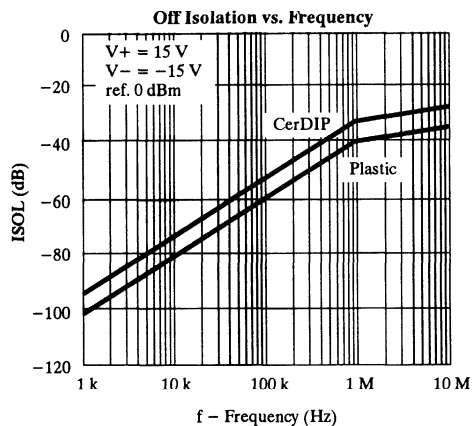
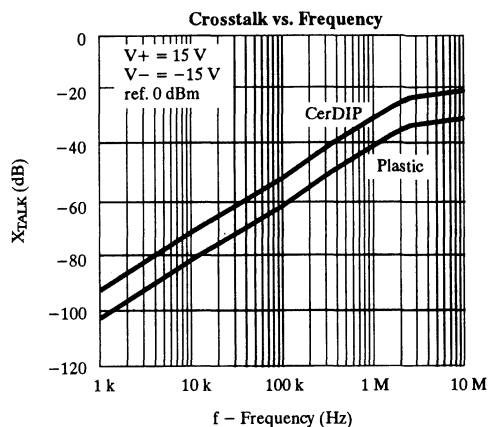
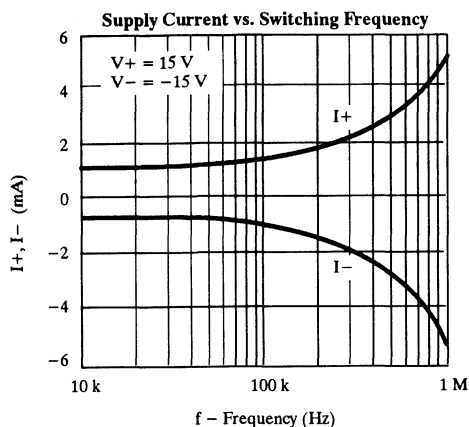
**Notes:**

- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

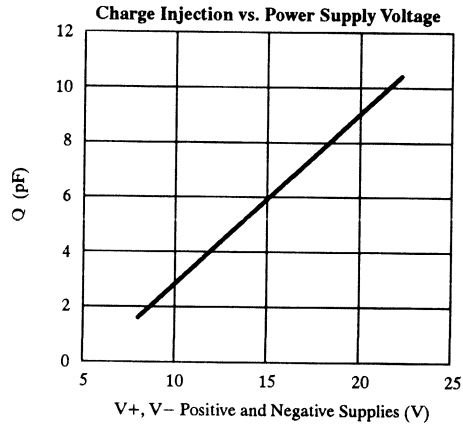
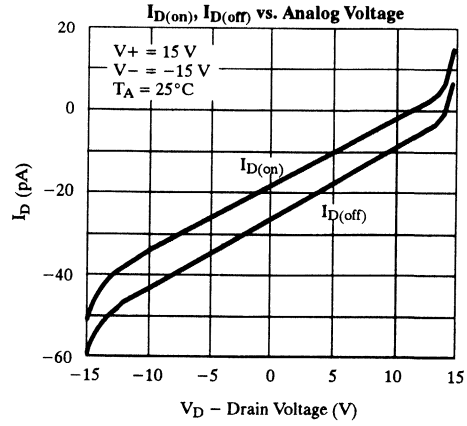
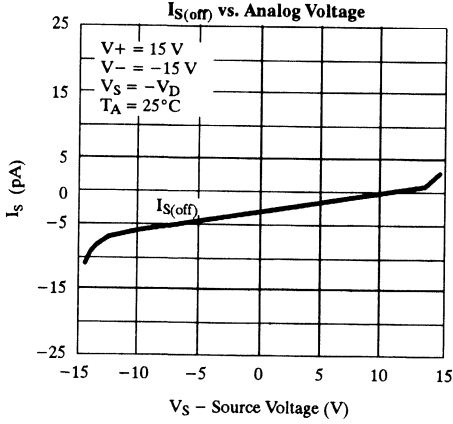
**Typical Characteristics**



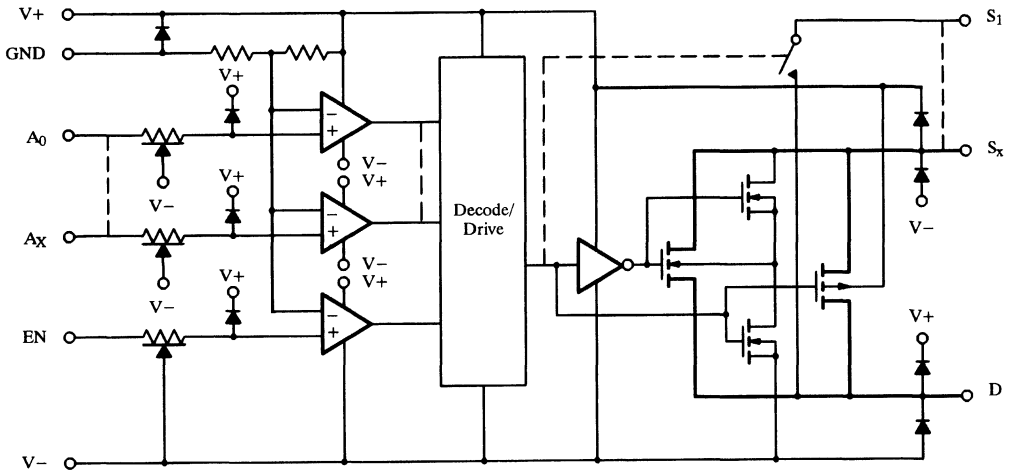
## Typical Characteristics (Cont'd)



**Typical Characteristics (Cont'd)**



## Schematic Diagram (Typical Channel)



## Test Circuits

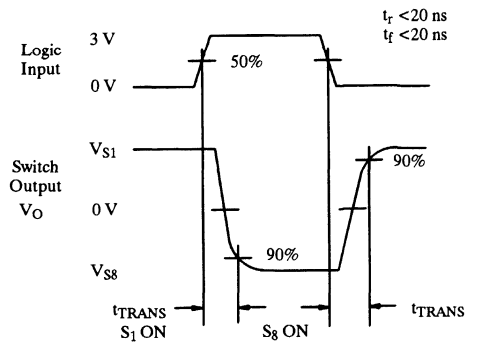
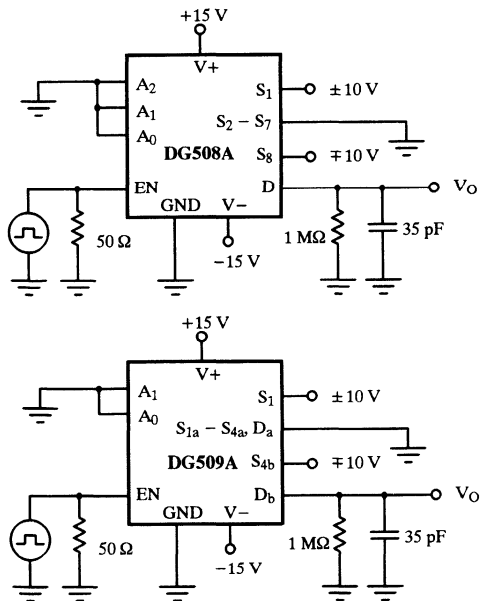
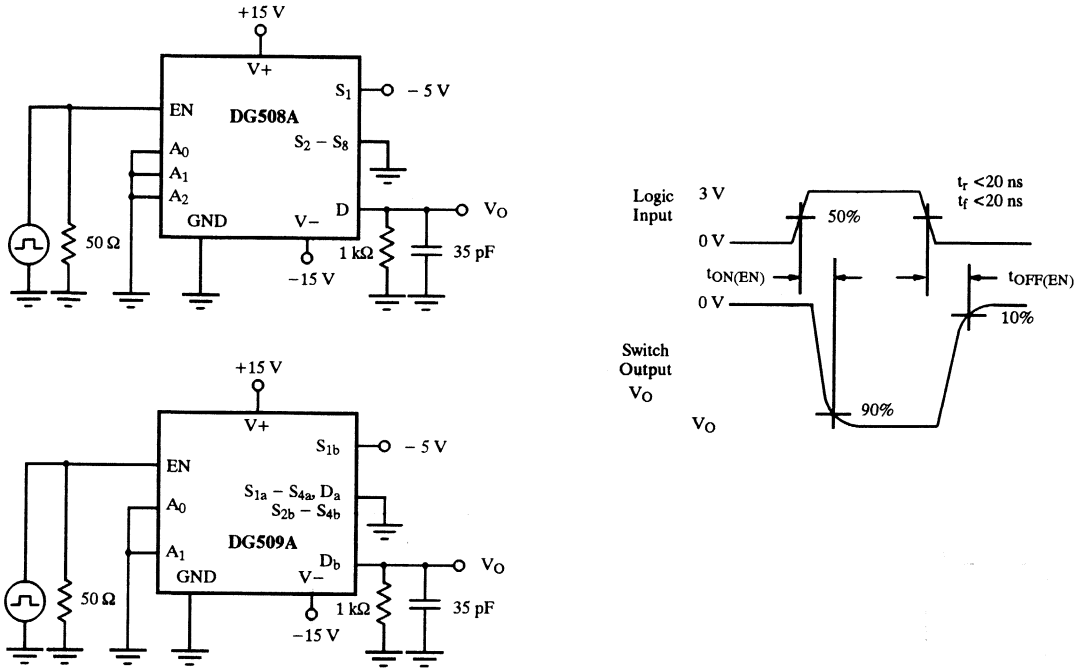


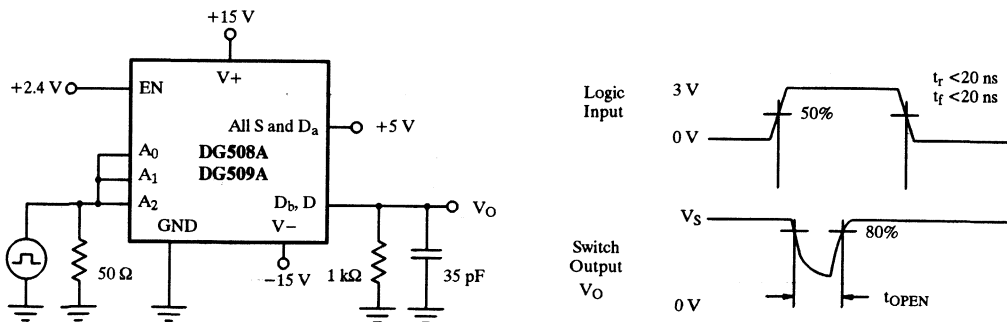
Figure 2. Transition Time



**Test Circuits (Cont'd)**

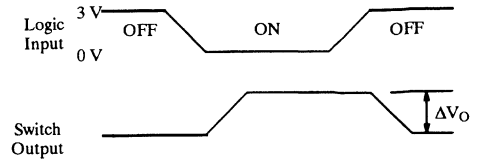
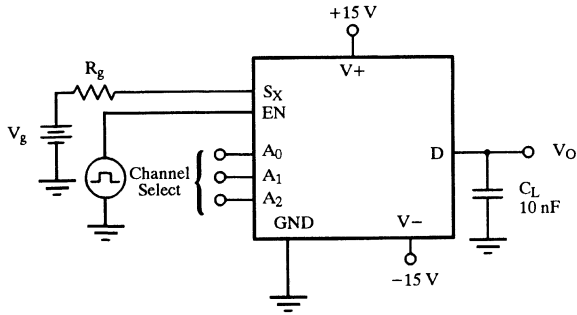


**Figure 3. Enable Switching Time**



**Figure 4. Break-Before-Make Interval**

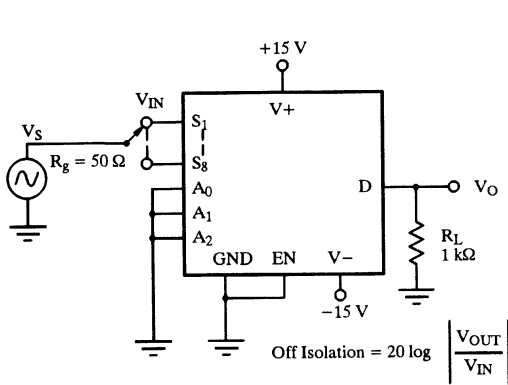
## Test Circuits (Cont'd)



$\Delta V_O$  is the measured voltage due to charge transfer error  $Q$ , when the channel turns off.

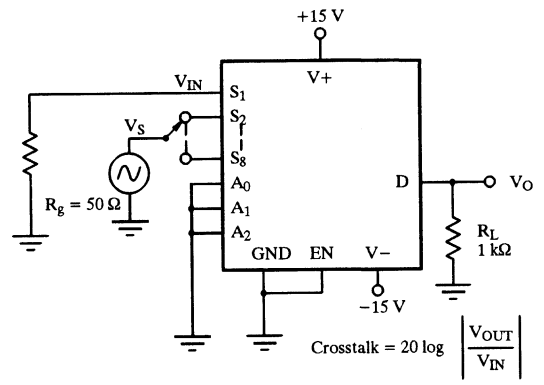
$$Q = C_L \times \Delta V_O$$

**Figure 5.** Charge Injection



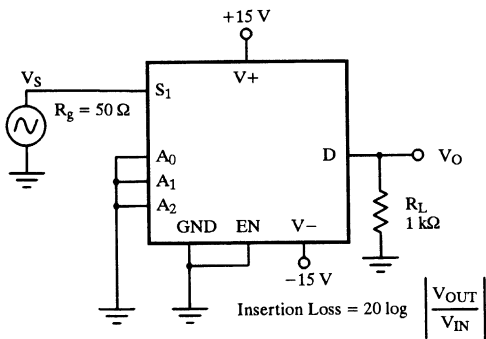
$$\text{Off Isolation} = 20 \log \left| \frac{V_{OUT}}{V_{IN}} \right|$$

**Figure 6.** Off Isolation



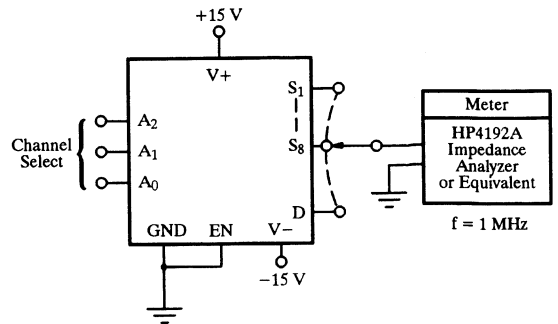
$$\text{Crosstalk} = 20 \log \left| \frac{V_{OUT}}{V_{IN}} \right|$$

**Figure 7.** Crosstalk



$$\text{Insertion Loss} = 20 \log \left| \frac{V_{OUT}}{V_{IN}} \right|$$

**Figure 8.** Insertion Loss



Meter  
HP4192A  
Impedance  
Analyzer  
or Equivalent

$f = 1 \text{ MHz}$

**Figure 9.** Source Drain Capacitance

**Applications**

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15	-15	2.4/0.8	-15 to 15
10	-12	2.4/0.8	-12 to 12
12	-10	2.4/0.6	-10 to 10
8 <sup>b</sup>	-8	2.4/0.4	-8 to 8

Notes:

- a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- b. Operation below ±8 V is not recommended.

**Overvoltage Protection**

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 11). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V<sub>S</sub> and the V- rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

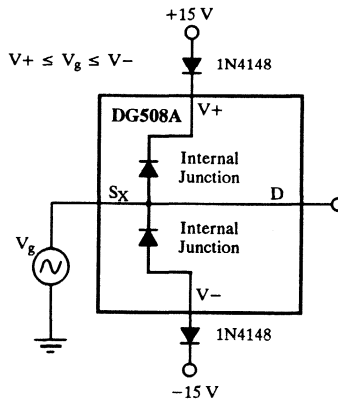


Figure 10. Overvoltage Protection Using Blocking Diodes

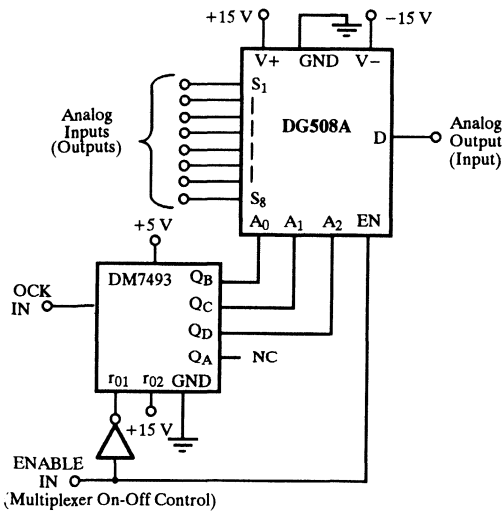


Figure 11. 8-Channel Sequential Multiplexer/  
Demultiplexer

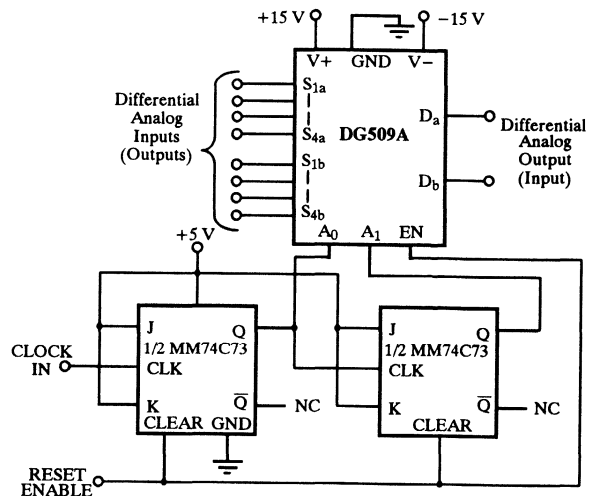


Figure 12. Differential 4-Channel Sequential Multiplexer/  
Demultiplexer

## Latchable Single 8-Channel/Differential 4-Channel Analog Multiplexers

### Features

- Low  $I_{DS(on)}$ : 270  $\Omega$
- 44-V Power Supply Rating
- On-Board Address Latches
- Break-Before-Make
- Low Leakage— $I_{D(on)}$ : 30 pA

### Benefits

- Improved System Accuracy
- Microprocessor Bus Compatible
- Easily Interfaced
- Reduced Crosstalk

### Applications

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Medical Instrumentation

### Description

The DG528 is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address ( $A_0, A_1, A_2$ ). DG529, a 4-channel dual analog multiplexer, is designed to connect one of four differential inputs to a common differential output as determined by its 2-bit binary address ( $A_0, A_1$ ) logic.

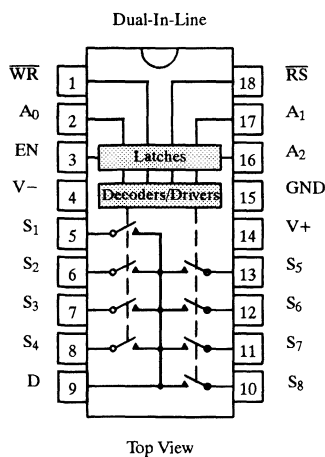
applications. Break-before-make switching action protects against momentary shorting of the input signals. The DG528/529 are built on the improved PLUS-40 CMOS process. A buried layer prevents latchup.

These analog multiplexers have on-chip address and control latches to simplify design in microprocessor based

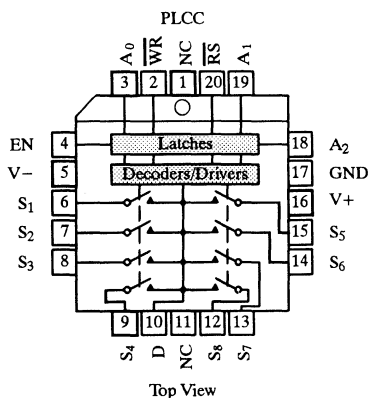
The on chip TTL-compatible address latches simplify digital interface design and reduce board space in data acquisition systems, process controls, avionics, and ATE.

### Functional Block Diagrams and Pin Configurations

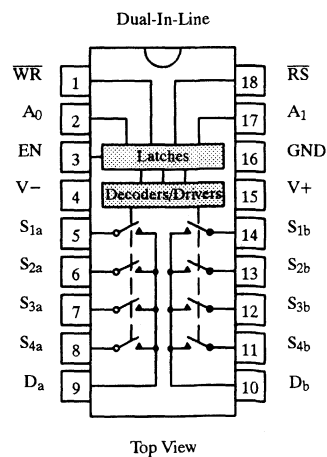
**DG528**



**DG528**




**DG529**




**Truth Tables**

**Truth Table — DG528**  
8-Channel Single-Ended Multiplexer

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
<b>Latching</b>						
X	X	X	X		1	Maintains previous switch condition
<b>Reset</b>						
X	X	X	X	X	0	None (latches cleared)
<b>Transparent Operation</b>						
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

**Truth Table — DG529**  
Differential 4-Channel Multiplexer

A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
<b>Latching</b>					
X	X	X		1	Maintains previous switch condition
<b>Reset</b>					
X	X	X	X	0	None (latches cleared)
<b>Transparent Operation</b>					
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "0" = V<sub>AL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>AH</sub> ≥ 2.4 V  
 X = Don't Care

**Ordering Information — DG528**

Temp Range	Package	Part Number
0 to 70°C	18-Pin Plastic DIP	DG528CJ
	20-Pin PLCC	DG528DN
-25 to 85°C	18-Pin CerDIP	DG528BK
		DG528AK
DG528AK/883		
5962-8768901VA		
-55 to 125°C		

**Ordering Information — DG529**

Temp Range	Package	Part Number
0 to 70°C	18-Pin Plastic DIP	DG529CJ
-25 to 85°C	18-Pin CerDIP	DG529BK
		DG529AK/883
-55 to 125°C		

**Absolute Maximum Ratings**

Voltage Referenced to V-

V+	44 V
GND	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Current (Any Terminal Except S or D)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Storage Temperature (AK, BK Suffix)	-65 to 150°C
(CJ, DN Suffix)	-65 to 125°C

Power Dissipation (Package)<sup>b</sup>

18-Pin Plastic DIP <sup>c</sup>	470 mW
18-Pin CerDIP <sup>d</sup>	900 mW
20-Pin PLCC <sup>e</sup>	800 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub> or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 6.3 mW/°C above 75°C.
- Derate 1.2 mW/°C above 75°C.
- Derate 10 mW/°C above 75°C.

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, \overline{WR} = 0$ $\overline{RS} = 2.4\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ }\mu\text{F}^d$		Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C, D Suffix -40 to 85°C		Unit
						Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full			-15	15	-15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}, I_S = -200\text{ }\mu\text{A}$	Room Full	270			400 500		450 550	$\Omega$
Greatest Change in $r_{DS(on)}$ Between Channels <sup>f</sup>	$\Delta r_{DS(on)}$	$-10\text{ V} < V_S < 10\text{ V}$	Room	6						%
Source Off Leakage Current	$I_{S(off)}$	$V_{EN} = 0\text{ V}, V_S = \pm 10\text{ V}$ $V_D = \mp 10\text{ V}$	Room Full	$\pm 0.005$	-1 -50	1 50	-5 -50	5 50		
Drain Off Leakage Current	$I_{D(off)}$	$V_{EN} = 0\text{ V}$ $V_D = \pm 10\text{ V}$ $V_S = \mp 10\text{ V}$	DG528	Room Full	$\pm 0.015$	-10 -200	10 200	-20 -200	20 200	nA
			DG529	Room Full	$\pm 0.008$	-10 -100	10 100	-20 -100	20 100	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 10\text{ V}$ $V_{EN} = 2.4\text{ V}$	DG528	Room Full	$\pm 0.03$	-10 -200	10 200	-20 -200	20 200	
			DG529	Room Full	$\pm 0.015$	-10 -100	10 100	-20 -100	20 100	
<b>Digital Control</b>										
Logic Input Current	$I_{AH}$	$V_A = 2.4\text{ V}$	Room Hot	-0.002	-10 -30		-10 -30			$\mu\text{A}$
Input Voltage High		$V_A = 15\text{ V}$	Room Hot	0.006		10 30		10 30		
Logic Input Current Input Voltage Low	$I_{AL}$	$V_{EN} = 0\text{ V}, 2.4\text{ V}, V_A = 0\text{ V}$ $\overline{RS} = 0\text{ V}, \overline{WR} = 0\text{ V}$	Room Hot	-0.002	-10 -30		-10 -30			
<b>Dynamic Characteristics</b>										
Transition Time	$t_{TRANS}$	See Figure 5	Room	0.6		1				$\mu\text{s}$
Break-Before-Make Interval	$t_{OPEN}$	See Figure 4	Room	0.2						
EN and $\overline{WR}$ Turn-On Time	$t_{ON(EN, WR)}$	See Figures 6 and 7	Room	1		1.5				
EN and $\overline{WR}$ Turn-Off Time	$t_{OFF(EN, WR)}$	See Figures 6 and 8	Room	0.4		1				
Charge Injection	Q	$V_S = 0\text{ V}, R_y = 0\text{ }\Omega, C_L = 10\text{ }\mu\text{F}$	Room	4						pC
Off Isolation	OIRR	$V_{EN} = 0\text{ V}, R_L = 1\text{ k}\Omega, C_L = 15\text{ pF}$ $V_S = 7\text{ V}_{RMS}, f = 500\text{ kHz}$	Room	68						dB
Logic Input Capacitance	$C_{in}$	$f = 1\text{ MHz}$	Room	2.5						pF
Source Off Capacitance	$C_{S(off)}$	$V_{EN} = 0\text{ V}, V_S = 0\text{ V}, f = 140\text{ kHz}$	Room	5						
Drain Off Capacitance	$C_{D(off)}$	$V_{EN} = 0\text{ V}, V_D = 0\text{ V}$ $f = 140\text{ kHz}$	DG528	Room	25					
			DG529	Room	12					
<b>Minimum Input Timing Requirements</b>										
Write Pulse Width	$t_w$		Full		300		300			ns
$A_X$ , EN Setup Time	$t_s$		Full		180		180			
$A_X$ , EN Hold Time	$t_H$		Full		30		30			
Reset Pulse Width	$t_{RS}$	$V_S = 5\text{ V}$ , See Figure 3	Full		500		500			

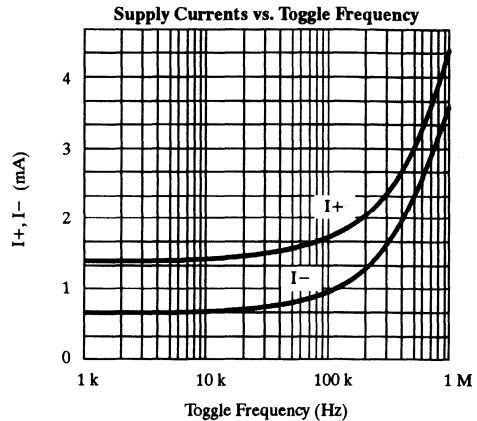
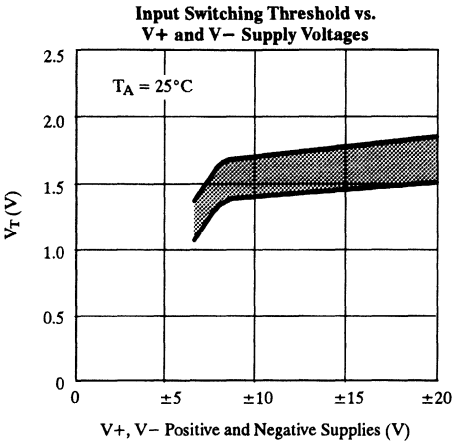
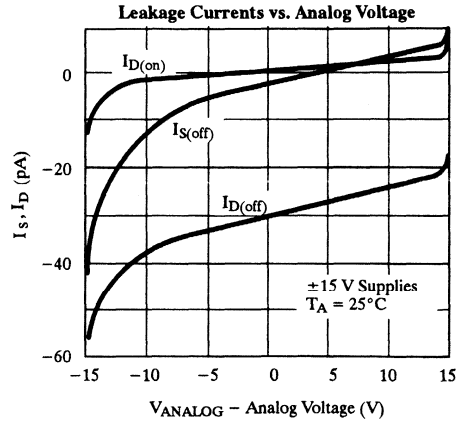
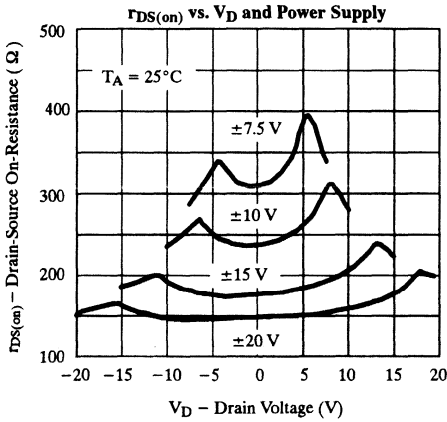
**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}, WR = 0$ $RS = 2.4\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ }\mu\text{F}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C, D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	$V_{EN} = 0\text{ V}, V_A = 0$	Room			2.5		2.5	mA
Negative Supply Current	I-		Room		-1.5		-1.5		

**Notes:**

- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

**Typical Characteristics**



## Schematic Diagram

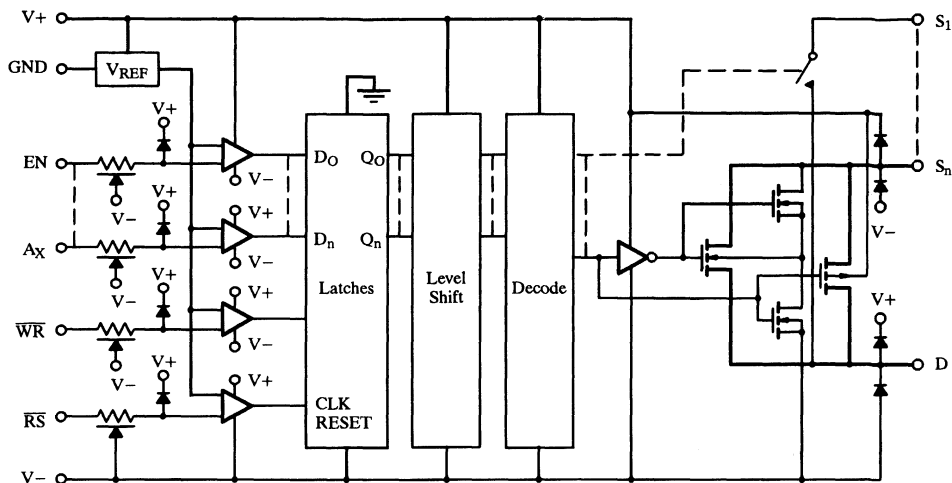


Figure 1.

## Detailed Description

The internal structure of the DG528/DG529 includes a 5-V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel n- and p-channel MOSFETs (see Figure 1).

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D type latch. The level sensitive D latch continuously places the  $D_X$  input signal on the  $Q_X$  output when the  $\overline{WR}$  input is low, resulting in transparent latch operation. As soon as  $\overline{WR}$  returns high, the latches hold the data last present on the  $D_X$  input, subject to the minimum input timing requirements.

Following the latches the  $Q_X$  signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full on/off switch operation for any analog signal present between the  $V+$  and  $V-$  supply rails.

The EN pin is used to enable the address latches during the  $\overline{WR}$  pulse. It can be hard-wired to the logic supply or to  $V+$  if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The  $\overline{RS}$  pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The  $\overline{WR}$  pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

## Timing Diagrams

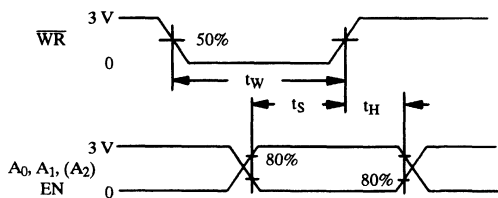


Figure 2.

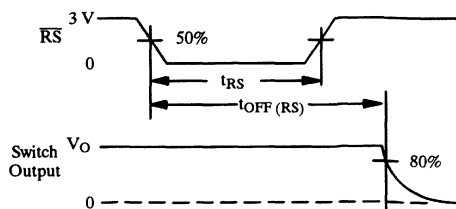
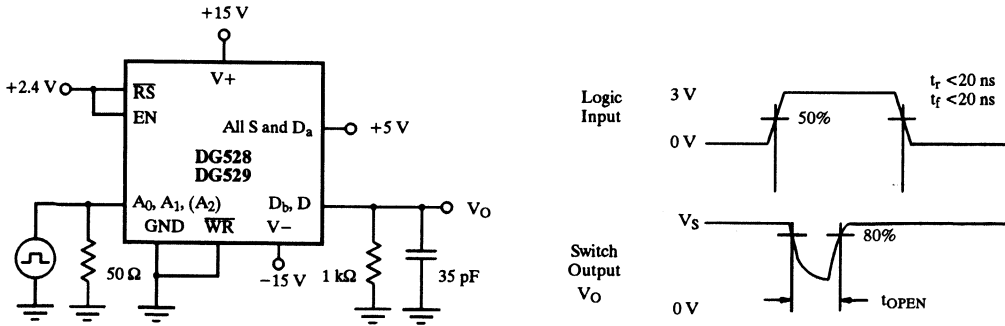


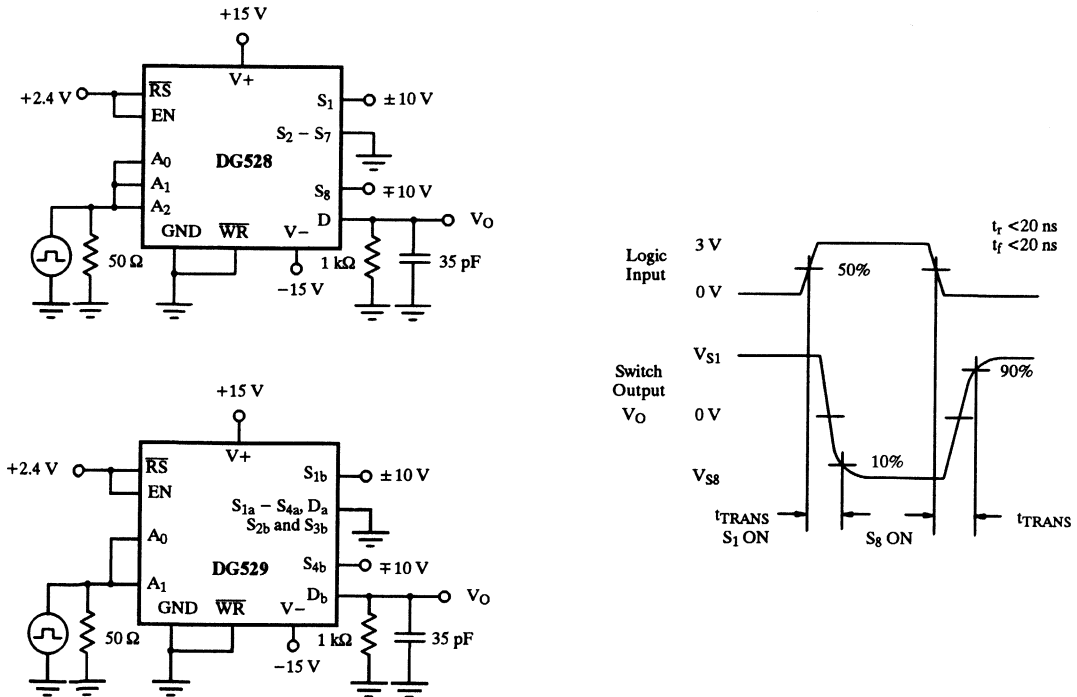
Figure 3.



**Test Circuits**



**Figure 4. Break-Before-Make**



**Figure 5. Transition Time**

## Test Circuits (Cont'd)

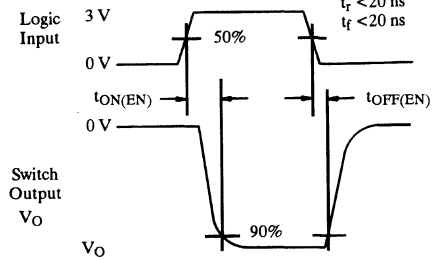
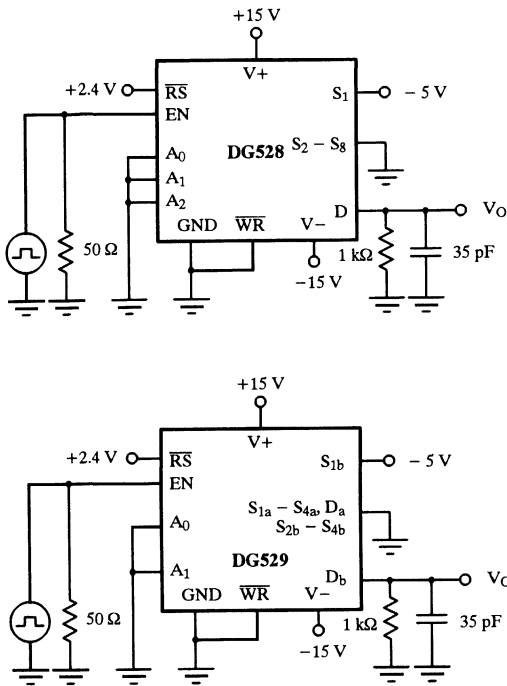


Figure 6. Enable  $t_{ON}/t_{OFF}$  Time

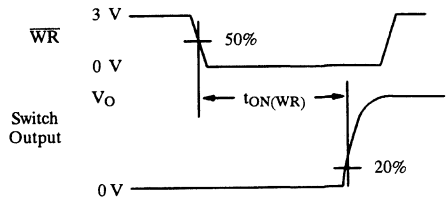
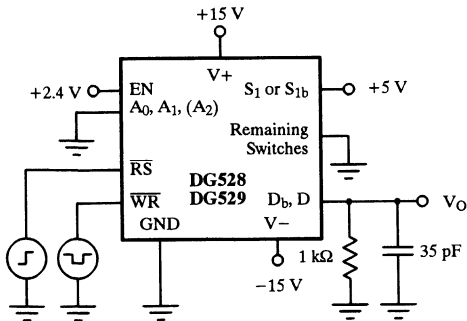
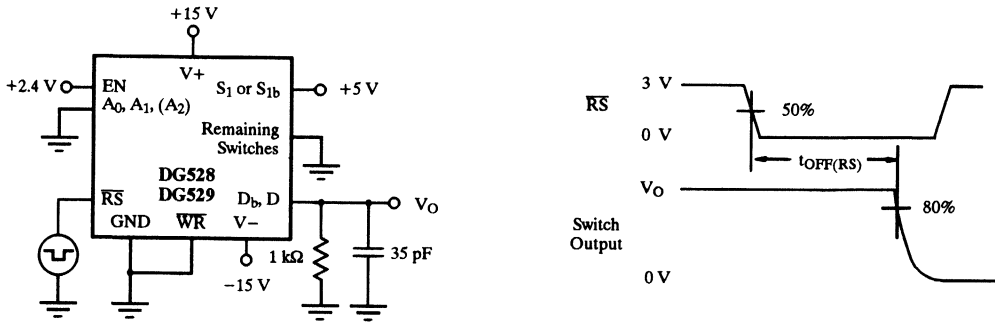
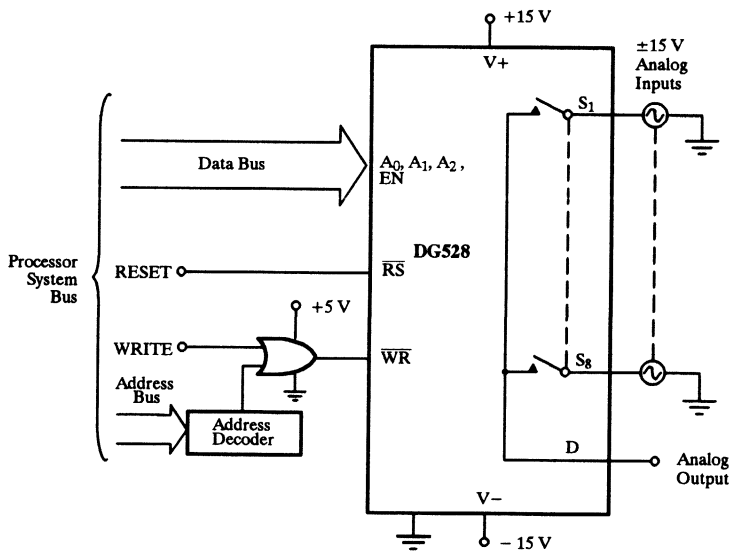


Figure 7. Write Turn-On Time  $t_{ON}(\overline{WR})$

**Test Circuits (Cont'd)**



**Figure 8.** Reset Turn-Off Time  $t_{OFF}(RS)$



**Figure 9.** Bus Interface

**Applications**

**Bus Interfacing**

The DG528/DG529 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only

memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 on) until the microprocessor determines it is necessary to turn different switches on or turn all switches off (see Figure 9).

## Applications (Cont'd)

The input latches become transparent when  $\overline{WR}$  is held low; therefore, these multiplexers operate by direct command of the coded switch state on  $A_2, A_1, A_0$ . In this mode the DG528 is identical to the popular DG508A. The same is true of the DG529 versus the popular DG509A.

During system power-up,  $\overline{RS}$  would be low, maintaining all eight switches in the off state. After  $\overline{RS}$  returned high the DG528 maintains all switches in the off state. When the system program performs a write operation to the address assigned to the DG528, the address decoder provides a  $\overline{CS}$  active low signal which is gated with the  $\overline{WR}$

control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the  $\overline{WR}$  signal returns to the high state, (positive edge) the input latches of the DG528 save the data from the DATA BUS. The coded information in the  $A_0, A_1, A_2$  and EN latches is decoded and the appropriate switch is turned on.

The EN latch allows all switches to be turned off under program control. This becomes useful when two or more DG528s are cascaded to build 16-line and larger multiplexers.

## Application Hints<sup>a</sup>

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
20	-20	2.4/0.8	±20
15 <sup>b</sup>	-15	2.4/0.8	±15
8 <sup>c</sup>	-8 (min)	2.4/0.8	±8

**Notes:**

- a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- b. Electrical Parameter Chart based on V+ = 15 V, V<sub>L</sub> = 5 V, V<sub>R</sub> = GND.
- c. Operation below ±8 V is not recommended.

## 4-/8-Channel Wideband Video Multiplexers

### Features

- Wide Bandwidth: 500 MHz
- Very Low Crosstalk:  $-97$  dB @ 5 MHz
- On-Board TTL-Compatible Latches with Readback
- Optional Negative Supply
- Low  $r_{DS(on)}$ :  $45 \Omega$

### Benefits

- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- Allows Differential Signal Switching

### Applications

- Wideband Signal Routing and Multiplexing
- Video Switchers
- ATE Systems
- Infrared Imaging

### Description

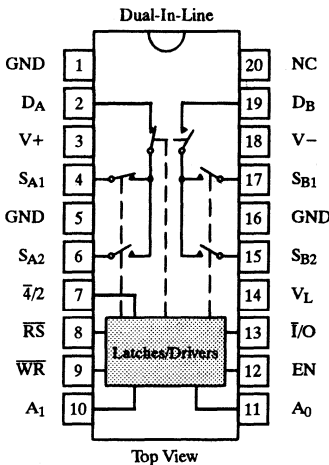
The DG534 is a digitally selectable 4-channel or dual 2-channel multiplexer. The DG538 is an 8-channel or dual 4-channel multiplexer. On-chip TTL-compatible address decoding logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low on-resistance and low capacitance of these devices make them ideal for wideband data multiplexing and video and audio signal routing in channel selectors and crosspoint arrays. An optional negative supply pin allows the handling of bipolar signals without dc biasing.

The DG534/DG538 are built on a D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are in a "T" configuration to achieve extremely high levels of off isolation. Crosstalk is reduced to  $-97$  dB at 5 MHz by including a ground line between each adjacent signal path.

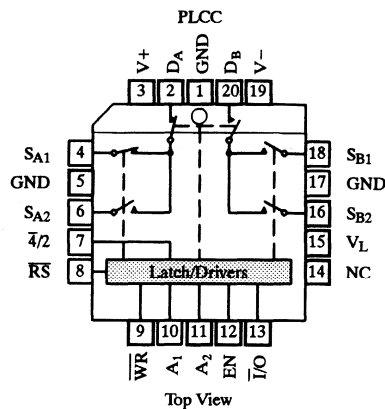
The DG534A/DG538A are recommended for new designs.

### Functional Block Diagrams and Pin Configurations

DG534DJ

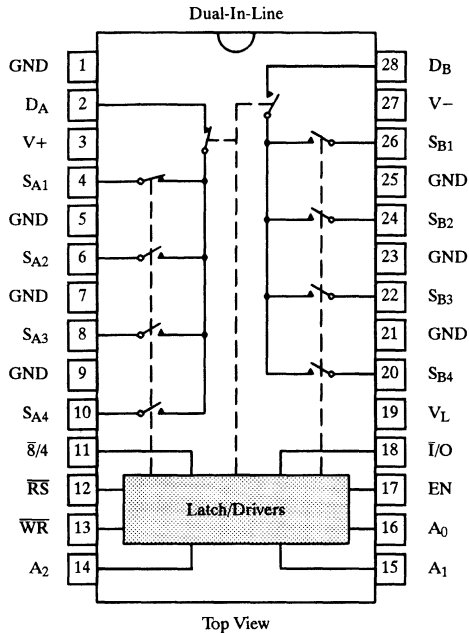


DG534DN

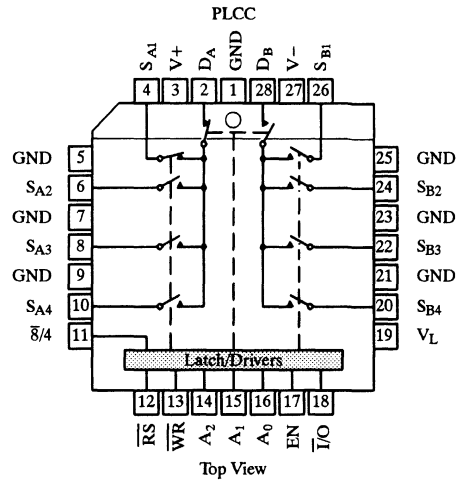


## Functional Block Diagrams and Pin Configurations (Cont'd)

**DG538DJ**



**DG538DN**



## Truth Tables and Ordering Information

Ordering Information – DG534

Temp Range	Package	Part Number
-40 to 85°C	20-Pin Plastic DIP	DG534DJ
	20-Pin PLCC	DG534DN
-55 to 125°C	20-Pin Sidebrazed	DG534AP
		DG534AP/883

Truth Table — DG534

I/O	A <sub>1</sub>	A <sub>0</sub>	EN	WR	RS	4/2 <sup>a</sup>	On Switch	
X	X	X	X	1	1	1	Maintains previous state	
X	X	X	X	X	0	X	None (latches cleared)	
X	X	X	0	0	1	X	None	
0	0	0	1	0	1	0	D <sub>A</sub> and D <sub>B</sub> may be connected externally	
0	0	1	1	0	1	0		S <sub>A1</sub>
0	1	0	1	0	1	0		S <sub>A2</sub>
0	1	0	1	0	1	0		S <sub>B1</sub>
0	1	1	1	0	1	0		S <sub>B2</sub>
0	X	0	1	0	1	1		S <sub>A1</sub> and S <sub>B1</sub>
0	X	1	1	0	1	1	S <sub>A2</sub> and S <sub>B2</sub>	
1	Note b		1	1	Note c		Latches Transparent	

Logic "0" = V<sub>AL</sub> ≤ 0.8 V

Logic "1" = V<sub>AH</sub> ≥ 2 V

X = Don't Care

Notes:

- Connect D<sub>A</sub> and D<sub>B</sub> together externally for single-ended operation.
- With I/O high, A<sub>n</sub> pin becomes output and reflects latch contents. See timing diagrams for more detail.
- 4/2 can be either "1" or "0" but should not change during these operations.

**Truth Tables and Ordering Information (Cont'd)**

Ordering Information – DG538

Temp Range	Package	Part Number
-40 to 85°C	28-Pin Plastic DIP	DG538DJ
	28-Pin PLCC	DG538DN
-55 to 125°C	28-Pin Sidebrazed	DG538AP
		DG538AP/883

Truth Table — DG538

I/O	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	$\overline{8/4}^a$	On Switch		
X	X	X	X	X	1	1	1	Maintains previous state		
X	X	X	X	X	X	0	X	None (latches cleared)		
X	X	X	X	0	0	1	X	None		
0	0	0	0	1	0	1	0	S <sub>A1</sub>	D <sub>A</sub> and D <sub>B</sub> should be connected externally	Latches Transparent
0	0	0	1	1	0	1	0	S <sub>A2</sub>		
0	0	1	0	1	0	1	0	S <sub>A3</sub>		
0	0	1	1	1	0	1	0	S <sub>A4</sub>		
0	1	0	0	1	0	1	0	S <sub>B1</sub>		
0	1	0	1	1	0	1	0	S <sub>B2</sub>		
0	1	1	0	1	0	1	0	S <sub>B3</sub>		
0	1	1	1	1	0	1	0	S <sub>B4</sub>		
0	X	0	0	1	0	1	1	S <sub>A1</sub> and S <sub>B1</sub>		
0	X	0	1	1	0	1	1	S <sub>A2</sub> and S <sub>B2</sub>		
0	X	1	0	1	0	1	1	S <sub>A3</sub> and S <sub>B3</sub>		
0	X	1	1	1	0	1	1	S <sub>A4</sub> and S <sub>B4</sub>		
1	Note b				1	1	Note c			

Logic "0" = V<sub>AL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>AH</sub> ≥ 2 V  
 X = Don't Care

Notes:

- Connect D<sub>A</sub> and D<sub>B</sub> together externally for single-ended operation.
- With I/O high, A<sub>n</sub> pin becomes output and reflects latch contents. See timing diagrams for more detail.
- $\overline{8/4}$  can be either "1" or "0" but should not change during these operations.

**Absolute Maximum Ratings**

V <sub>+</sub> to GND	-0.3 V to +21 V
V <sub>+</sub> to V <sub>-</sub>	-0.3 V to +21 V
V <sub>-</sub> to GND	-10 V to +0.3 V
V <sub>L</sub>	0 V to (V <sub>+</sub> ) + 0.3 V
Digital Inputs	(V <sub>-</sub> ) -0.3 V to (V <sub>+</sub> ) + 0.3 V or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub>	(V <sub>-</sub> ) -0.3 V to (V <sub>-</sub> ) + 14 V or 20 mA, whichever occurs first
Current (any terminal) Continuous	20 mA
Current(S or D) Pulsed 1 ms 10% Duty	40 mA

Storage Temperature	(A Suffix) -65 to 150°C
	(D Suffix) -65 to 125°C

Power Dissipation (Package) <sup>a</sup>	
Plastic DIP <sup>b</sup>	625 mW
PLCC <sup>c</sup>	450 mW
Sidebrazed <sup>d</sup>	1200 mW

Notes:

- All leads soldered or welded to PC board.
- Derate 8.3 mW/°C above 75°C.
- Derate 6 mW/°C above 75°C.
- Derate 16 mW/°C above 75°C.

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}, V_L = 5\text{ V}$ $WR = 0.8\text{ V}, RS, EN = 2\text{ V}$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>g</sup>	$V_{ANALOG}$	$V_- = -5\text{ V}$	Full		-5	8	-5	8	V	
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_S = 0\text{ V}$ $V_{AIL} = 0.8\text{ V}, V_{AIH} = 2\text{ V}$ Sequence Each Switch On	Room	45		90		90	$\Omega$	
Resistance Match Between Channels	$\Delta r_{DS(on)}$		Room			9		9		
Source Off Leakage Current	$I_{S(off)}$	$V_S = 8\text{ V}, V_D = 0\text{ V}, EN = 0.8\text{ V}$	Room Full	0.05	-5 -50	5 50	-5 -50	5 50	nA	
Drain Off Leakage Current	$I_{D(off)}$	$V_S = 0\text{ V}, V_D = 8\text{ V}, EN = 0.8\text{ V}$	Room Full	0.1	-20 -500	20 500	-20 -100	20 100		
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = 8\text{ V}$	Room Full	0.1	-20 -1000	20 1000	-20 -200	20 200		
<b>Digital Control</b>										
Input Voltage High	$V_{AIH}$		Full		2		2		V	
Input Voltage Low	$V_{AIL}$		Full			0.8		0.8		
Address Input Current	$I_{AI}$	$V_{AI} = 0\text{ V}, \text{ or } 2\text{ V} \text{ or } 5\text{ V}$	Room Full	-0.1	-1 -10	1 10	-1 -10	1 10	$\mu\text{A}$	
Address Output Current	$I_{AO}$	$V_{AO} = 2.7\text{ V}$	Room	-300						
		$V_{AO} = 0.4\text{ V}$	Room	300						
<b>Dynamic Characteristics</b>										
On State Input Capacitance <sup>g</sup>	$C_{S(on)}$		PLCC	Room	28		40		40	pF
			DIP	Room	31		45		45	
Off State Input Capacitance <sup>g</sup>	$C_{S(off)}$		PLCC	Room	3		5		4	
			DIP	Room	4				5	
Off State Output Capacitance <sup>g</sup>	$C_{D(off)}$		PLCC	Room	6		10		8	
			DIP	Room	8				10	
Transition Time	$t_{TRANS}$		Room Full	170		300 500		300 500	ns	
Break-Before-Make Interval	$t_{OPEN}$		Room Full	80	50 25		50 25			
EN, WR Turn On Time	$t_{ON}$		Room Full	180		300 500		300 500		
EN, Turn Off Time	$t_{OFF}$		Room Full	95		175 300		175 300		
Charge Injection	$Q_i$		Room	-70					pC	
Chip Disabled Crosstalk <sup>f</sup>	$X_{TALK(CD)}$	$R_L = 75\ \Omega, f = 5\text{ MHz}$ $EN = 0.8\text{ V}$	PLCC	Room	-75					dB
			DIP	Room	-65					
Adjacent Input Crosstalk <sup>f</sup>	$X_{TALK(AI)}$	$R_{IN} = 10\ \Omega, R_L = 10\text{ k}\Omega$ $f = 5\text{ MHz}$	PLCC	Room	-97					
			DIP	Room	-87					
		$R_{IN} = 75\ \Omega, R_L = 75\ \Omega$ $f = 5\text{ MHz}$	PLCC	Room	-80					
			DIP	Room	-70					



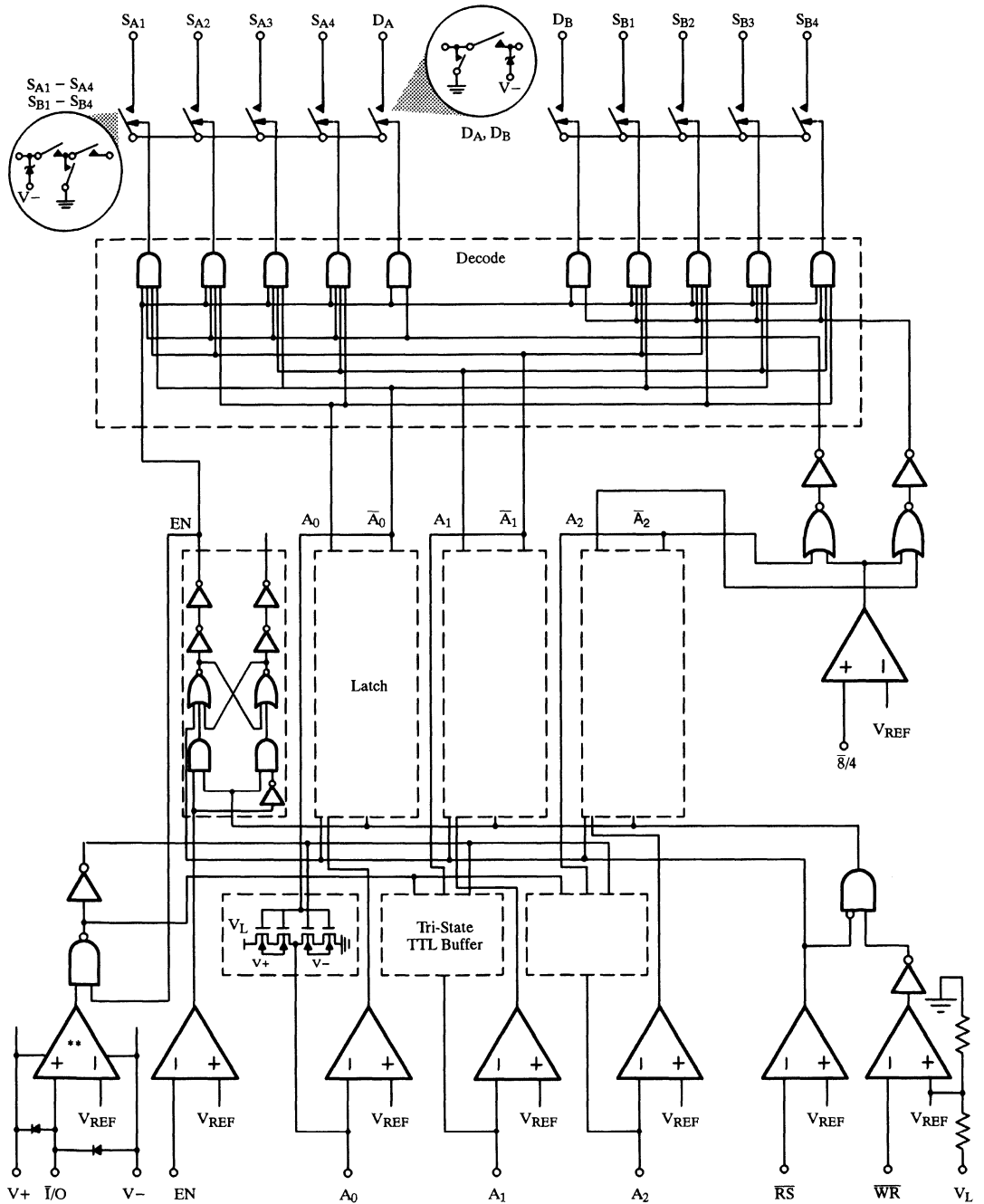
**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}, V_L = 5\text{ V}$ $\overline{WR} = 0.8\text{ V}, \overline{RS}, \overline{EN} = 2\text{ V}$		Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
						Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Dynamic Characteristics (Cont'd)</b>										
All Hostile Crosstalk	$X_{TALK(AH)}$	$R_{IN} = 10\ \Omega, R_L = 10\ \text{k}\Omega$ $f = 5\ \text{MHz}$	PLCC	Room	-77					dB
			DIP	Room	-72					
		$R_{IN} = 75\ \Omega, R_L = 75\ \Omega$ $f = 5\ \text{MHz}$	PLCC	Room	-77					
			DIP	Room	-72					
Differential Crosstalk	$X_{TALK(DIFF)}$	$R_{IN} = 10\ \Omega, R_L = 10\ \text{k}\Omega$ $f = 5\ \text{MHz}$		Room	-84					
		$R_{IN} = R_L = 75\ \Omega$ $f = 5\ \text{MHz}$		Room	-84					
Bandwidth	BW	$R_L = 50\ \Omega$		Room	500					MHz
<b>Power Supplies</b>										
Positive Supply Current	I+	Any One Channel Selected with Address Inputs at GND or V+		Room Full	0.6		2 5		2 5	mA
Negative Supply Current	I-			Room Full	0.6	-1.8 -2		-1.8 -2		
Functional Check of Maximum Operating Supply Voltage Range	V+ to V-	Functional Test Only		Full		10	21	10	21	V
	V- to GND			Full		-5.5	0	-5.5	0	
	V+ to GND			Full		10	21	10	21	
Logic Supply Current	$I_L$			Full	150		500		500	$\mu\text{A}$
<b>Timing</b>										
Reset to Write	$t_{RW}$	See Figure 1		Full		50		50		ns
$\overline{WR}, \overline{RS}$ Minimum Pulse Width	$t_{MPW}$			Full		200		200		
$A_0, A_1, \overline{EN}$ Data Valid to Strobe	$t_{DW}$			Full		100		100		
$A_0, A_1, \overline{EN}$ Data Valid after Strobe	$t_{WD}$			Full		50		50		
Address Bus Tri-State <sup>e</sup>	$t_{AZ}$			Room	25					
Address Bus Output	$t_{AO}$			Room	95					
Address Bus Input	$t_{AI}$			Room	110					

**Notes:**

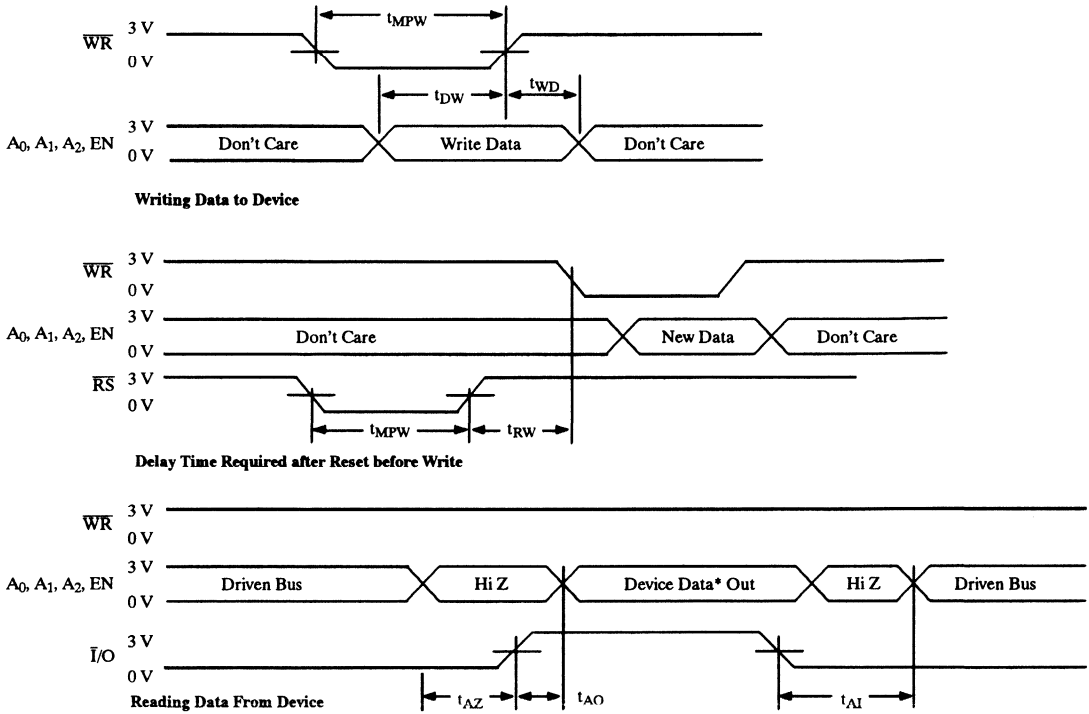
- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Defined by system bus requirements.
- f. Each individual pin shown as GND must be grounded.
- g. Guaranteed by design, not subject to production test.

## Control Circuitry



\* Decode section includes delay circuitry in AND gating to ensure proper break-before-make operation.  
 \*\* Typical all digital inputs.

**Output Timing Requirements**



\* Enable must be latched high to read data, otherwise BUS is high Z.  $V_- \leq -3$  V required for readback functionality.

Figure 1.

**Applications**

To protect against latchup  $V_L$  must not exceed  $V+$  by more than 0.3 V. This is easily achieved by generating  $V_L$  from  $V+$  using a Zener or a resistor divider network as shown in Figure 2. When an external  $V_L$  is available the alternative

simple protection circuit shown in Figure 3 should be used to prevent triggering the parasitic SCR during power up. The DG53XA does not require these protection diodes.

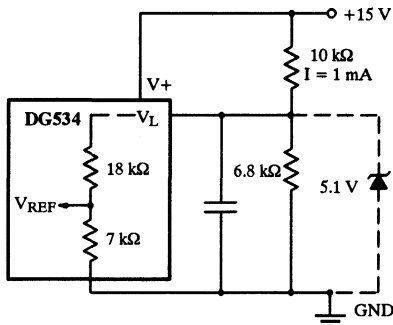


Figure 2.  $V_L$  Generated from  $V+$

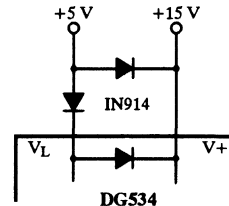


Figure 3. External Diodes Prevent Latchup

## 4-/8-Channel Wideband Video Multiplexers

### Features

- Wide Bandwidth: 500 MHz
- Very Low Crosstalk:  $-97$  dB @ 5 MHz
- On-Board TTL-Compatible Latches with Readback
- Optional Negative Supply
- Low  $r_{DS(on)}$ : 45  $\Omega$
- Single-Ended or Differential Operation
- Latch-up Proof

### Benefits

- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- High-Speed Readback
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- Allows Differential Signal Switching

### Applications

- Wideband Signal Routing and Multiplexing
- Video Switchers
- ATE Systems
- Infrared Imaging
- Ultrasound Imaging

### Description

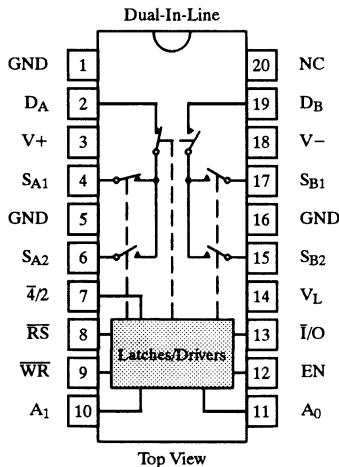
The DG534A is a digitally selectable 4-channel or dual 2-channel multiplexer. The DG538A is an 8-channel or dual 4-channel multiplexer. On-chip TTL-compatible address decoding logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low on-resistance and low capacitance of these devices make them ideal for wideband data multiplexing and video and audio signal routing in channel selectors and crosspoint arrays. An optional negative supply pin allows the handling of bipolar signals without dc biasing.

The DG534A/DG538A are built on a D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are connected in a "T" configuration to achieve extremely high levels of off isolation. Crosstalk is reduced to  $-97$  dB at 5 MHz by including a ground line between adjacent signal paths. An epitaxial layer prevents latch-up.

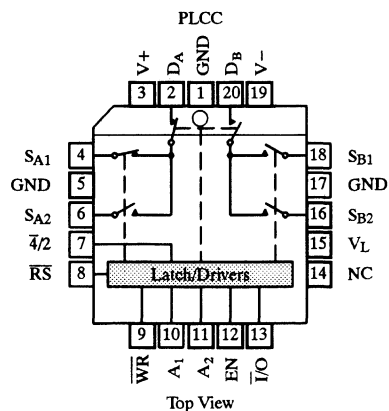
For more information refer to Siliconix Applications Note AN502.

### Functional Block Diagrams and Pin Configurations

DG534ADJ

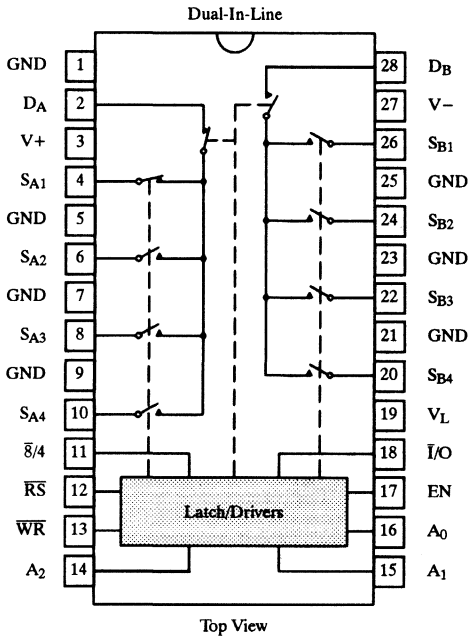


DG534ADN

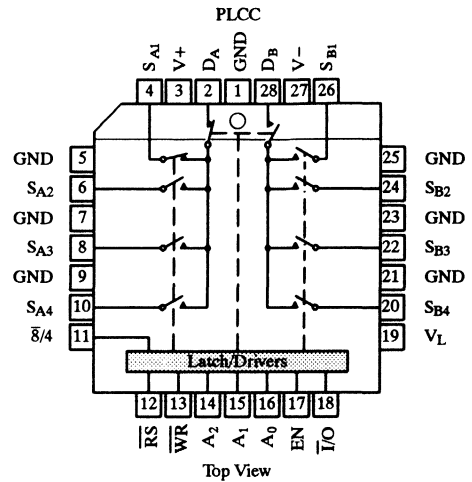


**Functional Block Diagrams and Pin Configurations (Cont'd)**

**DG538ADJ**



**DG538ADN**



**Truth Tables and Ordering Information**

**Ordering Information – DG534A**

Temp Range	Package	Part Number
-40 to 85°C	20-Pin Plastic DIP	DG534ADJ
	20-Pin PLCC	DG534ADN
-55 to 125°C	20-Pin Sidebrazed	DG534AAP/883

**Truth Table — DG534A**

I/O	A <sub>1</sub>	A <sub>0</sub>	EN	WR	RS	4/2 <sup>a</sup>	On Switch	Latches Transparent
X	X	X	X	1	1	1	Maintains previous state	
X	X	X	X	X	0	X	None (latches cleared)	
X	X	X	0	0	1	X	None	
0	0	0	1	0	1	0	SA1	
0	0	1	1	0	1	0	SA2	
0	1	0	1	0	1	0	SB1	
0	1	1	1	0	1	0	SB2	
0	X	0	1	0	1	1	SA1 and SB1	
0	X	1	1	0	1	1	SA2 and SB2	
1	Note b		1	1	Note c			

Logic "0" = V<sub>AL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>AH</sub> ≥ 2 V  
 X = Don't Care

**Notes:**

- Connect D<sub>A</sub> and D<sub>B</sub> together externally for single-ended operation.
- With I/O high, A<sub>n</sub> and EN pins become outputs and reflect latch contents. See timing diagrams for more detail.
- 4/2 can be either "1" or "0" but should not change during these operations.

## Truth Tables and Ordering Information (Cont'd)

Ordering Information – DG538A

Temp Range	Package	Part Number
-40 to 85°C	28-Pin Plastic DIP	DG538ADJ
	28-Pin PLCC	DG538ADN
-55 to 125°C	28-Pin Sidebrazed	DG538AAP/883

Truth Table — DG538A

I/O	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	WR	RS	8/4 <sup>a</sup>	On Switch		
X	X	X	X	X	$\bar{J}$	1	1	Maintains previous state		
X	X	X	X	X	X	0	X	None (latches cleared)		
X	X	X	X	0	0	1	X	None		
0	0	0	0	1	0	1	0	SA1	D <sub>A</sub> and D <sub>B</sub> should be connected externally	
0	0	0	1	1	0	1	0	SA2		
0	0	1	0	1	0	1	0	SA3		
0	0	1	1	1	0	1	0	SA4		
0	1	0	0	1	0	1	0	SB1		
0	1	0	1	1	0	1	0	SB2		
0	1	1	0	1	0	1	0	SB3		
0	1	1	1	1	0	1	0	SB4		
0	X	0	0	1	0	1	1	SA1 and SB1		
0	X	0	1	1	0	1	1	SA2 and SB2		
0	X	1	0	1	0	1	1	SA3 and SB3		
0	X	1	1	1	0	1	1	SA4 and SB4		
1	Note b				1	1	Note c			

Logic "0" =  $V_{AL} \leq 0.8 V$

Logic "1" =  $V_{AH} \geq 2 V$

X = Don't Care

Notes:

- Connect D<sub>A</sub> and D<sub>B</sub> together externally for single-ended operation.
- With I/O high, A<sub>n</sub> and EN pins become outputs and reflect latch contents. See timing diagrams for more detail.
- 8/4 can be either "1" or "0" but should not change during these operations.

## Absolute Maximum Ratings

V <sub>+</sub> to GND	-0.3 V to +21 V
V <sub>+</sub> to V <sub>-</sub>	-0.3 V to +21 V
V <sub>-</sub> to GND	-10 V to +0.3 V
V <sub>L</sub>	0 V to (V <sub>+</sub> ) + 0.3 V
Digital Inputs	(V <sub>-</sub> ) -0.3 V to (V <sub>L</sub> ) + 0.3 V or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub>	(V <sub>-</sub> ) -0.3 V to (V <sub>-</sub> ) + 14 V or 20 mA, whichever occurs first
Current (any terminal) Continuous	20 mA
Current(S or D) Pulsed 1 ms 10% Duty	40 mA

Storage Temperature (A Suffix)	-65 to 150°C
(D Suffix)	-65 to 125°C

Power Dissipation (Package) <sup>a</sup>	
Plastic DIP <sup>b</sup>	625 mW
PLCC <sup>c</sup>	450 mW
Sidebrazed <sup>d</sup>	1200 mW

Notes:

- All leads soldered or welded to PC board.
- Derate 8.3 mW/°C above 75°C.
- Derate 6 mW/°C above 75°C.
- Derate 16 mW/°C above 75°C.

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}, V_L = 5\text{ V}$ $WR = 0.8\text{ V}, RS, EN = 2\text{ V}$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>g</sup>	V <sub>ANALOG</sub>	V <sub>-</sub> = -5 V	Full		-5	8	-5	8	V	
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>S</sub> = 0 V V <sub>AIL</sub> = 0.8 V, V <sub>AIH</sub> = 2 V Sequence Each Switch On	Room Full	45		90		90	Ω	
Resistance Match Between Channels	Δr <sub>DS(on)</sub>		Room			9		9		
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = 8 V, V <sub>D</sub> = 0 V, EN = 0.8 V	Room Full	0.05	-5 -50	5 50	-5 -50	5 50	nA	
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>S</sub> = 0 V, V <sub>D</sub> = 8 V, EN = 0.8 V	Room Full	0.1	-20 -500	20 500	-20 -100	20 100		
Drain On Leakage Current	I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = 8 V	Room Full	0.1	-20 -1000	20 1000	-20 -200	20 200		
<b>Digital Control</b>										
Input Voltage High	V <sub>AIH</sub>		Full		2		2		V	
Input Voltage Low	V <sub>AIL</sub>		Full			0.8		0.8		
Address Input Current	I <sub>AI</sub>	V <sub>AI</sub> = 0 V, or 2 V or 5 V	Room Full	-0.1	-1 -10	1 10	-1 -10	1 10	μA	
Address Output Current	I <sub>AO</sub>	V <sub>AO</sub> = 2.7 V	Room	-21		-2.5		-2.5	mA	
		V <sub>AO</sub> = 0.4 V	Room	3.5	2.5		2.5			
<b>Dynamic Characteristics</b>										
On State Input Capacitance <sup>g</sup>	C <sub>S(on)</sub>	See Figure 11	PLCC	Room	28		40		40	pF
			DIP	Room	31		45		45	
Off State Input Capacitance <sup>g</sup>	C <sub>S(off)</sub>	See Figure 12	PLCC	Room	3		5		4	
			DIP	Room	4				5	
Off State Output Capacitance <sup>g</sup>	C <sub>D(off)</sub>		PLCC	Room	6		10		8	
			DIP	Room	8				10	
Transition Time	t <sub>TRANS</sub>	See Figure 4	Room Full	160		300 500		300 500	ns	
Break-Before-Make Interval	t <sub>OPEN</sub>		Room Full	80	50 25		50 25			
EN, WR Turn On Time	t <sub>ON</sub>	See Figure 2 and 3	Room Full	150		300 500		300 500		
EN, Turn Off Time	t <sub>OFF</sub>	See Figure 2	Room Full	105		175 300		175 300		
Charge Injection	Q <sub>i</sub>	See Figure 5	Room	-70					pC	
Chip Disabled Crosstalk <sup>f</sup>	X <sub>TALK(CD)</sub>	R <sub>L</sub> = 75 Ω, f = 5 MHz EN = 0.8 V, See Figure 8	PLCC	Room	-75					dB
			DIP	Room	-65					
Adjacent Input Crosstalk <sup>f</sup>	X <sub>TALK(AI)</sub>	R <sub>IN</sub> = 10 Ω, R <sub>L</sub> = 10 kΩ f = 5 MHz, See Figure 9	PLCC	Room	-97					
			DIP	Room	-87					
		R <sub>IN</sub> = 75 Ω, R <sub>L</sub> = 75 Ω f = 5 MHz, See Figure 9	PLCC	Room	-80					
			DIP	Room	-70					

## Specifications<sup>a</sup>

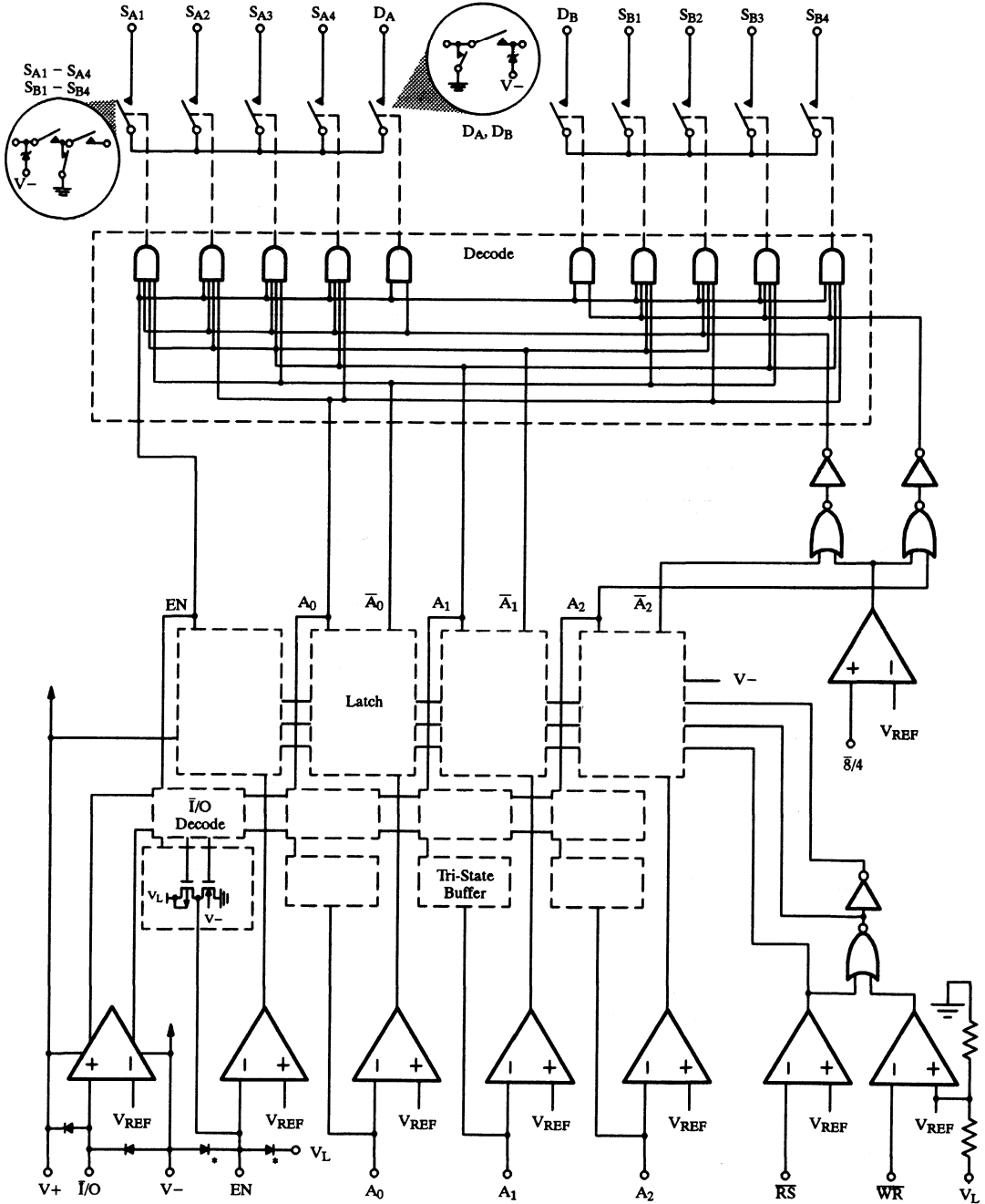
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}, V_L = 5\text{ V}$ $\overline{WR} = 0.8\text{ V}, \overline{RS}, \overline{EN} = 2\text{ V}$		Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
						Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
<b>Dynamic Characteristics (Cont'd)</b>											
All Hostile Crosstalk	$X_{\text{TALK(AH)}}$	$R_{\text{IN}} = 10\ \Omega, R_L = 10\ \text{k}\Omega$ $f = 5\ \text{MHz}$ , See Figure 7	PLCC	Room	-77					dB	
			DIP	Room	-72						
		$R_{\text{IN}} = 75\ \Omega, R_L = 75\ \Omega$ $f = 5\ \text{MHz}$ , See Figure 7	PLCC	Room	-77						
			DIP	Room	-72						
Differential Crosstalk	$X_{\text{TALK(DIFF)}}$	$R_{\text{IN}} = 10\ \Omega, R_L = 10\ \text{k}\Omega$ $f = 5\ \text{MHz}$ , See Figure 10		Room	-84						
		$R_{\text{IN}} = R_L = 75\ \Omega$ $f = 5\ \text{MHz}$ , See Figure 10		Room	-84						
Bandwidth	BW	$R_L = 50\ \Omega$ , See Figure 6		Room	500					MHz	
<b>Power Supplies</b>											
Positive Supply Current	I+	Any One Channel Selected with Address Inputs at GND or 5 V		Room	0.6		2		2	mA	
Negative Supply Current	I-			Full	0.6	-1.8 -2		-1.8 -2			5
Functional Check of Maximum Operating Supply Voltage Range	V+ to V-	Functional Test Only		Full		10	21	10	21	V	
	V- to GND			Full		-5.5	0	-5.5	0		
	V+ to GND			Full		10	21	10	21		
Logic Supply Current	I <sub>L</sub>			Full	150		500		500	μA	
<b>Timing</b>											
Reset to Write	t <sub>RW</sub>	See Figure 1		Room	-22			50		ns	
$\overline{WR}, \overline{RS}$ Minimum Pulse Width	t <sub>MPW</sub>			Room	60		200		200		
A <sub>0</sub> , A <sub>1</sub> , EN Data Valid to Strobe	t <sub>DW</sub>			Room	20		100		100		
A <sub>0</sub> , A <sub>1</sub> , EN Data Valid after Strobe	t <sub>WD</sub>			Room	-20		50		50		
Address Bus Tri-State <sup>e</sup>	t <sub>AZ</sub>			Room	25						
Address Bus Output	t <sub>AO</sub>			Room	95						
Address Bus Input	t <sub>AI</sub>			Room	110						

**Notes:**

- Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Defined by system bus requirements.
- Each individual pin shown as GND must be grounded.
- Guaranteed by design, not subject to production test.

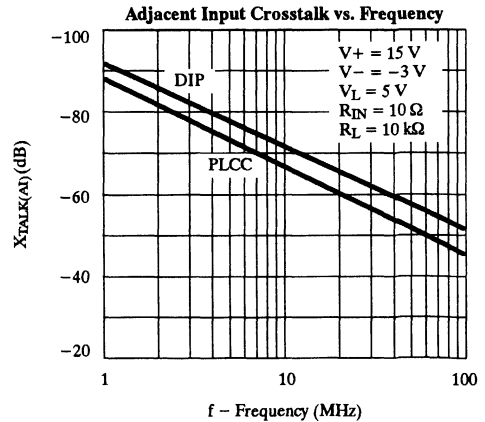
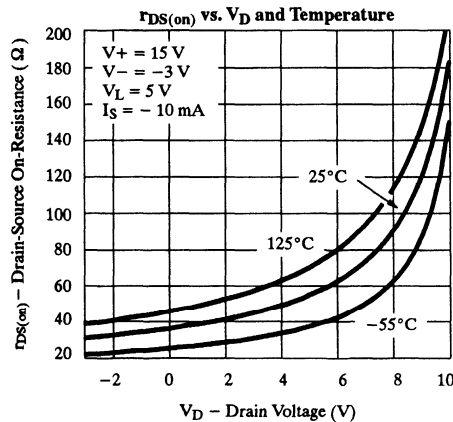
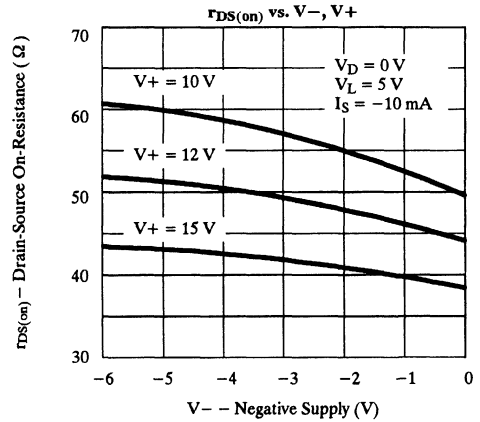
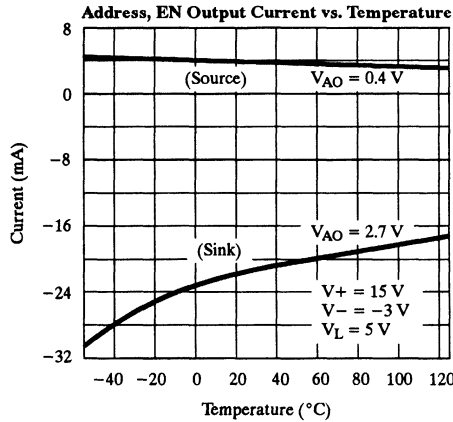
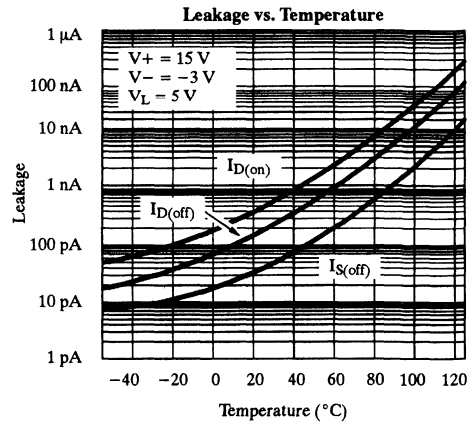
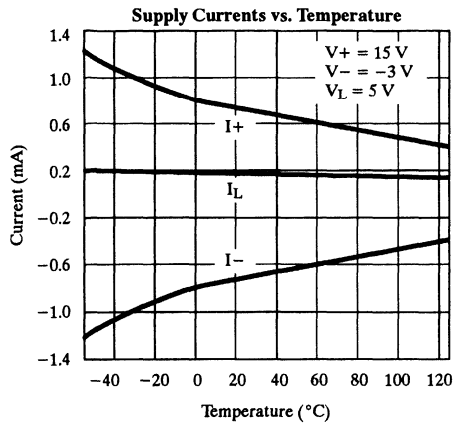


**Control Circuitry**

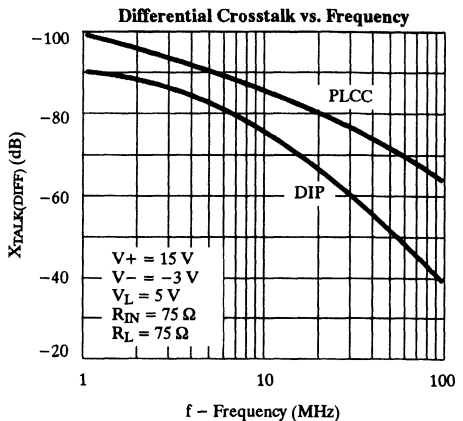
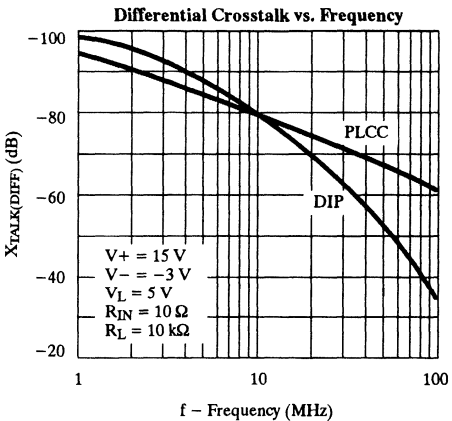
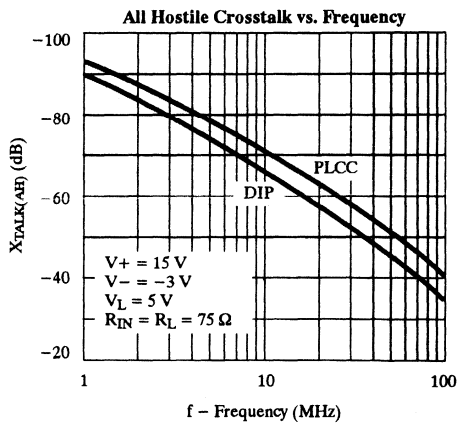
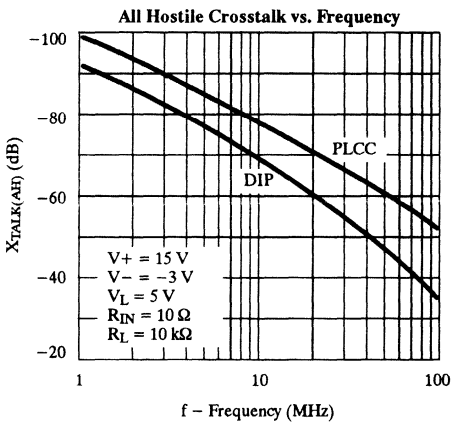
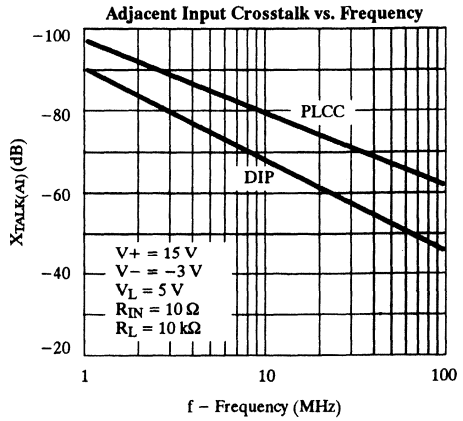
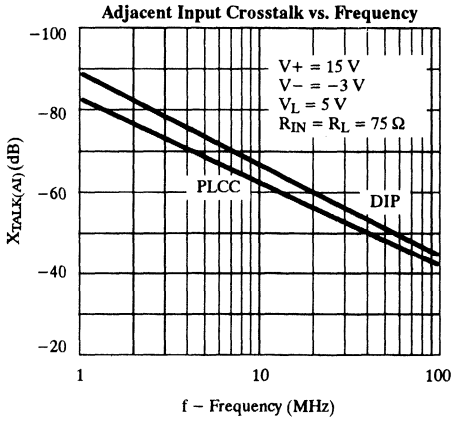


\*Typical all Readback (Ax, EN) pins

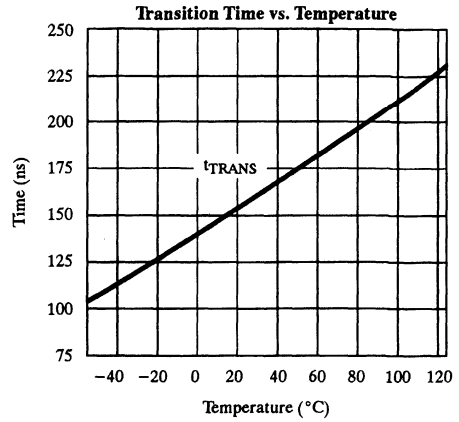
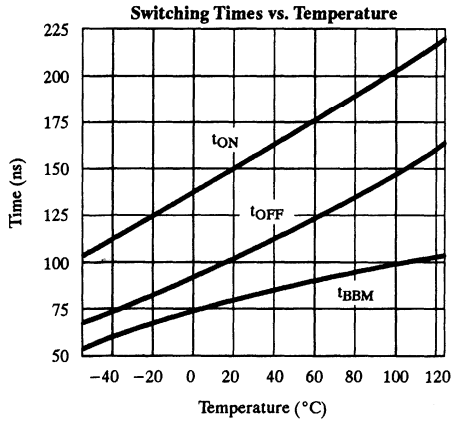
## Typical Characteristics



**Typical Characteristics (Cont'd)**



## Typical Characteristics (Cont'd)



## Output Timing Requirements

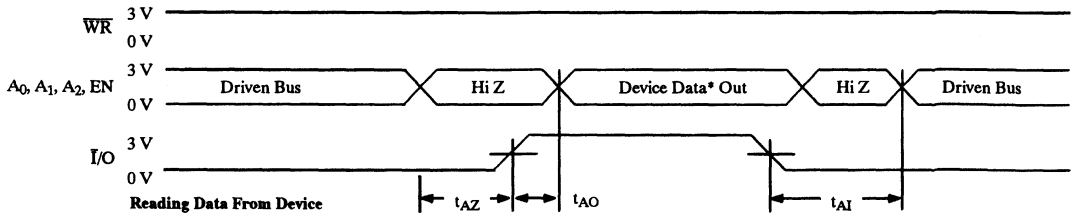
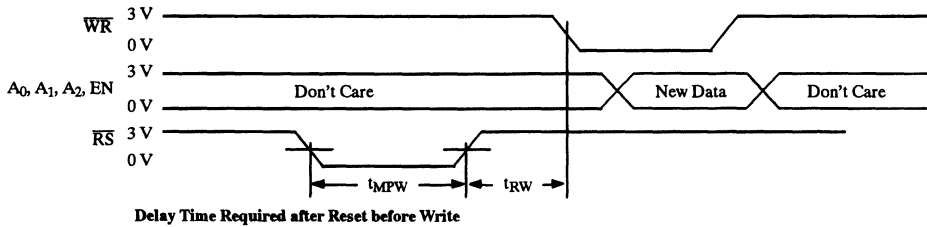
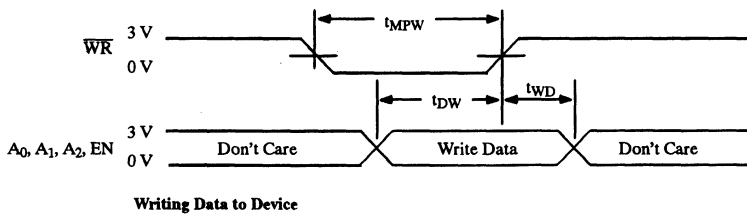
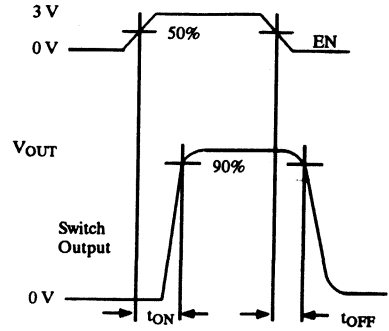
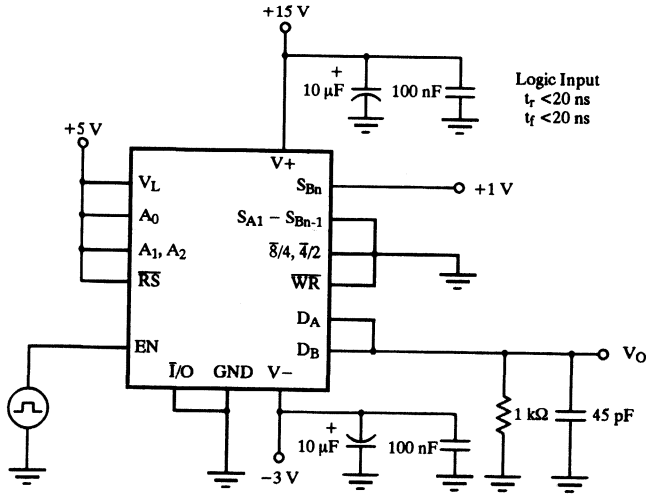
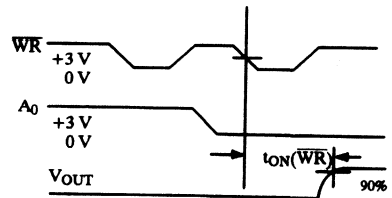
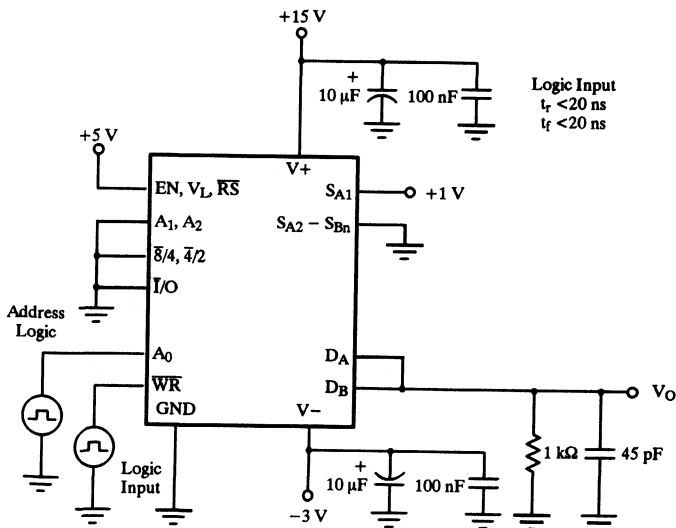


Figure 1.

**Test Circuits**



**Figure 2.** EN, CS,  $\overline{\text{CS}}$ , Turn On/Off Time



**Figure 3.** WR, Turn On Time

## Test Circuits (Cont'd)

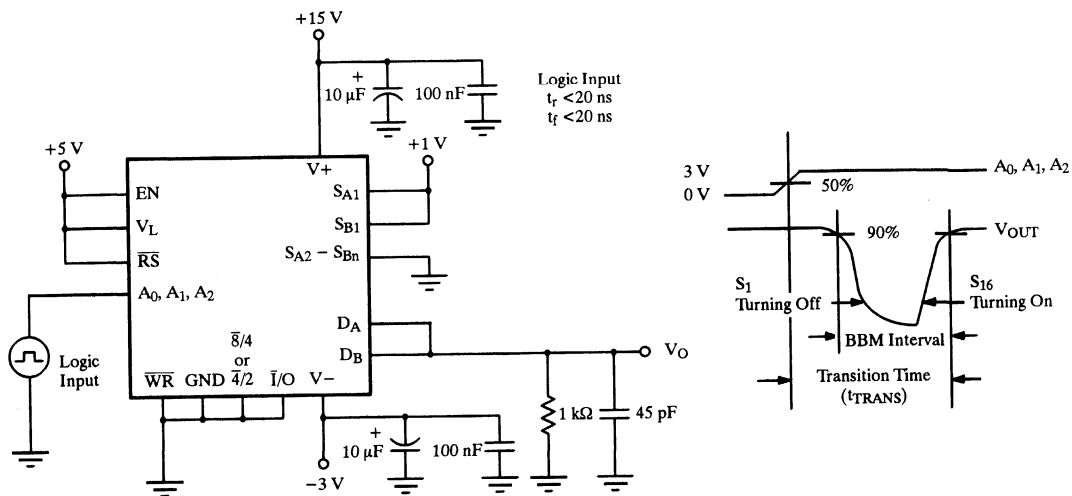


Figure 4. Transition Time and Break-Before-Make Interval

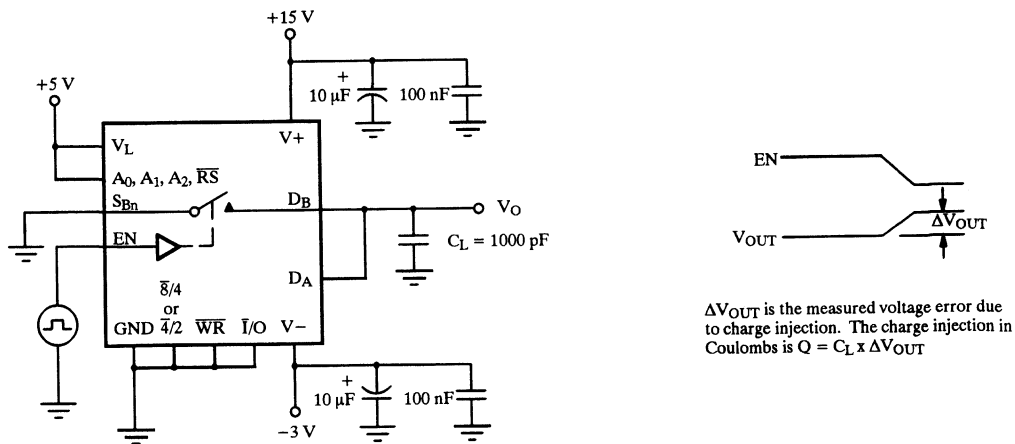
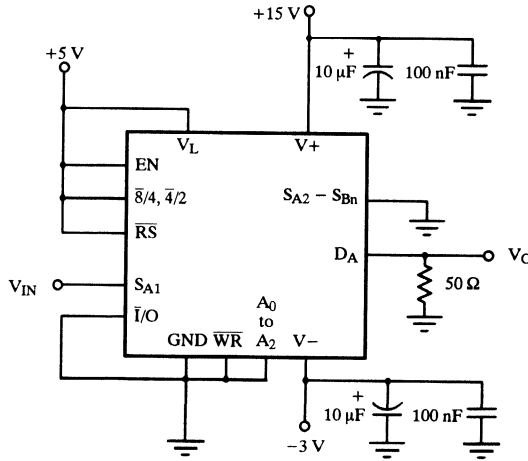
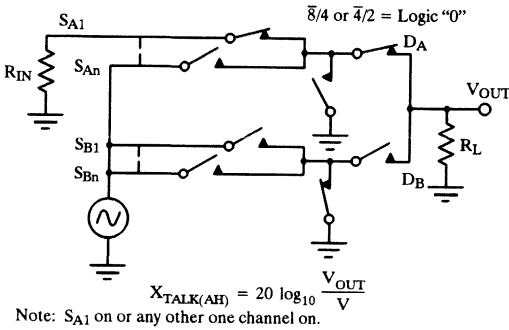


Figure 5. Charge Injection

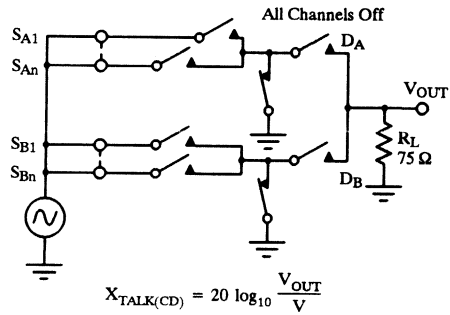
**Test Circuits (Cont'd)**



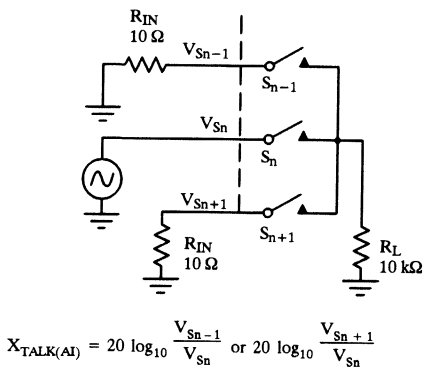
**Figure 6.** Bandwidth



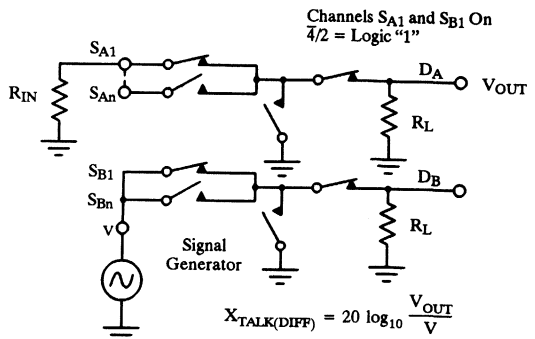
**Figure 7.** All Hostile Crosstalk



**Figure 8.** Chip Disabled Crosstalk



**Figure 9.** Adjacent Input Crosstalk



**Figure 10.** Differential Crosstalk

## Test Circuits (Cont'd)

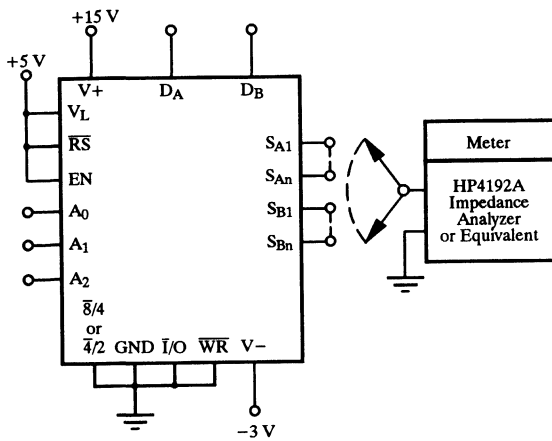


Figure 11. On State Input Capacitance

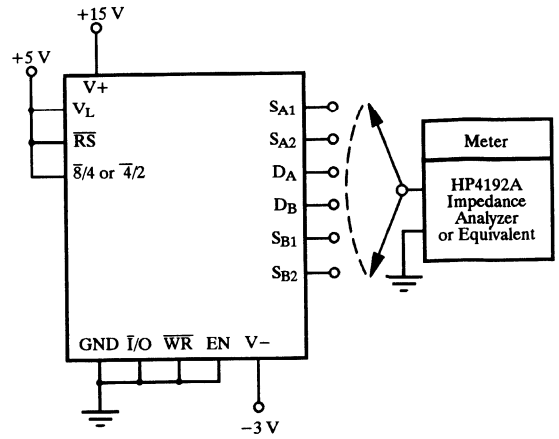
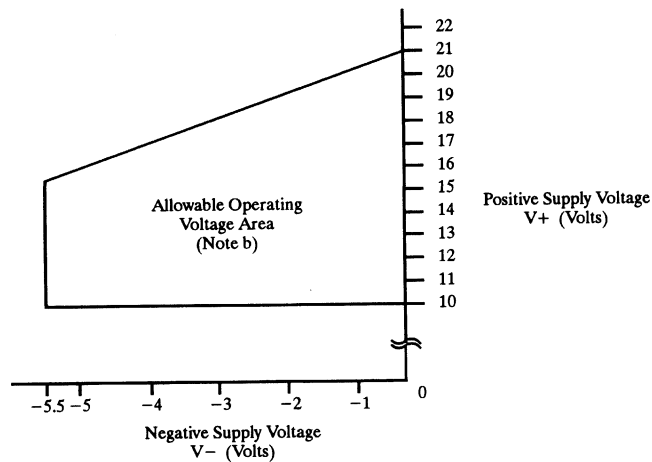


Figure 12. Off State Input/Output Capacitance

## Operating Voltage Range



**Notes:**

- a. Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10- $\mu$ F tantalum bead in parallel with 100-nF ceramic disc.
- b. Production tested with V+ = 15 V and V- = -3 V.
- a. For V<sub>L</sub> = 5 V  $\pm$  10%, 0.8- or 2-V TTL compatibility is maintained over the entire operating voltage range.

Figure 13.



**Pin Description**

Symbol	Pin Number		Description
	DG534A	DG538A	
D <sub>A</sub>	2	2	Analog Output/Input
V <sub>+</sub>	3	3	Positive Supply Voltage
S <sub>A1</sub>	4	4	Analog Input/Output
S <sub>A2</sub>	6	6	Analog Input/Output
S <sub>A3</sub>	–	8	Analog Input/Output
S <sub>A4</sub>	–	10	Analog Input/Output
$\bar{4}/2$	7	–	4 x 1 or 2 x 2 Select
$\bar{8}/4$	–	11	8 x 1 or 4 x 2 Select
$\bar{R}\bar{S}$	8	12	Reset
$\bar{W}\bar{R}$	9	13	Write command that latches A, EN
A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub>	11, 10, –	16, 15, 14	Binary address inputs that determine which channel(s) is/are connected to the output(s)
EN	12	17	Enable. Input/Output, if EN = 0, all channels are open
$\bar{I}/O$	13	18	Input/Output control. Used to write to or read from the address latches
V <sub>L</sub>	14	19	Logic Supply Voltage, usually +5 V
S <sub>B4</sub>	–	20	Analog Input/Output
S <sub>B3</sub>	–	22	Analog Input/Output
S <sub>B2</sub>	15	24	Analog Input/Output
S <sub>B1</sub>	17	26	Analog Input/Output
V <sub>–</sub>	18	27	Negative Supply Voltage
D <sub>B</sub>	19	28	Analog Output/Input
GND	1, 5, 16	1, 5, 7, 9, 21, 23, 25	Analog and Digital Grounds. All grounds should be connected externally to optimize dynamic performance

**Applications**

**Device Description**

The DG534A/538A D/CMOS wideband multiplexers offer single-ended or differential functions. A  $\bar{8}/4$  or  $\bar{4}/2$  logic input pin selects the single-ended or differential mode.

To meet the high dynamic performance demands of video, high definition TV, digital data routing (in excess of 100 Mbps), etc., the DG534A/538A are fabricated with DMOS transistors configured in 'T' arrangements with second level 'L' configurations (see Functional Block Diagram).

Use of DMOS technology yields devices with very low capacitance and low r<sub>DS(on)</sub>. This directly relates to improved high frequency signal handling and higher switching speeds, while maintaining low insertion loss figures. The 'T' and 'L' switch configurations further

improve dynamic performance by greatly reducing crosstalk and output node capacitances.

The DG534A/DG538A are improved pin-compatible replacements for the non-A versions. Improvements include: higher current readback drivers, readback of the EN bit, latchup protection

**Frequency Response**

A single multiplexer on-channel exhibits both resistance (r<sub>DS(on)</sub>) and capacitance (C<sub>S(on)</sub>). This RC combination causes a frequency dependent attenuation of the analog signal. The –3-dB bandwidth of the DG534A/538A is typically 500 MHz (into 50 Ω). This figure of 500 MHz illustrates that the switch-channel cannot be represented by a simple RC combination. The on capacitance of the channel is distributed along the on-resistance, and hence becomes a more complex multi-stage network of R's and C's making up the total r<sub>DS(on)</sub> and C<sub>S(on)</sub>.

# DG534A/538A

## Applications (Cont'd)

### Power Supplies and Decoupling

A useful feature of the DG534A/538A is its power supply flexibility. It can be operated from unipolar supplies ( $V^-$  connected to 0 V) if required. Allowable operating voltage ranges are shown in Figure 13.

Note that the analog signal must not go below  $V^-$  by more than 0.3 V (see absolute maximum ratings). However, the addition of a  $V^-$  pin has a number of advantages:

- It allows flexibility in analog signal handling, i.e. with  $V^- = -5$  V and  $V^+ = 15$  V, up to  $\pm 5$  V ac signals can be accepted.
- The value of on capacitance ( $C_{S(on)}$ ) may be reduced by increasing the reverse bias across the internal FET body to source junction.  $V^+$  has no effect on  $C_{S(on)}$ .  
It is useful to note that tests indicate that optimum video differential phase and gain occur when  $V^-$  is  $-3$  V.
- $V^-$  eliminates the need to bias an ac analog signal using potential dividers and large decoupling capacitors.

It is established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG534/538 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

#### Rules:

- Decoupling capacitors should be incorporated on all power supply pins ( $V^+$ ,  $V^-$ ,  $V_L$ ).
- They should be mounted as close as possible to the device pins.
- Capacitors should have good frequency characteristics - tantalum bead and/or ceramic disc types are suitable. Recommended decoupling capacitors are 1- to 10- $\mu$ F tantalum bead, in parallel with 100-nF ceramic or polyester.
- Additional high frequency protection may be provided by 51- $\Omega$  carbon film resistors connected in series with the power supply pins (see Figure 14).

### Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by the DG534A/538A. Some tips for minimizing stray effects are:

- Use extensive ground planes on double sided PCB separating adjacent signal paths. Multilayer PCB is even better.
- Keep signal paths as short as practically possible with all channel paths of near equal length.
- Use strip-line layout techniques.

Improvements in performance can be obtained by using PLCC parts instead of DIPs. The stray effects of the quad PLCC package are lower than those of the dual-in-line packages. Sockets for the PLCC packages usually increase crosstalk.

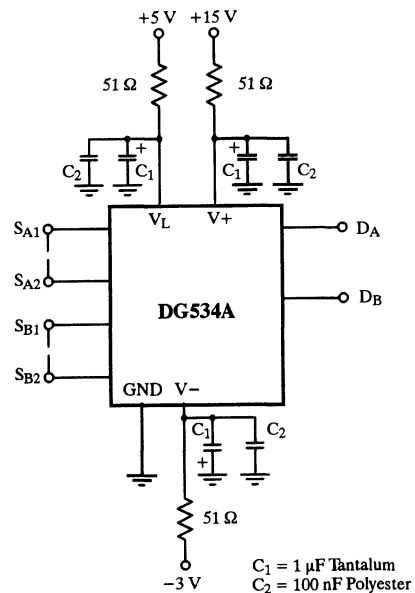


Figure 14. DG534A Power Supply Decoupling

### Interfacing

Logic interfacing is easily accomplished. Comprehensive addressing and control functions are incorporated in the design.

The  $V_L$  pin permits interface to various logic types. The device is primarily designed to be TTL or CMOS logic compatible with +5 V applied to  $V_L$ . The actual logic threshold can be raised simply by increasing  $V_L$ .

A typical switching threshold versus  $V_L$  is shown in Figure 15.

These devices feature an address readback (Tally) facility, whereby the last address written to the device may be output to the system. This allows improved status monitoring and hand shaking without additional external components.

**Applications (Cont'd)**

This function is controlled by the  $\bar{I}/O$  pin, which directly addresses the tri-state buffers connected to the EN and address pins. EN and address pins can be assigned to accept data (when  $\bar{I}/O = 0$ ;  $\overline{WR} = 0$ ;  $\overline{RS} = 1$ ), or output data (when  $\bar{I}/O = 1$ ;  $\overline{WR} = 1$ ;  $\overline{RS} = 1$ ), or to reflect a high impedance and latched state (when  $\bar{I}/O = 0$ ;  $\overline{WR} = 1$ ;  $\overline{RS} = 1$ ).

When  $\bar{I}/O$  is high, the address output can sink or source current. Note that  $V_L$  is the logic high output condition. This point must be respected if  $V_L$  is varied for input logic threshold shifting.

Further control pins facilitate easy microprocessor interface. On chip address, data latches are activated by  $\overline{WR}$ , which serves as a strobe type function eliminating the need for peripheral latch or memory I/O port devices. Also,

for ease of interface, a direct reset function ( $\overline{RS}$ ) allows all latches to be cleared and switches opened. Reset should be used during power up, etc., to avoid spurious switch action. See Figure 16.

Channel address data can only be entered during  $\overline{WR}$  low, when the address latches are transparent and  $\bar{I}/O$  is low. Similarly, address readback is only operational when  $\overline{WR}$  and  $\bar{I}/O$  are high.

The Siliconix Si582 Video amplifier is recommended as an output buffer to reduce insertion loss and to drive coaxial cables. For low power video routing applications or for unity gain input buffers Siliconix Si581/Si584 are recommended.

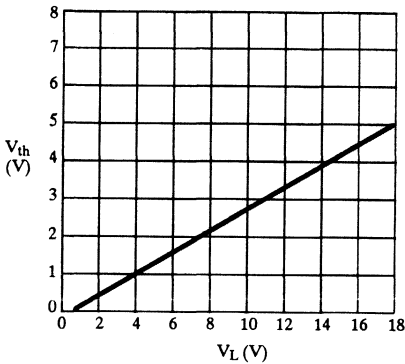


Figure 15. Switching Threshold Voltage vs. VL

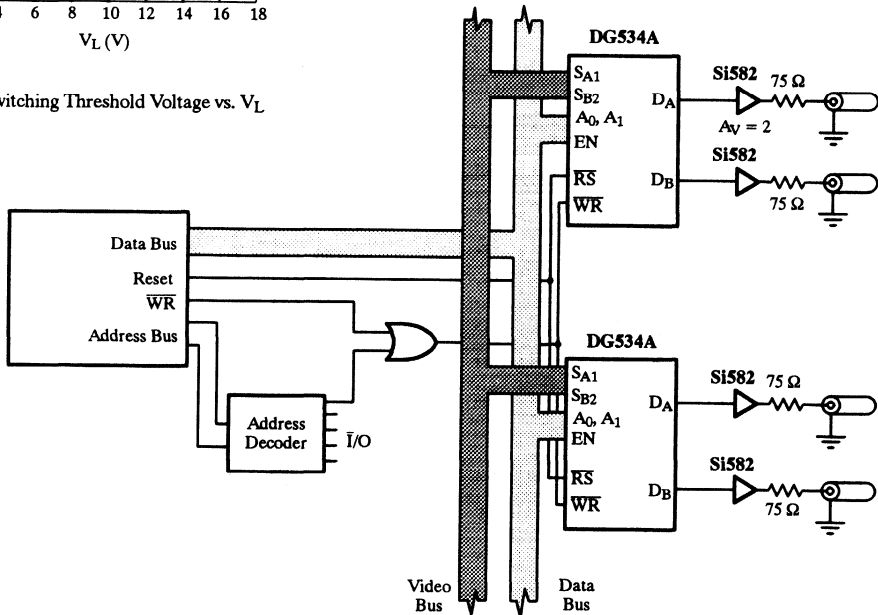


Figure 16. DG534A in a Video Matrix

## 16-Channel Wideband Video Multiplexers

### Features

- Crosstalk:  $-100\text{ dB @ }5\text{ MHz}$
- 300 MHz Bandwidth
- Low Input and Output Capacitance
- Low Power:  $75\ \mu\text{W}$
- Low  $r_{DS(on)}$ :  $50\ \Omega$
- On-Board Address Latches
- Disable Output

### Benefits

- High Video Quality
- Reduced Insertion Loss
- Reduced Input Buffer Requirements
- Minimizes Power Consumption
- Simplifies Bus Interface

### Applications

- Video Switching/Routing
- High Speed Data Routing
- RF Signal Multiplexing
- Precision Data Acquisition
- Crosspoint Arrays
- FLIR Systems

### Description

The DG535/536 are 16-channel multiplexers designed for routing one of 16 wideband analog or digital input signals to a single output. They feature low input and output capacitance, low on-resistance, and n-channel DMOS “T” switches, resulting in wide bandwidth, low crosstalk and high “off” isolation. In the on state, the switches pass signals in either direction, allowing them to be used as multiplexers or as demultiplexers.

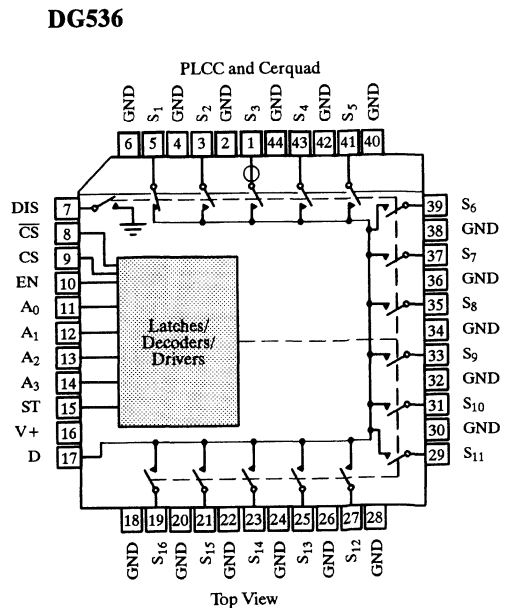
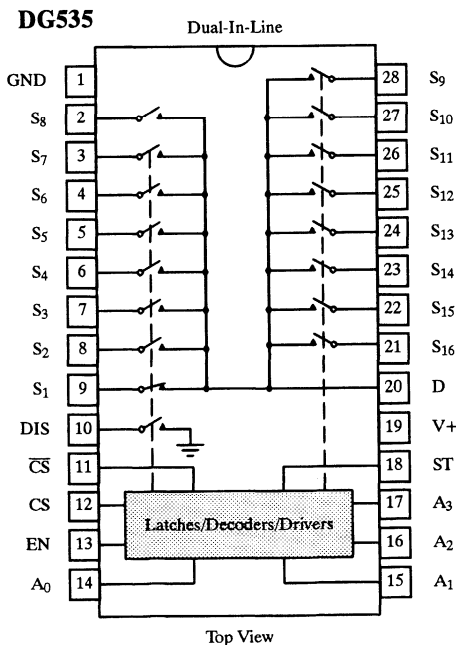
On-chip address latches and decode logic simplify microprocessor interface. Chip Select and Enable inputs

simplify addressing in large matrices. Single-supply operation and a low  $75\text{-}\mu\text{W}$  power consumption vastly reduces power supply requirements.

These devices are built on a proprietary D/CMOS process which creates low-capacitance DMOS FETs and high-speed, low-power CMOS logic on the same substrate.

For more information please refer to Siliconix Application Note AN501.

### Functional Block Diagrams and Pin Configurations



**Truth Tables and Ordering Information**

**Ordering Information**

Temp Range	Package	Part Number
-40 to 85°C	28-Pin Plastic DIP	DG535DJ
	28-Pin Sidebrazed	DG535AP
		DG535AP/883
-55 to 125°C	44-Pin PLCC	DG536DN
	44-Pin Cerquad	DG536AM/883

**Truth Table**

EN	CS	$\overline{CS}$	ST <sup>a</sup>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Channel Selected	Disable <sup>b</sup>
0	X	X	1	X	X	X	X	None	High Z
X	0	X		X	X	X	X	S <sub>1</sub> S <sub>2</sub> S <sub>3</sub> S <sub>4</sub> S <sub>5</sub> S <sub>6</sub> S <sub>7</sub> S <sub>8</sub> S <sub>9</sub> S <sub>10</sub> S <sub>11</sub> S <sub>12</sub> S <sub>13</sub> S <sub>14</sub> S <sub>15</sub> S <sub>16</sub>	Low Z
X	X	1		0	0	0	0		
1	1	0	1	0	0	0	0		
				0	0	0	1		
				0	0	1	0		
				0	0	1	1		
				0	1	0	0		
				0	1	0	1		
				0	1	1	0		
				0	1	1	1		
				1	0	0	0		
				1	0	0	1		
				1	0	1	0		
				1	0	1	1		
				1	1	0	0		
				1	1	0	1		
				1	1	1	0		
				1	1	1	1		
X	X	X	0	X	X	X	X	Maintains previous switch condition	High Z or Low Z

Logic "0" = V<sub>AL</sub> ≤ 4.5 V  
 Logic "1" = V<sub>AH</sub> ≥ 10.5 V  
 X = Don't Care

**Notes:**

- a. Strobe input (ST) is level triggered.
- b. Low Z, High Z = impedance of Disable Output to GND. Disable output sinks current when any channel is selected.

**Absolute Maximum Ratings**

V+ to GND	-0.3 V to +18 V
Digital Inputs	(GND - 0.3 V) to (V+ plus 2 V) or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub>	(GND - 0.3 V) to V+ plus 2 V) or 20 mA, whichever occurs first
Current (any terminal) Continuous	20 mA
Current (S or D) Pulsed 1 ms 10% duty cycle	40 mA
Storage Temperature (A Suffix)	-65 to 150°C
(D Suffix)	-65 to 125°C
Power Dissipation (Package) <sup>a</sup>	
28-Pin Plastic DIP <sup>b</sup>	625 mW

28-Pin Sidebrazed <sup>c</sup>	1200 mW
44-Pin PLCC <sup>d</sup>	450 mW
44-Pin Cerquad <sup>e</sup>	825 mW

**Notes:**

- a. All leads soldered or welded to PC board.
- b. Derate 8.6 mW/°C above 75°C.
- c. Derate 16 mW/°C above 75°C.
- d. Derate 6 mW/°C above 75°C.
- e. Derate 11 mW/°C above 75°C.

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $ST, CS = 10.5\text{ V}$ $\overline{CS} = 4.5\text{ V}$ , $V_A = 4.5\text{ or }10.5\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min <sup>c</sup>	Max <sup>c</sup>	Min <sup>c</sup>	Max <sup>c</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		0	10	0	10	V	
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -1\text{ mA}$ , $V_D = 3\text{ V}$ $EN = 10.5\text{ V}$ Sequence Each Switch On	Room	55		90		90	$\Omega$	
Resistance Match	$\Delta r_{DS(on)}$		Room			9		9		
Source Off Leakage Current	$I_{S(off)}$	$V_S = 3\text{ V}$ , $V_D = 0\text{ V}$ , $EN = 4.5\text{ V}$	Room		-10	10	-10	10	nA	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = 3\text{ V}$ , $EN = 10.5\text{ V}$	Room		-10	10	-10	10		
Disable Output	$R_{DISABLE}$	$I_{DISABLE} = 1\text{ mA}$ , $EN = 10.5\text{ V}$	Room	100		200		200	$\Omega$	
			Full		250			250		
<b>Digital Control</b>										
Input Voltage High	$V_{AIH}$		Full		10.5		10.5		V	
Input Voltage Low	$V_{AIL}$		Full			4.5		4.5		
Address Input Current	$I_{AI}$	$V_A = \text{GND or } V_+$	Room	<0.01	-1	1	-1	1	$\mu\text{A}$	
Address Input Capacitance	$C_A$		Full	5					pF	
<b>Dynamic Characteristics</b>										
On State Input Capacitance <sup>e</sup>	$C_{S(on)}$	$V_D = V_S = 3\text{ V}$	PLCC	Room	32		45		45	pF
			Cerquad	Room	35					
			DIP	Room	40		55		55	
Off State Input Capacitance <sup>e</sup>	$C_{S(off)}$	$V_S = 3\text{ V}$	PLCC	Room	2		8		8	pF
			Cerquad	Room	5					
			DIP	Room	3					
Off State Output Capacitance <sup>e</sup>	$C_{D(off)}$	$V_D = 3\text{ V}$	PLCC	Room	8		20		20	pF
			Cerquad	Room	12					
			DIP	Room	9					
Multiplexer Switching Time	$t_{TRANS}$	See Figure 4	Full			300		300	ns	
Break-Before-Make Interval	$t_{OPEN}$		Full		25		25			
$EN, CS, \overline{CS}, ST, t_{ON}$	$t_{ON}$	See Figure 2 and 3	Full			300		300		
$EN, CS, \overline{CS}, ST, t_{OFF}$	$t_{OFF}$	See Figure 2	Full			150		150		
Charge Injection	Q	See Figure 5	Room	-35					pC	
Single-Channel Crosstalk	$X_{TALK(SC)}$	$R_{IN} = 75\ \Omega$ , $R_L = 75\ \Omega$ $f = 5\text{ MHz}$ See Figure 9	PLCC	Room	-100					dB
			Cerquad	Room	-93					
			DIP	Room	-60					
Chip Disabled Crosstalk	$X_{TALK(CD)}$	$R_{IN} = R_L = 75\ \Omega$ $f = 5\text{ MHz}$ , $EN = 4.5\text{ V}$ See Figure 8	PLCC	Room	-85					dB
			Cerquad	Room	-84					
			DIP	Room	-60					

**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V, ST, CS} = 10.5\text{ V}$ $\overline{\text{CS}} = 4.5\text{ V, }V_A = 4.5\text{ or }10.5\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>c</sup>	Max <sup>c</sup>	Min <sup>c</sup>	Max <sup>c</sup>	

**Dynamic Characteristics (Cont'd)**

Parameter	Symbol	Test Conditions	Package	Temp	Typ	A Suffix	D Suffix	Unit
Adjacent Input Crosstalk	$X_{\text{TALK(AI)}}$	$R_{\text{IN}} = 10\ \Omega, R_L = 10\ \text{k}\Omega$ $f = 5\ \text{MHz}$ See Figure 10	PLCC	Room	-92			dB
			Cerquad	Room	-87			
			DIP	Room	-72			
All Hostile Crosstalk <sup>e</sup>	$X_{\text{TALK(AH)}}$	$R_{\text{IN}} = 10\ \Omega, R_L = 10\ \text{k}\Omega$ $f = 5\ \text{MHz}$ See Figure 7	PLCC	Room	-74	-60	-60	dB
			Cerquad	Room	-74			
			DIP	Room	-60			
Bandwidth	BW	$R_L = 50\ \Omega$ , See Figure 6	Room	500				MHz

**Power Supplies**

Parameter	Symbol	Test Conditions	Temp	Typ	A Suffix	D Suffix	Unit
Positive Supply Current	I+	Any One Channel Selected with All Logic Inputs at GND or V+	Room Full	5	50 100	50 100	$\mu\text{A}$
Supply Voltage Range	V+		Full		10	16.5	V

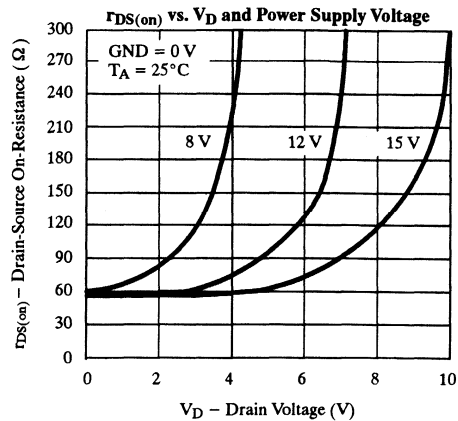
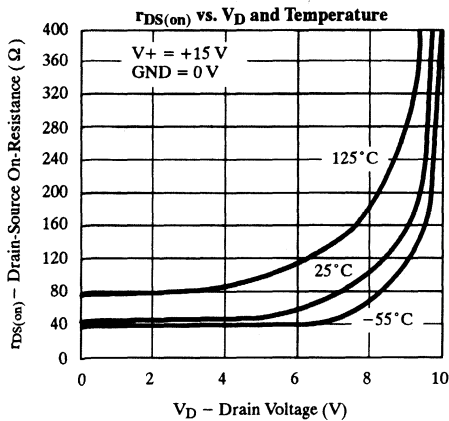
**Minimum Input Timing Requirements**

Parameter	Symbol	Test Conditions	Temp	Typ	A Suffix	D Suffix	Unit
Strobe Pulse Width	$t_{\text{SW}}$	See Figure 1	Full	200		200	ns
$A_0, A_1, A_2, A_3, \overline{\text{CS}}, \overline{\text{EN}}$ Data Valid to Strobe	$t_{\text{DW}}$		Full	100		100	
$A_0, A_1, A_2, A_3, \overline{\text{CS}}, \overline{\text{EN}}$ Data Valid after Strobe	$t_{\text{WD}}$		Full	50		50	

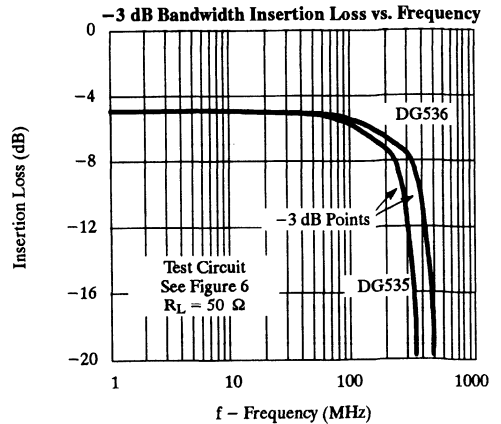
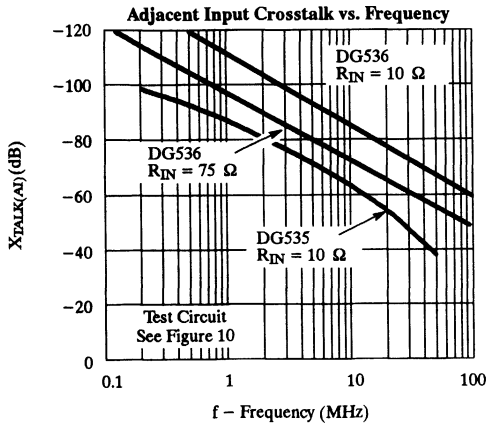
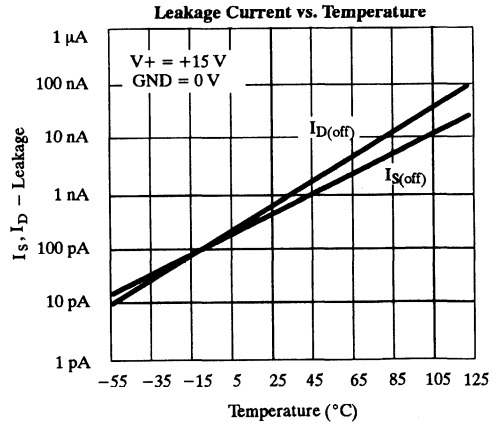
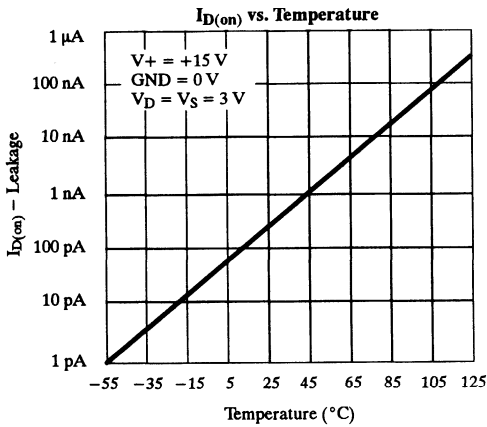
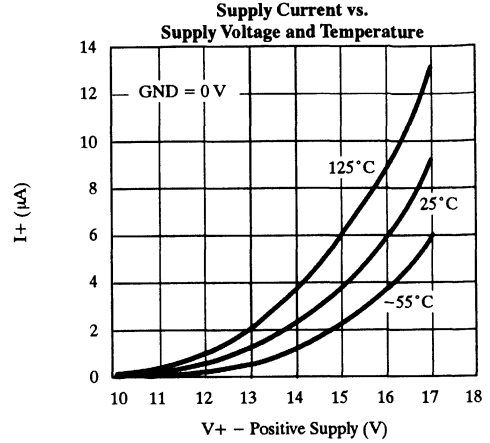
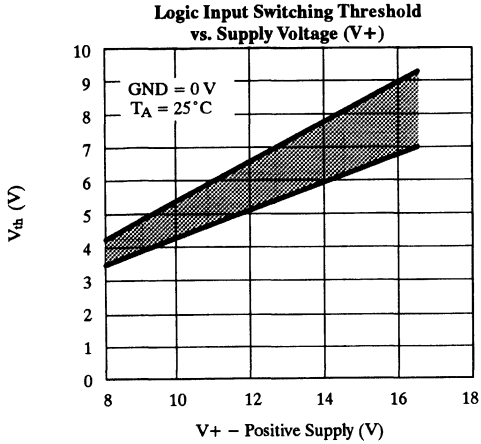
**Notes:**

- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_A$  = input voltage to perform proper function.

**Typical Characteristics**

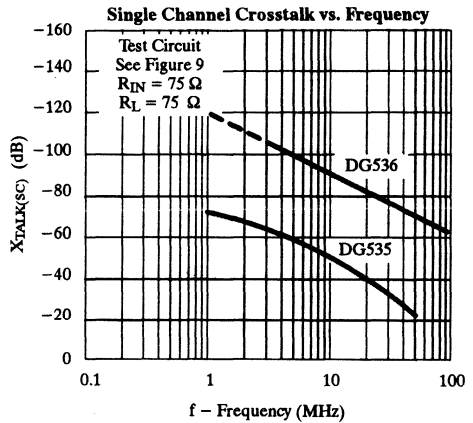
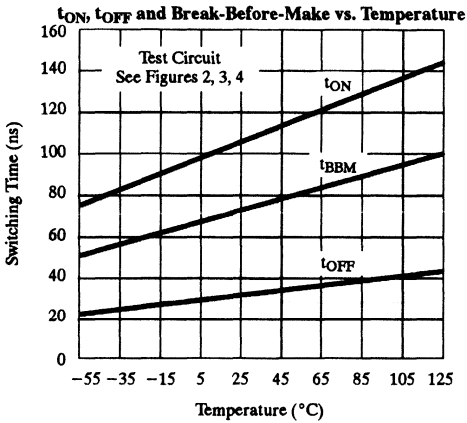
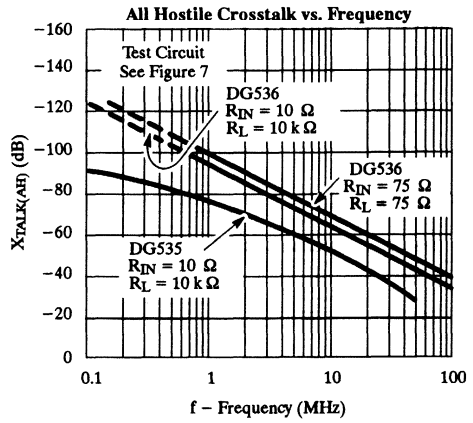
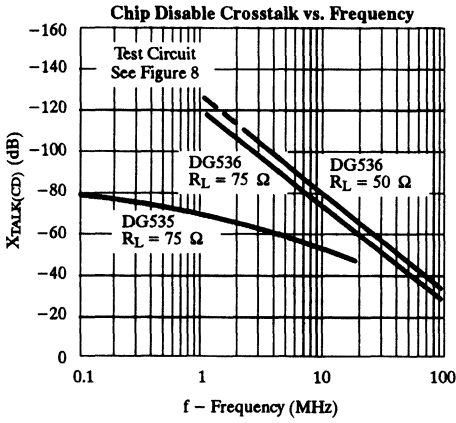


## Typical Characteristics (Cont'd)





**Typical Characteristics (Cont'd)**



**Input Timing Requirements**

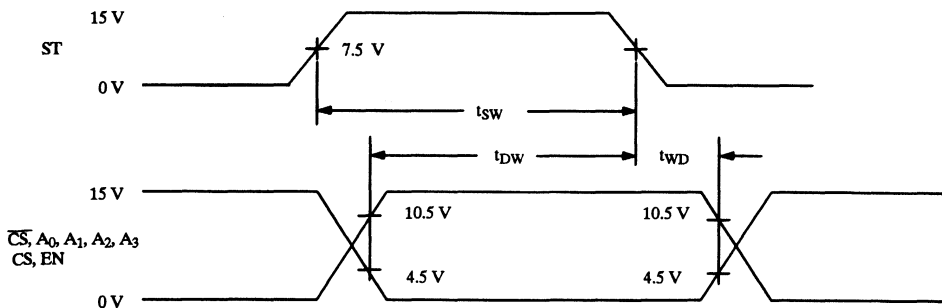


Figure 1.

## Test Circuits

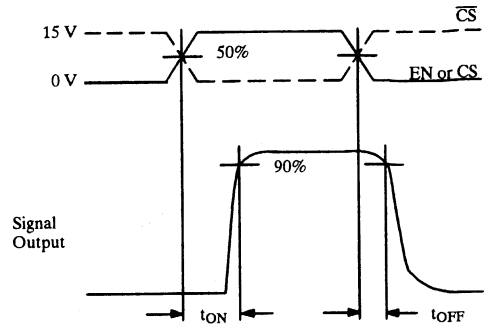
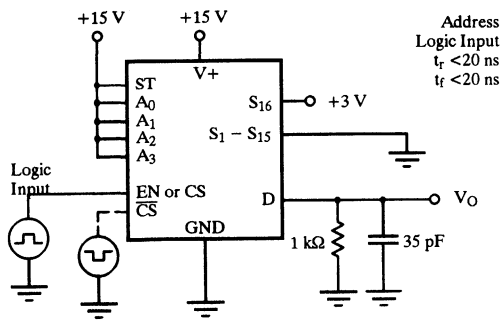


Figure 2. EN, CS,  $\overline{CS}$ , Turn On/Off Time

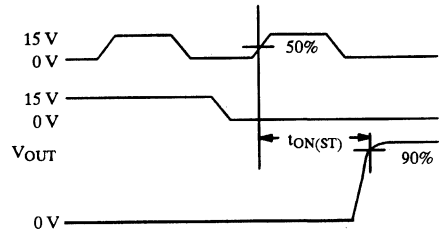
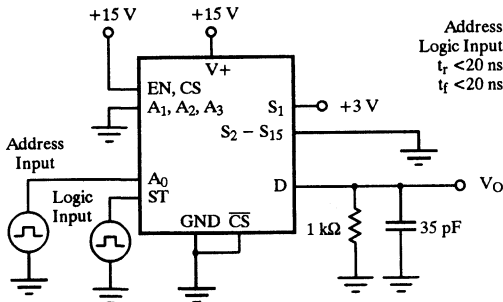


Figure 3. Strobe ST Turn On Time

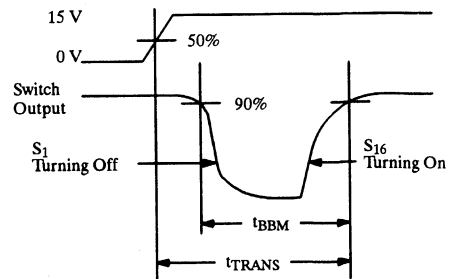
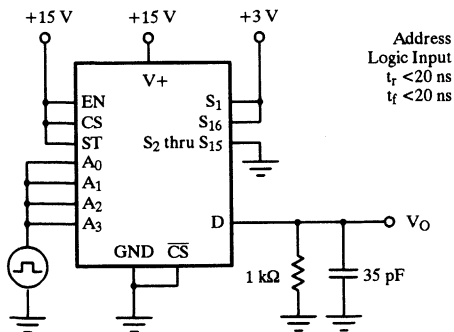
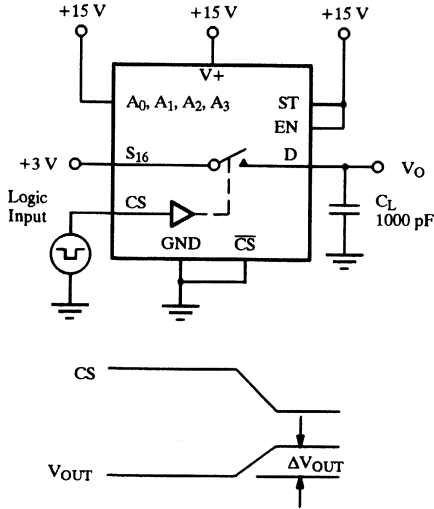


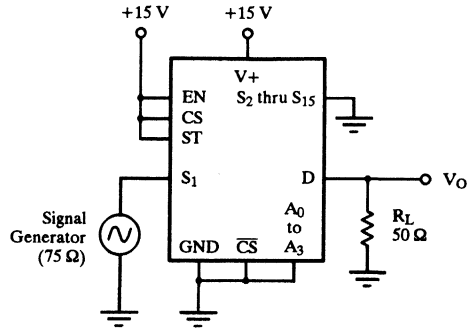
Figure 4. Transition Time and Break-Before-Make Interval

**Test Circuits (Cont'd)**

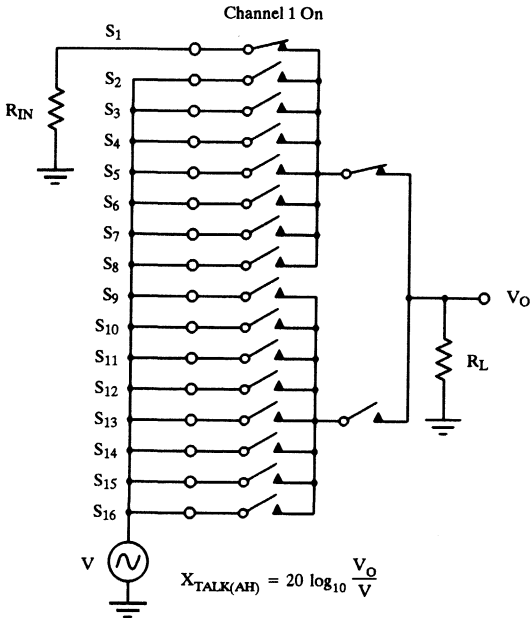


$\Delta V_{OUT}$  is the measured voltage error due to charge injection. The charge injection in Coulombs is  $Q = C_L \times \Delta V_{OUT}$

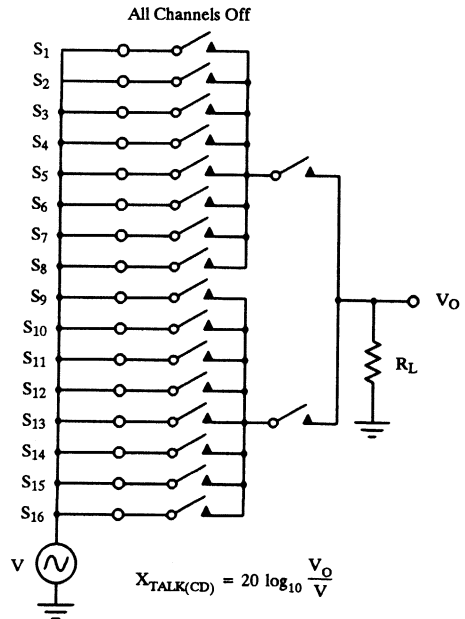
**Figure 5.** Charge Injection



**Figure 6.** Bandwidth

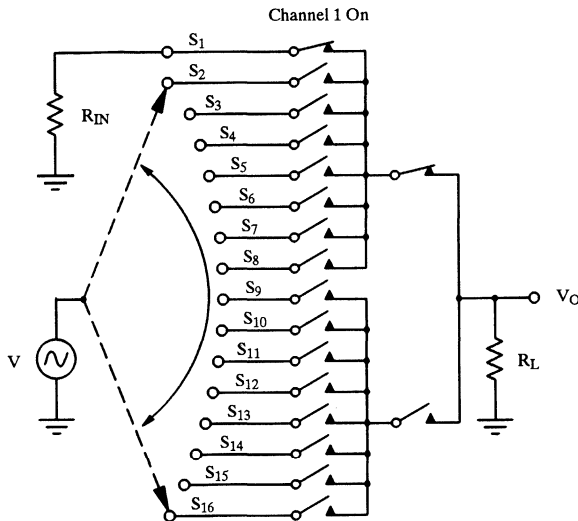


**Figure 7.** All Hostile Crosstalk



**Figure 8.** Chip Disabled Crosstalk

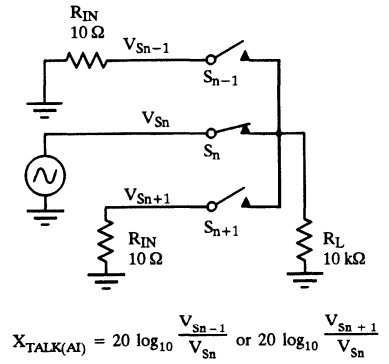
## Test Circuits (Cont'd)



Notes:

1. Any individual channel between  $S_2$  and  $S_{16}$  can be selected
2.  $X_{TALK(SC)} = 20 \log_{10} \frac{V_O}{V}$  is scanned sequentially from  $S_2$  to  $S_{16}$

Figure 9. Single Channel Crosstalk



$$X_{TALK(AI)} = 20 \log_{10} \frac{V_{S_{n-1}}}{V_{S_n}} \text{ or } 20 \log_{10} \frac{V_{S_{n+1}}}{V_{S_n}}$$

Figure 10. Adjacent Input Crosstalk

## Pin Description

Symbol	Description
$S_1$ thru $S_{16}$	Analog inputs/outputs
D	Multiplexer output/demultiplexer input
DIS	Open drain low impedance to analog ground when any channel is selected
$\overline{CS}$ , CS, EN	Logic inputs to selected desired multiplexer(s) when using several multiplexers in a system
$A_0$ thru $A_3$	Binary address inputs to determine which channel is selected
ST	Strobe input that latches $A_0$ , $A_1$ , $A_2$ , $A_3$ , $\overline{CS}$ , CS, EN
V+	Positive supply voltage input
GND	Analog signal ground and most negative potential <b>All ground pins should be connected externally to ensure dynamic performance</b>

## Detailed Description

The DG535/536 are 16-channel single-ended multiplexers with on-chip address logic and control latches.

The multiplexer connects one of sixteen inputs ( $S_1, S_2$  through  $S_{16}$ ) to a common output (D) under the control of a 4-bit binary address ( $A_0$  to  $A_3$ ). The specific input channel selected for each address is given in the Truth Table.

All four address inputs have on-chip data latches which are controlled by the Strobe (ST) input. These latches are transparent when Strobe is high but they maintain the chosen address when Strobe goes low. To facilitate easy microprocessor control in large matrices a choice of three independent logic inputs (EN, CS and  $\overline{CS}$ ) are provided on chip. These inputs are gated together (see Figure 11) and only when  $EN = CS = 1$  and  $\overline{CS} = 0$  can an output switch be selected. This necessary logic condition is then latched-in when Strobe (ST) goes low.

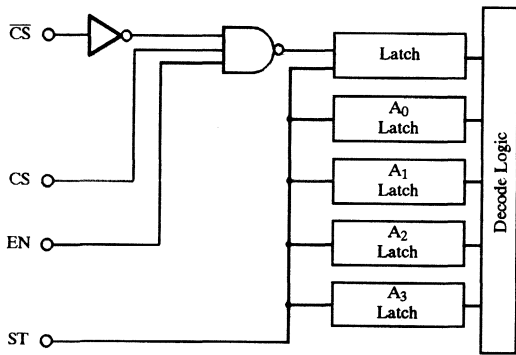


Figure 11.  $\overline{CS}$ , CS, EN, ST Control Logic

Break-before-make switching prevents momentary shorting when changing from one input to another.

The devices feature a two-level switch arrangement whereby two banks of eight switches (first level) are connected via two series switches (second level) to a common DRAIN output.

In order to improve crosstalk all sixteen first level switches are configured as "T" switches (see Figure 12).

With this method  $SW_2$  operates out of phase with  $SW_1$  and  $SW_3$ . In the on condition  $SW_1$  and  $SW_3$  are closed with  $SW_2$  open whereas in the off condition  $SW_1$  and  $SW_3$  are open and  $SW_2$  closed. In the off condition the input to  $SW_3$  is effectively the isolation leakage of  $SW_1$  working into the on-resistance of  $SW_2$  (typically 200  $\Omega$ ).

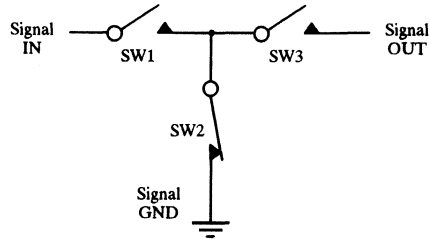


Figure 12. "T" Switch Arrangement

The two second level series switches further improve crosstalk and help to minimize output capacitance.

The DIS output can be used to signal external circuitry. DIS is a high impedance to GND when no channel is selected and a low impedance to GND when any one channel is selected.

The DG535/536 have extensive applications where any high frequency video or digital signals are switched or routed. Exceptional crosstalk and bandwidth performance is achieved by using n-channel DMOS FETs for the "T" and series switches.

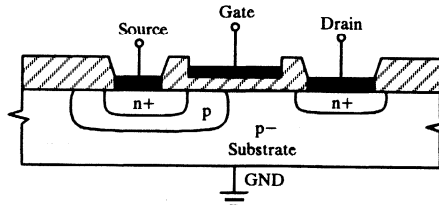


Figure 13. Cross-Section of a Single DMOS Switch

It can clearly be seen from Figure 13 that there exists a PN junction between the substrate and the drain/source terminals.

Should a signal which is negative with respect to the substrate (GND pin) be connected to a source or drain terminal, then the PN junction will become forward biased and current will flow between the signal source and GND. This effective shorting of the signal source to GND will not necessarily cause any damage to the device, provided that the total current flowing is less than the maximum rating, (i.e., 20 mA).

## Detailed Description (Cont'd)

Since no PN junctions exist between the signal path and V+, positive overvoltages are not a problem, unless the breakdown voltage of the DMOS drain terminal (see Figure 13) (+18 V) is exceeded. Positive overvoltage conditions must not exceed +18 V with respect to the GND pin. If this condition is possible (e.g. transients in the signal), then a diode or Zener clamp may be used to prevent breakdown.

The overvoltage conditions described may exist if the supplies are collapsed while a signal is present on the inputs. If this condition is unavoidable, then the necessary steps outlined above should be taken to protect the device

### DC Biasing

To avoid negative overvoltage conditions and subsequent distortion of ac analog signals, dc biasing may be necessary. Biasing is not required, however, in applications where signals are always positive with respect to the GND or substrate connection, or in applications involving multiplexing of low level (up to  $\pm 200$  mV) signals, where forward biasing of the PN substrate-source/drain terminals would not occur.

Biasing can be accomplished in a number of ways, the simplest of which is a resistive potential divider and a few dc blocking capacitors as shown in Figure 14.

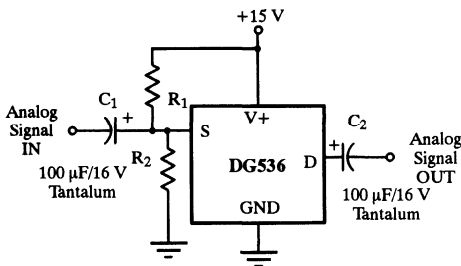


Figure 14. Simple Bias Circuit

$R_1$  and  $R_2$  are chosen to suit the appropriate biasing requirements. For video applications, approximately 3 V of bias is required for optimal differential gain and phase

performance. Capacitor  $C_1$  blocks the dc bias voltage from being coupled back to the analog signal source and  $C_2$  blocks the dc bias from the output signal. Both  $C_1$  and  $C_2$  should be tantalum or ceramic disc type capacitors in order to operate efficiently at high frequencies.

Active bias circuits are recommended if rapid switching time between channels is required.

An alternative method is to offset the supply voltages (see Figure 15).

Decoupling would have to be applied to the negative supply to ensure that the substrate is well referenced to signal ground. Again the capacitors should be of a type offering good high frequency characteristics.

Level shifting of the logic signals may be necessary using this offset supply arrangement.

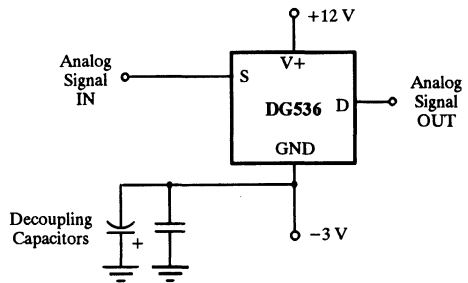


Figure 15. DG536 with Offset Supply

TTL to CMOS level shifting is easily obtained by using a MC14504B.

### Circuit Layout

Good circuit board layout and extensive shielding is essential for optimizing the high frequency performance of the DG536. Stray capacitances on the PC board and/or connecting leads will considerably degrade the ac performance. Hence, signal paths must be kept as short as practically possible, with extensive ground planes separating signal tracks.

## 8 × 4 Wideband Video Crosspoint Array

### Features

- Routes Any Input to Any Output
- Wide Bandwidth: 300 MHz
- Low Crosstalk: -85 dB @ 5 MHz
- Double Buffered TTL-Compatible Latches with Readback
- Low  $r_{DS(on)}$ : 45  $\Omega$
- Optional Negative Supply

### Benefits

- Reduced Board Space
- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- High Reliability

### Applications

- Wideband Signal Routing and Multiplexing
- High-End Video Systems
- NTSC, PAL, SECAM Switchers
- Digital Video Routing
- ATE Systems

### Description

The DG884 contains a matrix of 32 T-switches configured in an 8 × 4 crosspoint array. Any of the IN/OUT pins may be used as an input or output. Any of the IN pins may be switched to any or simultaneously to all OUT pins.

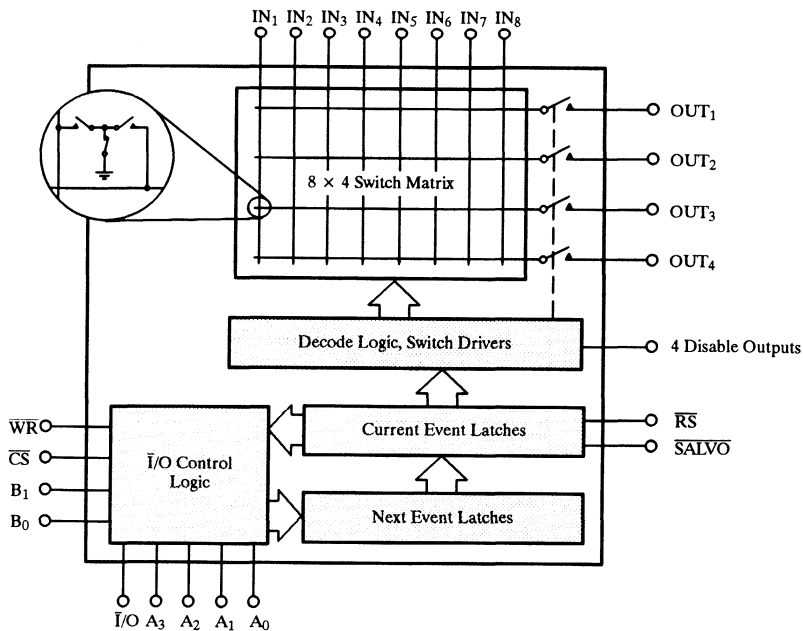
Control data is loaded individually into four Next Event latches. When all Next Event latches have been programmed, data is transferred into the Current Event latches via a SALVO command. Current Event latch data readback is available to poll array status.

The DG884 is built on a proprietary D/CMOS process that combines low capacitance switching DMOS FETs with low power CMOS control logic and drivers. The ground lines between adjacent signal input pins help to reduce crosstalk. The low on-resistance and low on-capacitance of the DG884 make it ideal for video and wideband signal routing.

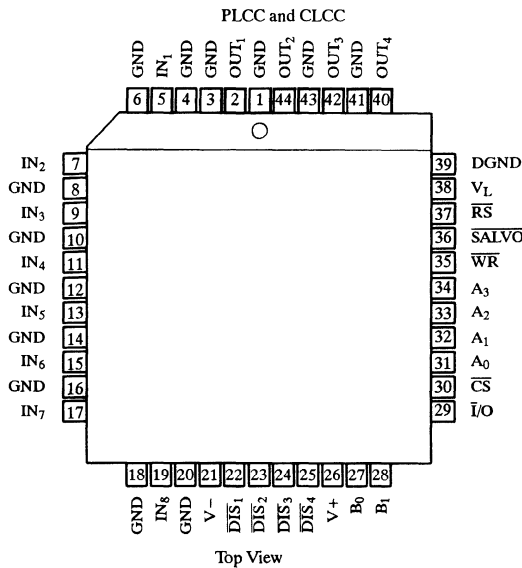
Output disable capabilities make it possible to parallel multiple DG884s to form larger switch arrays. DIS outputs provide control signals used to place external buffers in a power saving mode.

For additional information please refer to AN504.

### Functional Block Diagram



## Pin Configuration



### Ordering Information

Temp Range	Package	Part Number
-40 to 85°C	44-Pin PLCC	DG884DN
-55 to 125°C	44-Pin CLCC	DG884AM/883

## Truth Tables

RS	I/O	CS	WR	SALVO	Actions
1	0	1	1	1	No change to Next Event latches
1	0	0	1	1	Next Event latches loaded as defined in table below
1	0	0	0	1	Next Event latches are transparent.
1	0	0	1	1	Next Event data latched-in
1	0	X	1	1	Data in all Next Event latches is simultaneously loaded into the Current Event latches, i.e., all new crosspoint addresses change simultaneously when SALVO goes low.
1	0	0	X	0	Current Event latches are transparent
1	0	X	1	1	Current Event data latched-in
1	0	0	0	0	Both next and Current Event latches are transparent
1	1	1	1	1	A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> – High impedance
1	1	0	1	1	A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> become outputs and reflect the contents of the Current Event latches. B <sub>0</sub> , B <sub>1</sub> determine which Current Event latches are being read
0	X	X	1	1	All crosspoints opened (but data in Next Event latches is preserved)

All other states are not recommended.



**Truth Tables (Cont'd)**

$\overline{WR}$	B <sub>1</sub>	B <sub>0</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Next Event Latches	
0	0	0	1	0	0	0	IN <sub>1</sub> to OUT <sub>1</sub> Loaded	
				0	0	1	IN <sub>2</sub> to OUT <sub>1</sub> Loaded	
				0	1	0	IN <sub>3</sub> to OUT <sub>1</sub> Loaded	
				0	1	1	IN <sub>4</sub> to OUT <sub>1</sub> Loaded	
				1	0	0	IN <sub>5</sub> to OUT <sub>1</sub> Loaded	
				1	0	1	IN <sub>6</sub> to OUT <sub>1</sub> Loaded	
				1	1	0	IN <sub>7</sub> to OUT <sub>1</sub> Loaded	
				1	1	1	IN <sub>8</sub> to OUT <sub>1</sub> Loaded	
	0	X	X	X	Turn Off OUT <sub>1</sub> Loaded			
	0	1	1	1	0	0	0	IN <sub>1</sub> to OUT <sub>2</sub> Loaded
					0	0	1	IN <sub>2</sub> to OUT <sub>2</sub> Loaded
					0	1	0	IN <sub>3</sub> to OUT <sub>2</sub> Loaded
0					1	1	IN <sub>4</sub> to OUT <sub>2</sub> Loaded	
1					0	0	IN <sub>5</sub> to OUT <sub>2</sub> Loaded	
1					0	1	IN <sub>6</sub> to OUT <sub>2</sub> Loaded	
1					1	0	IN <sub>7</sub> to OUT <sub>2</sub> Loaded	
1					1	1	IN <sub>8</sub> to OUT <sub>2</sub> Loaded	
0	X	X	X	Turn Off OUT <sub>2</sub> Loaded				
0	1	0	1	0	0	0	IN <sub>1</sub> to OUT <sub>3</sub> Loaded	
				0	0	1	IN <sub>2</sub> to OUT <sub>3</sub> Loaded	
				0	1	0	IN <sub>3</sub> to OUT <sub>3</sub> Loaded	
				0	1	1	IN <sub>4</sub> to OUT <sub>3</sub> Loaded	
				1	0	0	IN <sub>5</sub> to OUT <sub>3</sub> Loaded	
				1	0	1	IN <sub>6</sub> to OUT <sub>3</sub> Loaded	
				1	1	0	IN <sub>7</sub> to OUT <sub>3</sub> Loaded	
				1	1	1	IN <sub>8</sub> to OUT <sub>3</sub> Loaded	
0	X	X	X	Turn Off OUT <sub>3</sub> Loaded				
0	1	1	1	0	0	0	IN <sub>1</sub> to OUT <sub>4</sub> Loaded	
				0	0	1	IN <sub>2</sub> to OUT <sub>4</sub> Loaded	
				0	1	0	IN <sub>3</sub> to OUT <sub>4</sub> Loaded	
				0	1	1	IN <sub>4</sub> to OUT <sub>4</sub> Loaded	
				1	0	0	IN <sub>5</sub> to OUT <sub>4</sub> Loaded	
				1	0	1	IN <sub>6</sub> to OUT <sub>4</sub> Loaded	
				1	1	0	IN <sub>7</sub> to OUT <sub>4</sub> Loaded	
				1	1	1	IN <sub>8</sub> to OUT <sub>4</sub> Loaded	
0	X	X	X	Turn Off OUT <sub>4</sub> Loaded				

Note: When  $\overline{WR} = 0$  Next Event latches are transparent. Each crosspoint is addressed individually, e.g., to connect IN<sub>1</sub> to OUT<sub>1</sub> thru OUT<sub>4</sub> requires A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub> = 0 to be latched with each combination of B<sub>0</sub>, B<sub>1</sub>. When  $\overline{RS} = 0$ , all four  $\overline{DIS}$  outputs pull low simultaneously.

**Absolute Maximum Ratings**

V <sub>+</sub> to GND	-0.3 V to 21 V
V <sub>+</sub> to V <sub>-</sub>	-0.3 V to 21 V
V <sub>-</sub> to GND	-10 V to 0.3 V
V <sub>L</sub> to GND	0 V to (V <sub>L</sub> ) + 0.3 V
Digital Inputs	(V <sub>-</sub> ) - 0.3 V to (V <sub>L</sub> ) + 0.3 V or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub>	(V <sub>-</sub> ) - 0.3 V to (V <sub>-</sub> ) + 14 V or 20 mA, whichever occurs first
CURRENT (any terminal) Continuous	20 mA
CURRENT (S or D) Pulsed 1 ms 10% duty	40 mA

Storage Temperature	(A Suffix) -65 to 150°C
	(D Suffix) -65 to 125°C
Operating Temperature	(A Suffix) -55 to 125°C
	(D Suffix) -40 to 85°C
Power Dissipation (Package) <sup>a</sup>	
44-Pin Quad J Lead PLCC <sup>b</sup>	450 mW
44-Pin Quad J Lead Hermetic CLCC <sup>c</sup>	1200 mW

- Notes:
- All leads soldered or welded to PC board.
  - Derate 6 mW/°C above 75°C.
  - Derate 16 mW/°C above 75°C.

## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -3\text{ V}$ $V_L = 5\text{ V}, \overline{RS} = 2.0\text{ V}$ $\overline{SALVO}, \overline{CS}, \overline{WR}, I/O = 0.8\text{ V}$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$	$V_- = -5\text{ V}$	Full		-5	8	-5	8	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = 0\text{ V}$ $V_{AIH} = 2.0\text{ V}, V_{AIL} = 0.8\text{ V}$ Sequence Each Switch On	Room Full	45		90 120		90 120	$\Omega$
Resistance Match Between Channels	$\Delta r_{DS(on)}$		Room	3		9		9	
Source Off Leakage Current	$I_{S(off)}$	$V_S = 8\text{ V}, V_D = 0\text{ V}, \overline{RS} = 0.8\text{ V}$	Room Full		-20 -200	20 200	-20 -200	20 200	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_S = 0\text{ V}, V_D = 8\text{ V}, \overline{RS} = 0.8\text{ V}$	Room Full		-20 -200	20 200	-20 -200	20 200	
Total Switch On Leakage Current	$I_{D(on)}$	$V_S = V_D = 8\text{ V}$	Room Full		-20 -2000	20 2000	-20 -200	20 200	
<b>Digital Input/Output</b>									
Input Voltage High	$V_{AIH}$		Full		2		2		V
Input Voltage Low	$V_{AIL}$		Full			0.8		0.8	
Address Input Current	$I_{AI}$	$V_{AI} = 0\text{ V or } 2\text{ V or } 5\text{ V}$	Room Full	0.1	-1 -10	1 10	-1 -10	1 10	$\mu\text{A}$
Address Output Current	$I_{AO}$	$V_{AO} = 2.7\text{ V}$ , See Truth Table	Room	-600		-200		-200	
		$V_{AO} = 0.4\text{ V}$ , See Truth Table	Room	1500	500		500		
$\overline{DIS}$ Pin Sink Current	$I_{DIS}$		Room	1.5					mA
<b>Dynamic Characteristics</b>									
On State Input Capacitance <sup>e</sup>	$C_{S(on)}$	1 In to 1 Out, See Figure 11	Room	30				40	pF
		1 In to 4 Out, See Figure 11	Room	120				160	
Off State Input Capacitance <sup>e</sup>	$C_{S(off)}$	See Figure 11	Room	8		20		20	
Off State Output Capacitance <sup>e</sup>	$C_{D(off)}$		Room	10		20		20	
Transition Time	$t_{TRANS}$	See Figure 5	Room					300	
Break-Before-Make Interval	$t_{OPEN}$		Full			10		10	
$\overline{SALVO}, \overline{WR}$ Turn On Time	$t_{ON}$	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ 50% Control to 90% Output See Figure 3	Room Full			300 500		300	ns
$\overline{SALVO}, \overline{WR}$ Turn Off Time	$t_{OFF}$		Room Full			175 300		175	
Charge Injection	Q	See Figure 6	Room	-100					pC
Matrix Disabled Crosstalk	$X_{TALK(DIS)}$	$R_{IN} = R_L = 75\text{ }\Omega$ $f = 5\text{ MHz}$ , See Figure 10	Room	-82					dB
Adjacent Input Crosstalk	$X_{TALK(AI)}$	$R_{IN} = 10\text{ }\Omega, R_L = 10\text{ k}\Omega$ $f = 5\text{ MHz}$ , See Figure 9	Room	-85					
All Hostile Crosstalk	$X_{TALK(AH)}$	$R_{IN} = 10\text{ }\Omega, R_L = 10\text{ k}\Omega$ $f = 5\text{ MHz}$ , See Figure 8	Room	-66					
Bandwidth	BW	$R_L = 50\text{ }\Omega$ , See Figure 7	Room	300					MHz

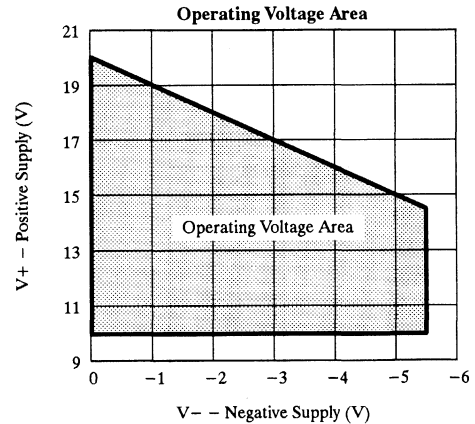
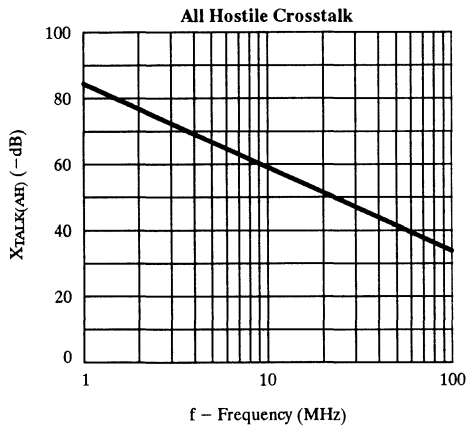
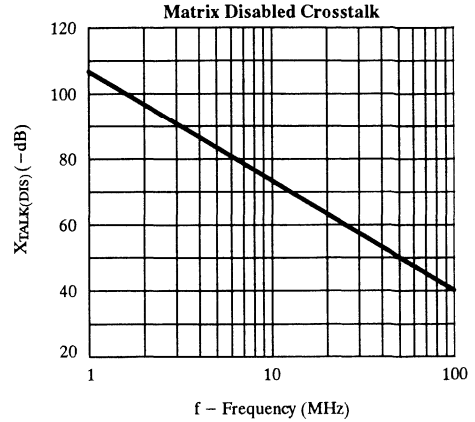
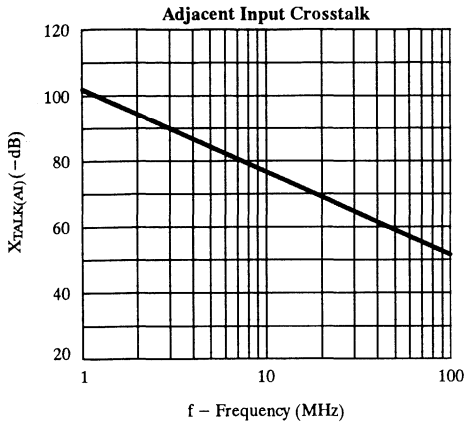
**Specifications<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -3 V V <sub>L</sub> = 5 V, RS = 2.0 V SALVO, CS, WR, I/O = 0.8 V	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Power Supplies</b>									
Positive Supply Current	I+	All Inputs At GND or 2 V RS = 2 V	Room Full	1.5		3 6		3 6	mA
Negative Supply Current	I-		Room Full	-1.5	-3 -5		-3 -5		
Digital GND Supply Current	I <sub>DG</sub>		Full	-275	-750		-750		μA
Logic Supply Current	I <sub>L</sub>	Full	200		500		500		
Functional Operating Supply Voltage Range <sup>e</sup>	V+ to V-	See Operating Voltage Range (Typical Characteristics) page 2-118	Full		13	20	13	20	V
	V- to GND		Full		-5.5	0	-5.5	0	
	V+ to GND		Full		10	20	10	20	
<b>Minimum Input Timing Requirements</b>									
Address Write Time	t <sub>AW</sub>	See Figure 1	Full	20	50		50		ns
Minimum WR Pulse Width	t <sub>WP</sub>		Full	50	100		100		
Write Address Time	t <sub>WA</sub>		Full	-10	10		10		
Chip Select Write Time	t <sub>CW</sub>		Full	50	100		100		
Write Chip Select Time	t <sub>WC</sub>		Full	25	75		75		
Minimum SALVO Pulse Width	t <sub>SP</sub>		Full	50	100		100		
SALVO Write Time	t <sub>SW</sub>		Full	-10	10		10		
Write SALVO Time	t <sub>WS</sub>		Room	20			50		
Input Output Time	t <sub>IO</sub>		Room	150	200		200		
Address Output Time	t <sub>AO</sub>		Room	150	200		200		
Chip Select Output Time	t <sub>CO</sub>		Room	150	200		200		
Chip Select Address Time	t <sub>CA</sub>		Room	60			100		
Reset to SALVO	t <sub>RS</sub>		Full		50		50		
I/O Address Input Time	t <sub>IA</sub>		Room	50					

Notes:

- a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.

## Typical Characteristics

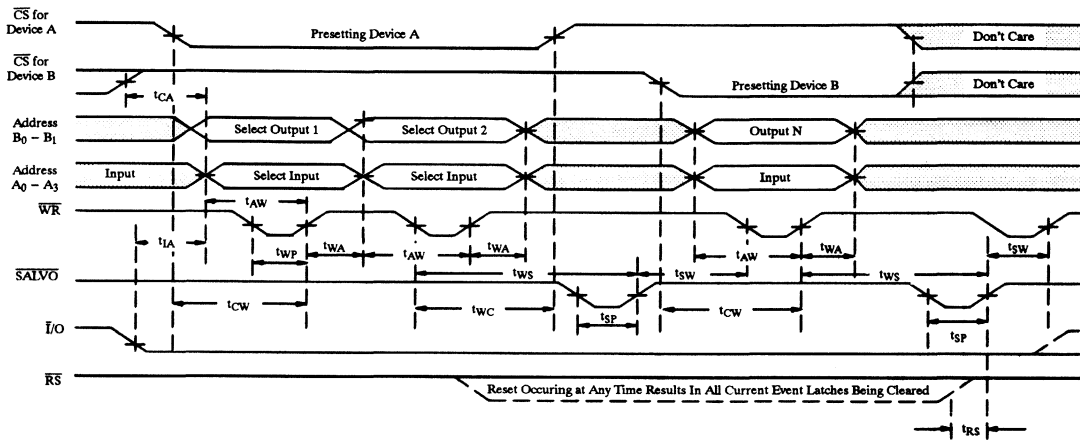


## Timing Diagrams and Parameter Definitions

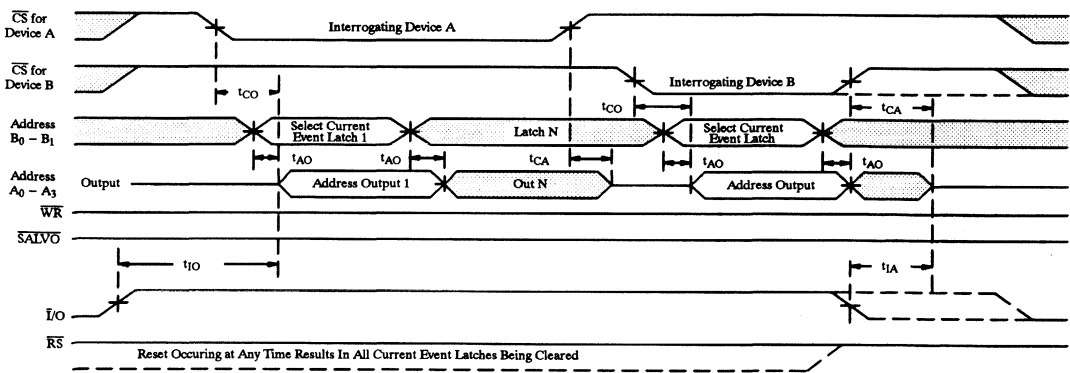
Symbol	Parameter	Description
T <sub>AW</sub>	Address to Write	Minimum time address must be valid before $\overline{WR}$ goes high
T <sub>WA</sub>	Write to Address	Minimum time address must remain valid after $\overline{WR}$ pulse goes high
T <sub>WP</sub>	$\overline{WR}$ Pulse	Minimum time of $\overline{WR}$ pulse width to write address into Next Event latches
T <sub>CW</sub>	Chip Select to $\overline{WR}$	Minimum time chip select must be valid before a $\overline{WR}$ pulse
T <sub>WC</sub>	$\overline{WR}$ to Chip Select	Minimum time chip select must remain valid after $\overline{WR}$ pulse
T <sub>SP</sub>	$\overline{SALVO}$ Pulse	Minimum time of $\overline{SALVO}$ pulse width
T <sub>WS</sub>	$\overline{WR}$ to $\overline{SALVO}$	Minimum time from $\overline{WR}$ pulse to $\overline{SALVO}$ to load new address
T <sub>SW</sub>	$\overline{SALVO}$ to $\overline{WR}$	Minimum time from $\overline{SALVO}$ pulse to $\overline{WR}$ to load current address
T <sub>IA</sub>	$\overline{I/O}$ to Address In	Minimum time $\overline{I/O}$ must be valid before address applied

**Timing Diagrams and Parameter Definitions (Cont'd)**

Symbol	Parameter	Description
$T_{RS}$	$\overline{RS}$ to $\overline{SALVO}$	Minimum time $\overline{RS}$ must be valid before $\overline{SALVO}$ pulse
$T_{IO}$	$\overline{I/O}$ to Output	Minimum time $\overline{I/O}$ must be valid before address output valid
$T_{AO}$	Address to Output	Minimum time address $B_X$ must be valid until address $A_X$ output valid
$T_{CO}$	$\overline{CS}$ to Output	Minimum time $\overline{CS}$ must be valid until $A_X$ output is valid
$T_{CA}$	$\overline{CS}$ to Address In	Minimum time $\overline{CS}$ must be valid before address applied if $\overline{I/O}$ is high



**Figure 1. Input Timing Requirements**



**Figure 2. Output Timing Requirements**

## Test Circuits

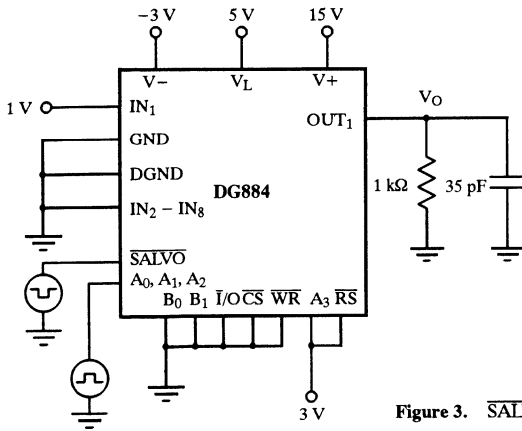


Figure 3.  $\overline{\text{SALVO}}$  Turn On/Off Time

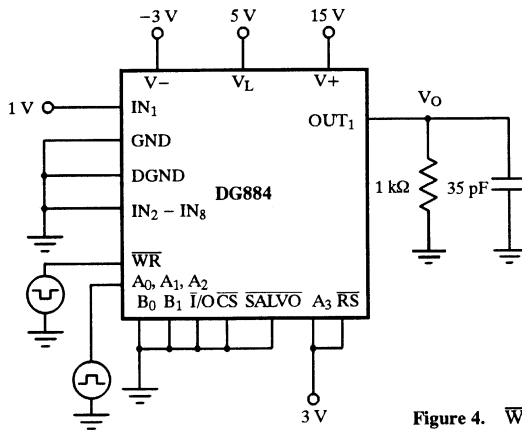
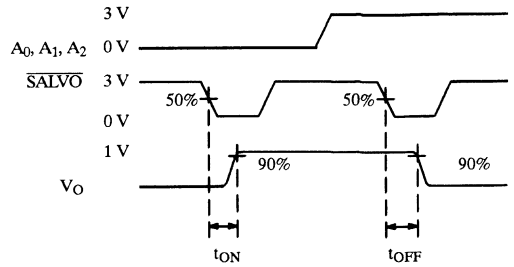


Figure 4.  $\overline{\text{WR}}$  Turn On/Off Time

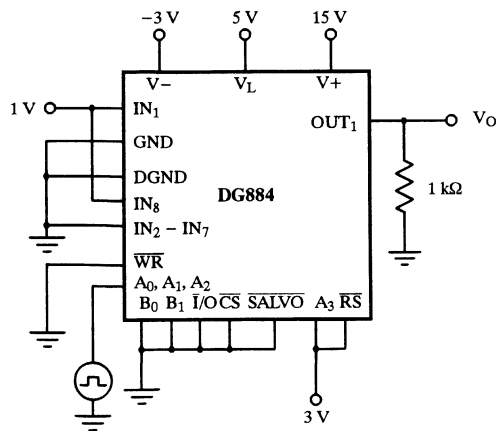
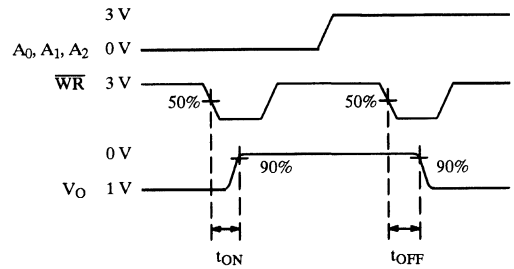
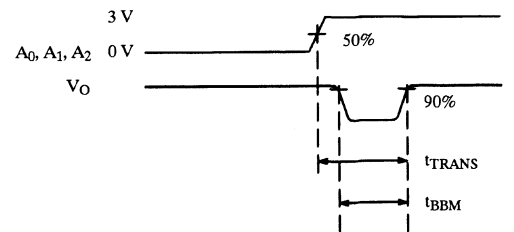
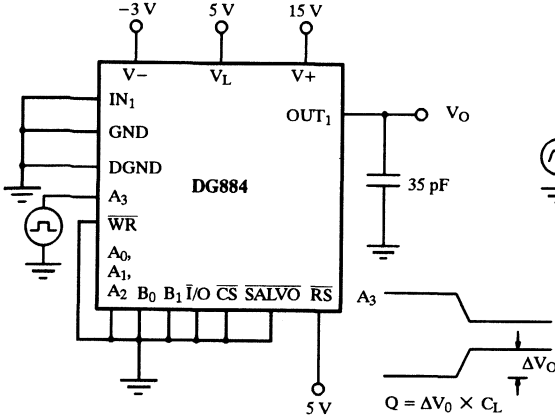


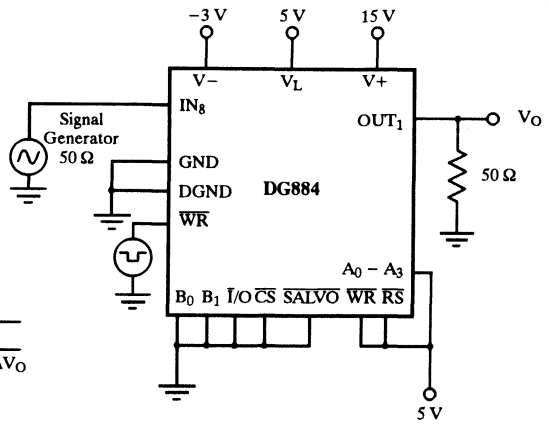
Figure 5. Transition Time and Break-Before-Make Interval



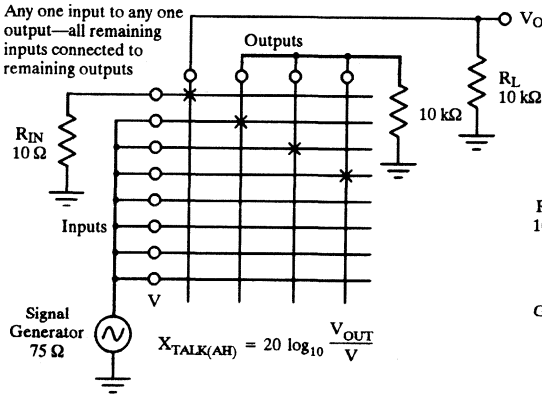
**Test Circuits**



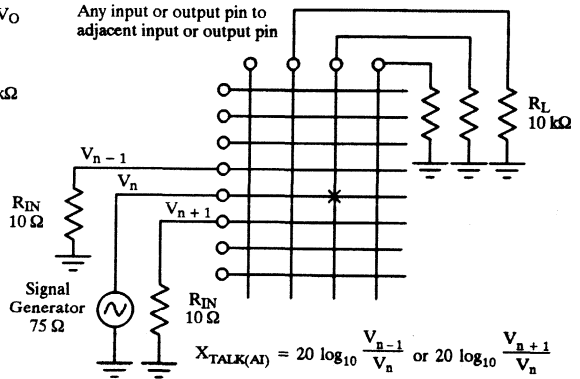
**Figure 6.** Charge Injection



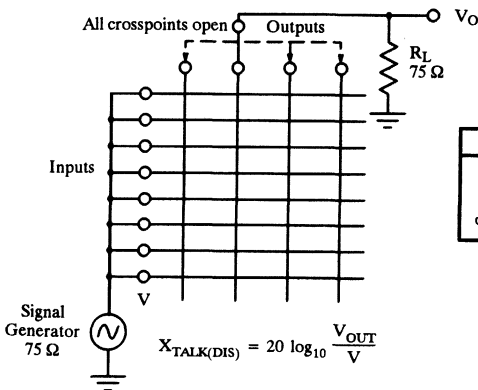
**Figure 7.** -3 dB Bandwidth



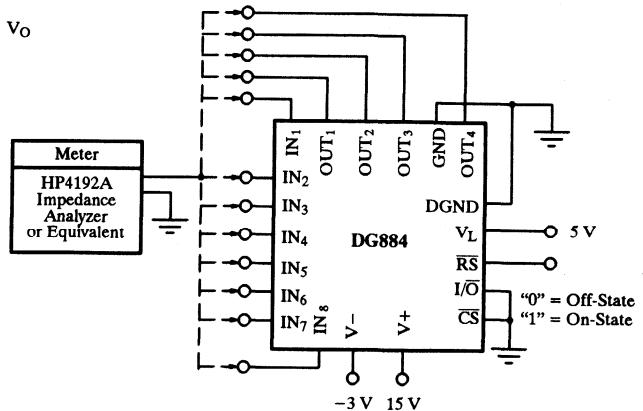
**Figure 8.** All Hostile Crosstalk



**Figure 9.** Adjacent Input Crosstalk



**Figure 10.** Matrix Disabled Crosstalk



**Figure 11.** On-State and Off-State Capacitances

## Pin Description

Pin	Symbol	Description
1, 3, 4, 6, 8, 10, 12, 14, 16, 18, 20, 41, 43	GND	Analog Signal Ground
39	DGND	Digital Ground
26	V+	Positive Supply Voltage
21	V-	Negative Supply Voltage
38	V <sub>L</sub>	Logic Supply Voltage—generally 5 V
5, 7, 9, 11, 13, 15, 17, 19	IN <sub>1</sub> to IN <sub>8</sub>	8 Analog Input Channels
2, 40, 42, 44	OUT <sub>1</sub> to OUT <sub>4</sub>	4 Analog Output Channels
29	I/O	Determines whether data is being written into the Next Event latches or read from the Current Event latches
30	CS	Chip Select—a logic input
31, 32, 22, 24	A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub>	IN Address—logic inputs or outputs as defined by I/O pin, select one of eight IN channels
27, 28	B <sub>0</sub> , B <sub>1</sub>	OUT Address—logic inputs, select one of four OUT channels
35	WR	Write command that latches A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> into the Next Event latches
36	SALVO	Master write command, that in one action, transfers all the data from Next Event latches into Current Event latches
37	RS	Reset—a low will clear the Current Event latches
22, 23, 24, 25	DIS <sub>1</sub> to DIS <sub>4</sub>	Open drain disable outputs—these outputs pull low when the corresponding OUT channel is off

## Device Description

The DG884 is the world's first monolithic wideband crosspoint array that operates from dc to >100 MHz. The DG884 offers the ability to route any one of eight input signals to any one of four OUT pins. Any input can be routed to one, two, three or four OUTs simultaneously with no risk of shorting inputs together (guaranteed by design).

Each crosspoint is configured as a "T" switch in which DMOS FETs are used due to their excellent low resistance and low capacitance characteristics. Each OUT line has a series switch that minimizes capacitive loading when the OUT is off.

### Interfacing

The DG884 was designed to allow complex matrices to be developed while maintaining a simple control interface. The status of the I/O pin determines whether the DG884 is being written to or read from (see Figures 1 and 2).

In order to WRITE to an individual latch, CS and I/O need to be low, while RS, WR and SALVO must be high. The IN to OUT path is selected by using address A<sub>0</sub> through A<sub>3</sub> to define the IN line and address B<sub>0</sub> and B<sub>1</sub> to define the OUT line. That is, The IN defined by A<sub>0</sub> through A<sub>3</sub> is electrically

connected to the OUT defined by B<sub>0</sub>, B<sub>1</sub>. This chosen path is loaded into the Next Event latches when WR goes low and returns high again. This operation is repeated up to three more times if other crosspoint connections need to be changed.

Upon completing all crosspoint connections that are to be changed in a single device, other DG884s can be similarly preset by taking the CS pin low on the appropriate device. When all DG884s are preset, the Current Event latches are simultaneously changed by a single SALVO command applied to all devices. In this manner the crosspoint configuration of any number of devices can be simultaneously updated.

### DIS Outputs

Four open drain disable OUTs are provided to control external line drivers or to provide visual or electrical signaling. For example, any or all of the DIS OUTs can directly interface with a Siliconix Si582 Video Amplifier to place it into a high impedance, low-power standby mode when the corresponding OUT is not being used. (See Figure 15). The DIS outputs are low and sink to V- when corresponding OUT is open or RS is low.



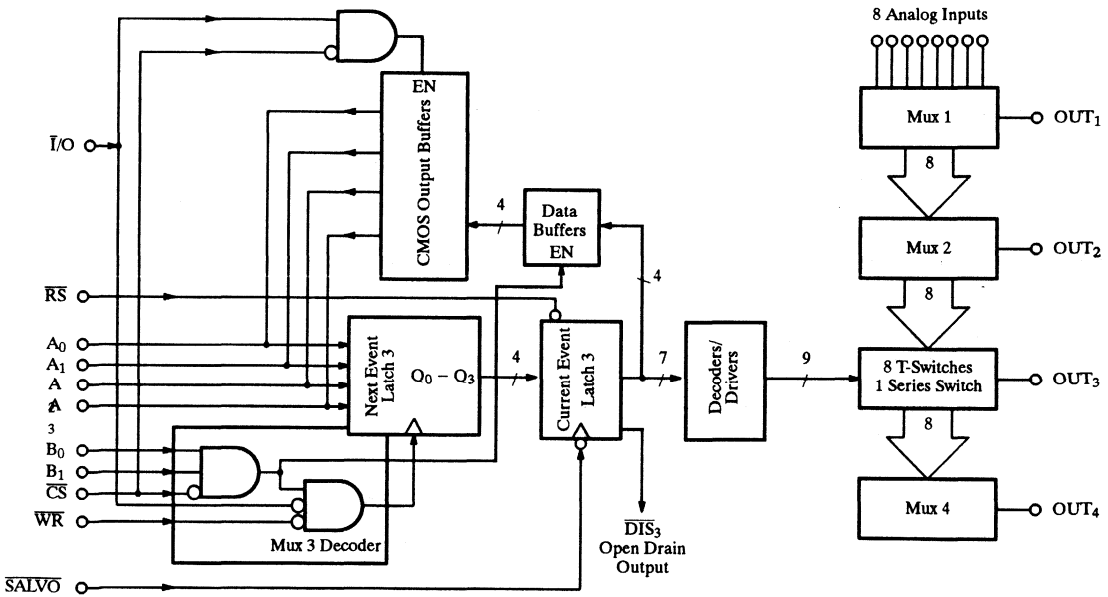
**Device Description (Cont'd)**

**Reset**

The reset function ( $\overline{RS}$ ) allows the resetting of all crosspoints to a known state (open). At power up, the reset facility may be used to guarantee that all switches are open. It should be noted that  $\overline{RS}$  clears the Current Event latches, but the Next Event latches remain unchanged. This useful facility allows the user to return the matrix to its previous state (prior to reset) by simply applying the SALVO command. Alternatively, the user can reprogram the Next Event latches, and then apply the SALVO command to reconfigure the matrix to a new state.

**Readback**

The I/O facility enables the user to write data to the Next Event latches or to read the contents of the Current Event latches. This feature permits the central controller to periodically monitor the state of the matrix. If a power loss to the controller occurs, the readback feature helps the matrix to recover rapidly. It also offers a means to perform PC board diagnostics both in production and in system operation.



One of Four Blocks of Logic/Latches Shown

**Figure 12. Control Circuitry**

## Applications

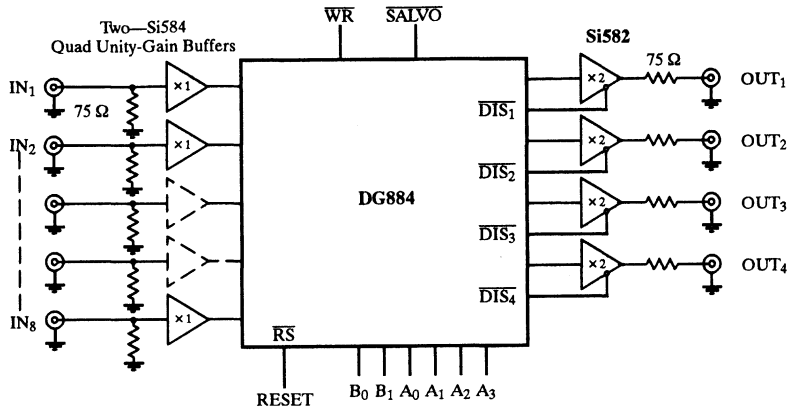


Figure 13. Fully Buffered 8 × 4 Crosspoint

### Power Supplies and Decoupling

A useful feature of the DG884 is its power supply flexibility. It can be operated from dual supplies, or a single positive supply ( $V^-$  connected to 0 V) if required. Allowable operating voltage ranges are shown in Operating Voltage Range (Typical Characteristics) graph, page 2-118.

Note that the analog signal must not go below  $V^-$  by more than 0.3 V (see absolute maximum ratings). However, the addition of a  $V^-$  pin has a number of advantages:

- 1) It allows flexibility in analog signal handling, i.e. with  $V^- = -5$  V and  $V^+ = 15$  V, up to  $\pm 5$  V ac signals can be accepted.
- 2) The value of on-capacitance ( $C_{S(on)}$ ) may be reduced by increasing the value of  $V^-$ . It is useful to note that optimum video differential phase and gain occur when  $V^-$  is -3 V. Note that  $V^+$  has no effect on  $C_{S(on)}$ .
- 3)  $V^-$  eliminates the need to bias an ac analog signal using potential dividers and large decoupling capacitors.

It is established RF design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG884 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

#### Rules:

- 1) Decoupling capacitors should be incorporated on all power supply pins ( $V^+$ ,  $V^-$ ,  $V_L$ ).

- 2) They should be mounted as close as possible to the device pins.
- 3) Capacitors should have good high frequency characteristics—tantalum bead and/or monolithic ceramic disc types are suitable.

Recommended decoupling capacitors are 1- to 10- $\mu$ F tantalum bead, in parallel with 100-nF monolithic ceramic.

- 4) Additional high frequency protection may be provided by 51- $\Omega$  carbon film resistors connected in series with the power supply pins (see Figure 14).

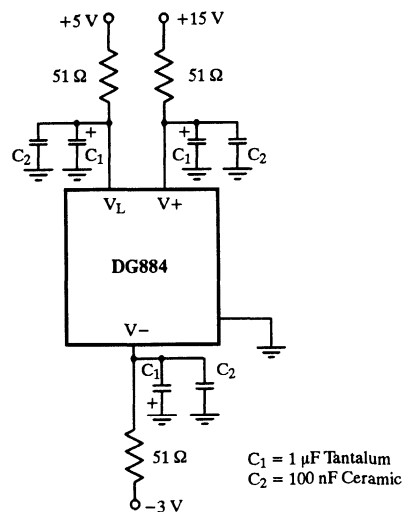


Figure 14. DG884 Power Supply Decoupling

**Applications (Cont'd)**

The  $V_L$  pin permits interface to various logic types. The device is primarily designed to be TTL or CMOS logic compatible with +5 V applied to  $V_L$ . The actual logic threshold can be raised simply by increasing  $V_L$ .

A typical switching threshold versus  $V_L$  is shown in Figure 15.

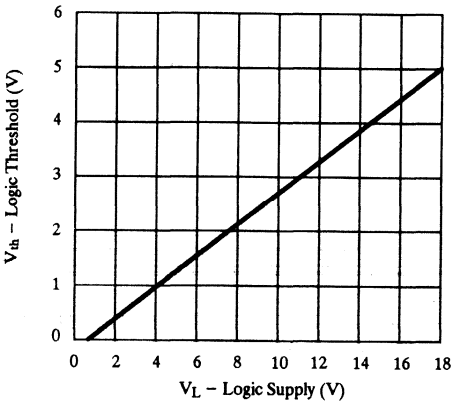


Figure 15. Switching Threshold Voltage vs.  $V_L$

These devices feature an address readback facility whereby the last address written to the device may be read by the

system. This allows improved status monitoring and hand shaking without additional external components.

When the  $\bar{I/O}$  assigns the address output condition, the  $A_x$  address pins can sink or source current for logic low and high, respectively. Note that  $V_L$  is the logic high output condition. This point must be respected if  $V_L$  is varied for input logic threshold shifting.

Note: Even though these devices are designed to be latchup resistant,  $V_L$  must not exceed  $V+$  by more than 0.3 V in operation or during power supply on/off sequencing.

**Layout**

The PLCC package pinout is optimized so that large crosspoint arrays can be easily implemented with a minimum number of PCB layers (see Figure 16). Crosstalk is minimized and off-isolation is optimized by having ground pins located adjacent to each input and output signal pins. Optimum off-isolation and low crosstalk performance can only be achieved by the proper use of RF layout techniques: avoid sockets, use ground planes, avoid ground loops, bypass the power supplies with high frequency type capacitors (low ESR, low ESL), use striplines to maintain transmission line impedance matching.

For additional information please refer to Application Note AN504.

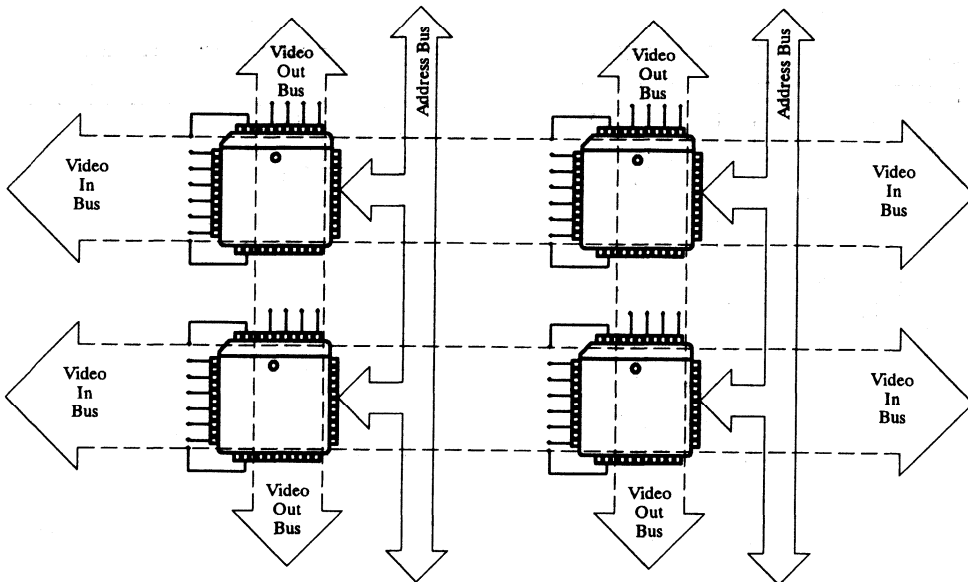


Figure 16. 16 x 8 Expandable Crosspoint Matrix Using DG884

## Component Video Selector

### Features

- Wide Bandwidth: 200 MHz
- Very Low Crosstalk: -70 dB at 5 MHz
- CMOS Compatible
- I<sup>2</sup>C Bus Compatible
- Fast Switching—t<sub>ON</sub>: <200 ns
- Low r<sub>DS(on)</sub>: 44 Ω
- Single Supply Capability

### Benefits

- Low Insertion Loss
- Improved System Performance
- Reduced Power Consumption
- Easily Interfaced
- Future System Expansion via I<sup>2</sup>C Bus

### Applications

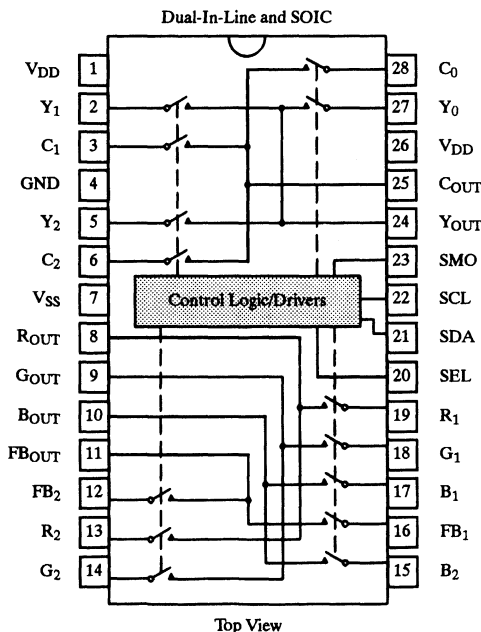
- Component Video Switching: RGB + SYNC, S-VHS, Y-C, etc.
- Audio/Video Routing
- Digital TV
- ATE
- I<sup>2</sup>C Bus Audio/Video Systems
- SCART Video Switching

### Description

The DG894 is a monolithic video selector designed for switching a variety of component video signals. The low on-resistance and low capacitance of the DG894 make it ideal for video/audio signal routing. Switch control can be through direct CMOS addressing or through the two-wire I<sup>2</sup>C bus.

The DG894 is built on the Siliconix proprietary D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. Low-capacitance DMOS FETs are used to achieve high levels of off isolation at low cost.

### Functional Block Diagram and Pin Configuration



Truth Table

SMD	SEL	SDA	SCL	Function/Switch On
0	0	I <sup>2</sup> C Bus Operation, Address A <sub>0</sub> = "1"		
0	1	I <sup>2</sup> C Bus Operation, Address A <sub>0</sub> = "0"		
1	0	0	0	All switches off
1	0	0	1	Y <sub>0</sub> , C <sub>0</sub>
1	0	1	0	Y <sub>1</sub> , C <sub>1</sub>
1	0	1	1	Y <sub>2</sub> , C <sub>2</sub>
1	1	0	0	R <sub>1</sub> , G <sub>1</sub> , B <sub>1</sub> , F <sub>1</sub>
1	1	0	1	R <sub>2</sub> , G <sub>2</sub> , B <sub>2</sub> , F <sub>2</sub>
1	1	1	0	R <sub>1</sub> , G <sub>1</sub> , B <sub>1</sub> , F <sub>1</sub> , Y <sub>1</sub> , C <sub>1</sub>
1	1	1	1	R <sub>2</sub> , G <sub>2</sub> , B <sub>2</sub> , F <sub>2</sub> , Y <sub>2</sub> , C <sub>2</sub>

Ordering Information

Temp Range	Package	Part Number
-40 to 85°C	28-Pin Plastic DIP	DG894DJ
	28-Pin Wide Body SOIC	DG894DW

**Absolute Maximum Ratings**

V+ to GND ..... -0.3 V to 19 V  
 V+ to V- ..... -0.3 V to 19 V  
 V- to GND ..... -10 V to 0.3 V  
 Digital Inputs ..... GND -0.3 V to (V+) +0.3 V  
 or 20 mA, whichever occurs first  
 Signal Inputs ..... V<sub>SS</sub> -0.3 V to 8 V  
 or 20 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 20 mA  
 Current (Any Terminal) Pulsed 1 ms, 10% Duty Cycle Max . 40 mA  
 Storage Temperature ..... -65 to 125°C  
 Power Dissipation (Package)<sup>a</sup>  
 28-Pin Plastic DIP ..... 625 mW  
 28-Pin Wide Body SOIC ..... 450 mW  
 Notes:  
 a. All leads welded or soldered to PC board.

**Specifications**

Parameter	Symbol	Test Conditions Unless Otherwise Specified  V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -5 V V <sub>INH</sub> = 3 V, V <sub>INL</sub> = 1.5 V <sup>c</sup>	Temp <sup>a</sup>	Limits -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>	V <sub>DD</sub> = 12 V, V <sub>SS</sub> = GND	Full	0		4	V
		V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -5 V	Full	-2		2	
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = 0 V	Room		44	100	Ω
			Full		51	150	
Resistance Match Between Channels	Δr <sub>DS(on)</sub>		Room		10		
Source Off Leakage Current	I <sub>S(off)</sub>	V <sub>S</sub> = 4 V, V <sub>D</sub> = 0 V	Room	-10	-0.05	10	nA
			Full	-100		100	
Drain Off Leakage Current	I <sub>D(off)</sub>	V <sub>D</sub> = 4 V, V <sub>S</sub> = 0 V	Room	-10	-0.05	10	
			Full	-100		100	
Total Switch On Leakage Current	I <sub>D(on)</sub>	V <sub>D</sub> = V <sub>S</sub> = 4 V	Room	-10	-0.07	10	nA
			Full	-100		100	
<b>Input</b>							
Input Voltage High	V <sub>INH</sub>		Full	3	2.55		V
Input Voltage Low	V <sub>INL</sub>		Full		2.55	1.5	
Input Threshold	V <sub>th</sub>		Room		2.55		
Temp Coefficient of Input Threshold	TC <sub>th</sub>		Full		-200		μV/°C
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = GND or V <sub>DD</sub>	Room	-1	0.05	1	μA
			Full	-20		20	
Output Voltage Low	V <sub>OL</sub>	Pin 21, During Acknowledge, I <sub>OL</sub> = 3 mA	Room			0.4	V
<b>Dynamic</b>							
Input Capacitance <sup>d</sup>	C <sub>in</sub>	Pin 21, 22	Room		3	10	pF
On State Input Capacitance <sup>d</sup>	C <sub>S(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V	Room		10	15	
Off State Input Capacitance <sup>d</sup>	C <sub>S(off)</sub>	V <sub>S</sub> = 0 V	Room		4	8	
Off State Output Capacitance <sup>d</sup>	C <sub>D(off)</sub>	V <sub>D</sub> = 0 V	Room		4	8	
Bandwidth <sup>d</sup>	BW	R <sub>L</sub> = 50 Ω, See Figure 1	Room	200	500		MHz
Turn On Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF, 50% to 90% V <sub>SS</sub> = -5 V, 0 V, V <sub>S</sub> = 3 V, See Figure 1	Room			200	ns
Turn Off Time	t <sub>OFF</sub>		Room			180	
SCL Max Clock Frequency	F <sub>SCL(MAX)</sub>		Full	100			kHz
Component Crosstalk	X <sub>TALK(CO)</sub>	R <sub>IN</sub> = 10 Ω, R <sub>L</sub> = 1 kΩ f = 5 MHz, See Figure 2 and 3	Room		-85		dB
Channel Crosstalk	X <sub>TALK(CH)</sub>		Room		-85		

## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{DD} = 12\text{ V}, V_{SS} = -5\text{ V}$ $V_{INH} = 3\text{ V}, V_{INL} = 1.5\text{ V}^e$	Temp <sup>a</sup>	Limits -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Supply Voltage</b>							
Positive Supply Current	I+	All Control Inputs 0 V, 5 V	Room Full		3 4	8 10	mA
Negative Supply Current	I-		Room Full	-8 -10	-2.5 -3.0		

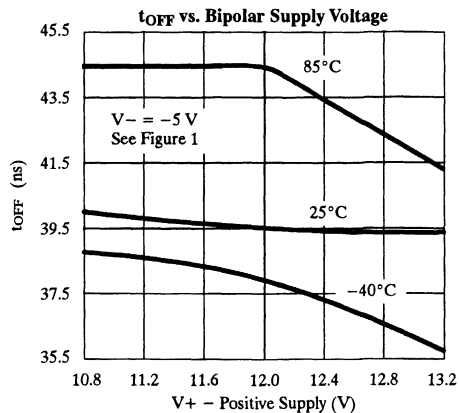
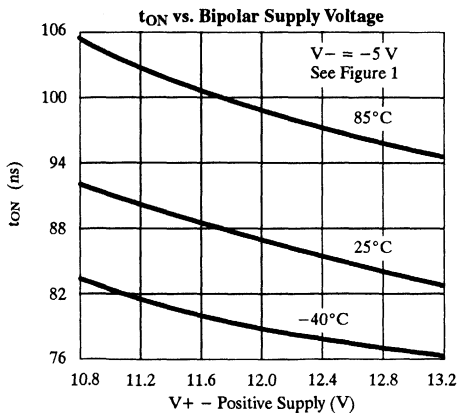
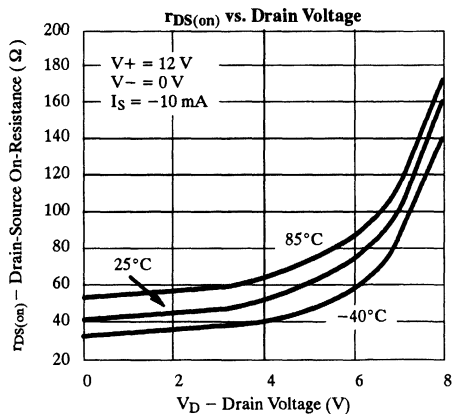
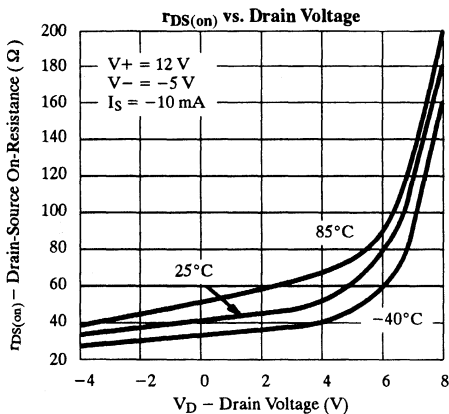
**Notes:**

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

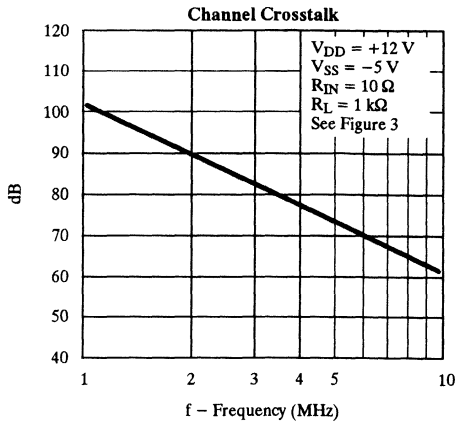
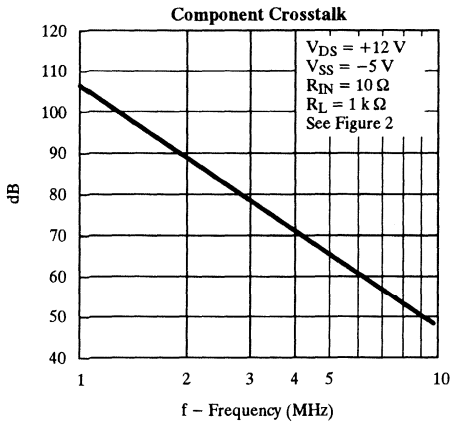
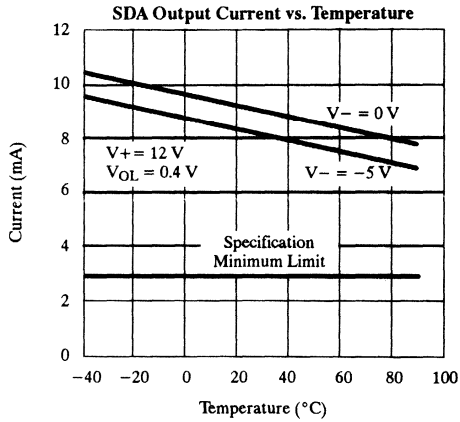
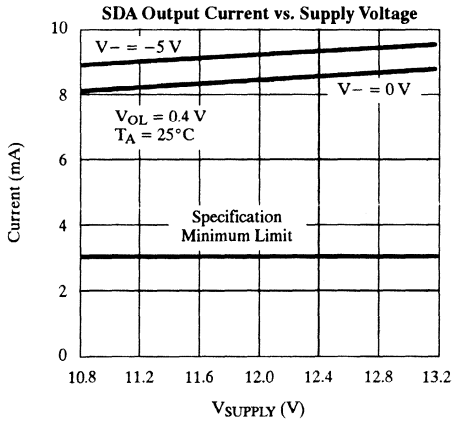
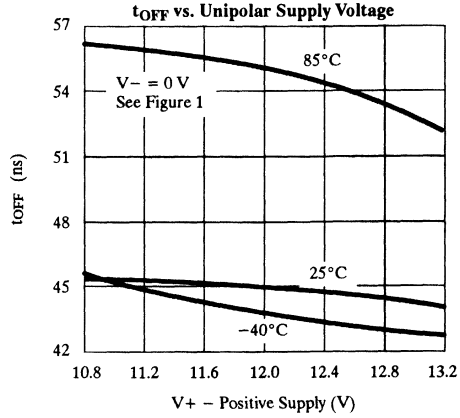
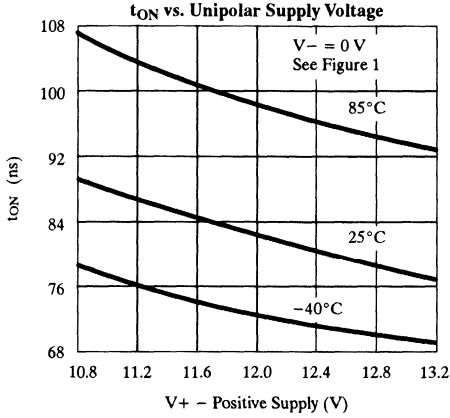


Purchase of Siliconix DG894 components conveys a license to use them in the I<sup>2</sup>C system as defined by Philips.

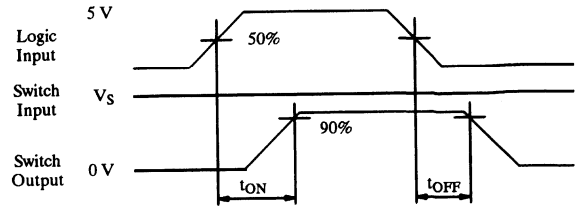
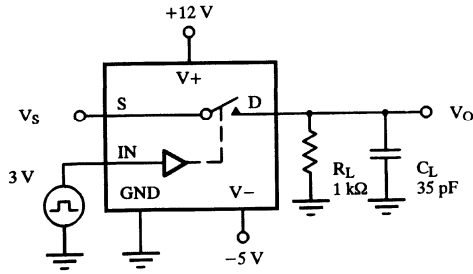
## Typical Characteristics



**Typical Characteristics (Cont'd)**



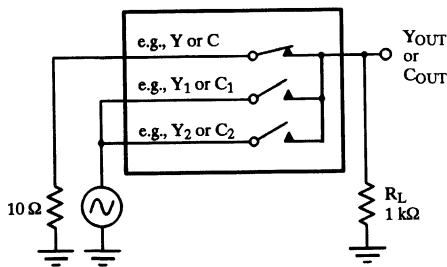
## Test Circuits



$C_L$  (includes fixture and stray capacitance)

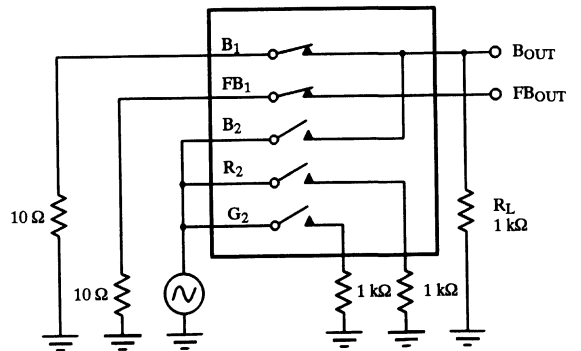
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

**Figure 1.** Switching Time



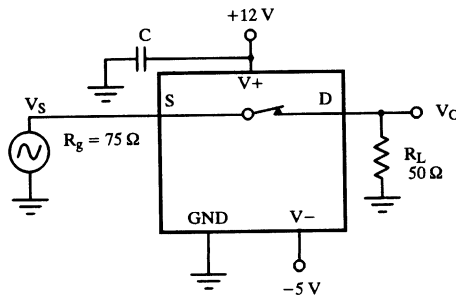
$$X_{TALK(CO)} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

**Figure 2.** Component Crosstalk



$$X_{TALK(CH)} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

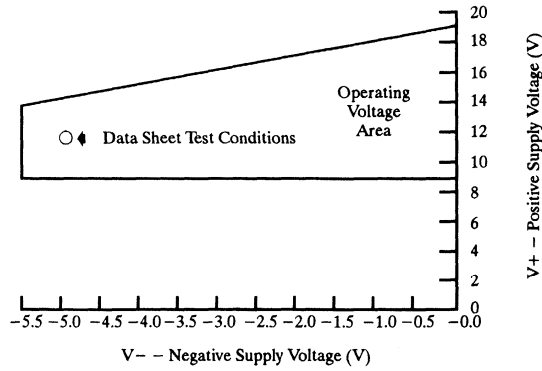
**Figure 3.** Channel Crosstalk



**Figure 4.** Bandwidth



## Operating Voltage Range



**Figure 5.**

## Pin Description

Symbol	Description
Y <sub>0</sub> , Y <sub>1</sub> , Y <sub>2</sub>	An analog channel input, typically luminance.
C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>	An analog channel input, typically chrominance.
R <sub>1</sub> , R <sub>2</sub> , G <sub>1</sub> , G <sub>2</sub> , B <sub>1</sub> , B <sub>2</sub> , FB <sub>1</sub> , FB <sub>2</sub>	An analog channel input, typically "red", "green", "blue" or "fast blanking", as appropriate.
GND	Analog and digital ground.
V <sub>DD</sub>	Positive supply voltage <sup>a</sup>
V <sub>SS</sub>	Negative supply voltage
Y <sub>OUT</sub> , C <sub>OUT</sub>	An analog channel output, typically luminance or chrominance, as appropriate
R <sub>OUT</sub> , G <sub>OUT</sub> , B <sub>OUT</sub> , FB <sub>OUT</sub>	An analog channel output, typically "red", "green", "blue" or "fast blanking", as appropriate.
SMO	A low selects serial mode (I <sup>2</sup> C) operation. A high selects CMOS operation.
SDA	Serial data line <sup>b</sup>
SCL	Serial clock line <sup>b</sup>
SEL	CMOS control line or I <sup>2</sup> C address <sup>c</sup> select line

**Notes:**

- a. Both V<sub>DD</sub> pins (Pin 1 and Pin 26) must be connected for proper operation.
- b. SDA and SCL pins become CMOS control inputs when SMO = High.
- c. The SEL pin, in I<sup>2</sup>C bus operation (i.e., with SMO low), is the least significant bit of the device address. This allows two devices to operate on the same I<sup>2</sup>C bus, yet retain independent control.

## Applications

### I<sup>2</sup>C Bus Operation—RGB Switching

Figure 6 shows an inexpensive RGB + stereo selector. The two audio channels are switched via the C, Y terminals. The Si584 quad video buffer drives four 75-Ω output lines.

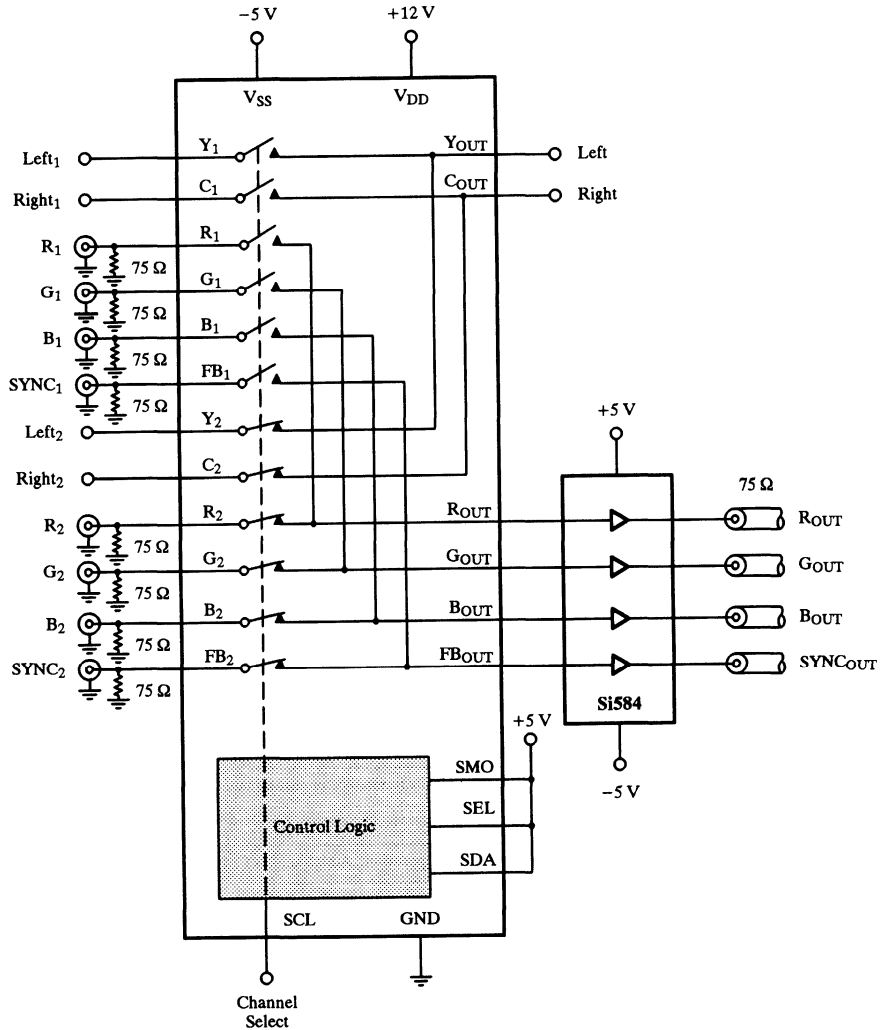


Figure 6.

**Applications (Cont'd)**

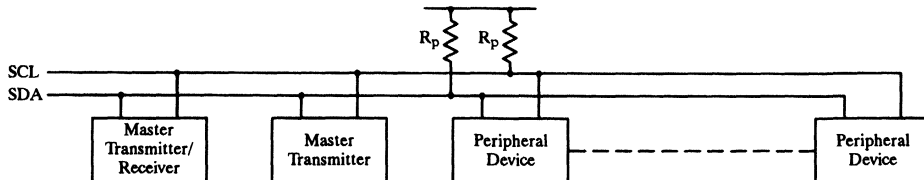


Figure 7.

**Characteristics of the I<sup>2</sup>C Bus**

The I<sup>2</sup>C Bus interface is ideally suited for communication between different ICs or modules. Its salient features are:

- Two wire bidirectional serial bus
  - Serial data (SDA) and serial clock (SCL) lines
- Multi-master system (built-in arbitration for multi-master systems)
- Devices have independent clocks
- Master and slave devices can be receivers and/or transmitters.
- Each device has a unique address.
- Maximum bus clock rate of 100 kHz.
- Any number of interfaces may be connected to the bus
  - Limited only by total capacitance of 400 pF
  - Each pin on bus limited to 10-pF capacitance
  - Input levels:
    - V<sub>IL</sub> max = 1.5 V (fixed supply operation)
    - V<sub>IH</sub> min = 3 V (fixed supply operation)
    - V<sub>IL</sub> max = 0.3 V<sub>DD</sub> (wide range supply operation)
    - V<sub>IH</sub> min = 0.7 V<sub>DD</sub> (wide range supply operation)

- total bus capacitance
- supply voltage (Figure 7).

**Data Transfer on the I<sup>2</sup>C Bus**

If the bus is not being used, both SDA and SCL lines must be left high.

Every byte put onto the SDA line should be eight bits long (MSB first), followed by an acknowledge bit, which is generated by the receiving device.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the address byte. If this is the device's own address, the device will generate an acknowledge by pulling the SDA line low during the ninth clock pulse, then accept the data in subsequent bytes until another start or stop condition is detected.

The eight bit of the address byte is the read/write bit (high = read from addressed device, low = write to the addressed device) so, for the DG894, the address is only considered valid if the R/W bit is low.

Data bytes are always acknowledged during the ninth clock pulse by the addressed device. Note that during the acknowledge period the transmitting device must leave the SDA line high.

Premature termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the DG894 will remain in the state defined by the last complete data byte transmitted.

**System Configuration**

R<sub>p</sub> value depends on:

- number of devices on bus

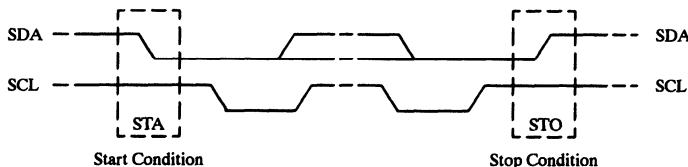


Figure 8. START and STOP Conditions

## Applications (Cont'd)

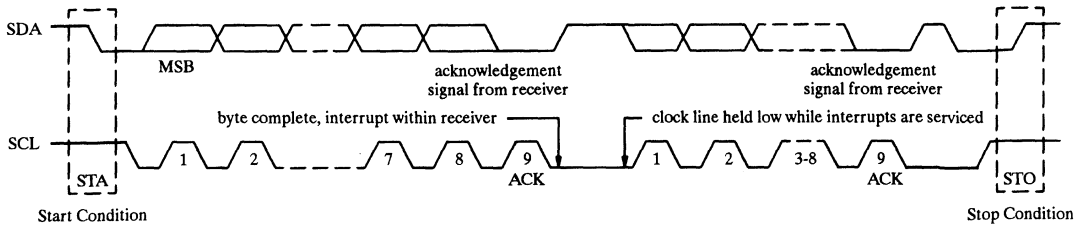


Figure 9. Data Transfer on the I<sup>2</sup>C Bus

### Timing Specifications of the I<sup>2</sup>C Bus

I<sup>2</sup>C bus load conditions for timing specifications are as follows:

4 kΩ pull-up resistors to +5 V; 200 pF capacitor to ground. All values are referred to V<sub>IH</sub> = 3 V, V<sub>IL</sub> = 1.5 V.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f <sub>scl</sub>	—	100	kHz
Bus Free Before Start	t <sub>BUF</sub>	4.7	—	μs
Start Condition Set-up Time	t <sub>SU,STA</sub>	4.7	—	
Start Condition Hold Time	t <sub>HD,STA</sub>	4	—	
SCL and SDA Low Period	t <sub>LOW</sub>	4.7	—	
SCL and SDA High Period	t <sub>HIGH</sub>	4	—	
SCL and SDA Rise Time	t <sub>r</sub>	—	1.0	
SCL and SDA Fall Time	t <sub>f</sub>	—	0.3	
Data Set-Up Time (WRITE)	t <sub>SU,DAT</sub>	0.25	—	
Data Hold Time (WRITE)	t <sub>HD,DAT</sub>	0*	—	

\* A transmitter must internally provide at least a hold time to bridge the undefined region (max 300 ns) of the falling edge of the SCL.

### I<sup>2</sup>C Bus Protocol

The DG894 is a slave receiver type of I<sup>2</sup>C interface and has four allocated addresses, two of which are user programmable through the SEL pin. Additional addresses may be obtained by a metal mask option for users requiring more than two DG894s on the same I<sup>2</sup>C bus. Contact Siliconix marketing for further information.

After the correct address has been sent, only one data byte is needed to define the switch configuration. Subsequent data put onto the bus will update the switches until a STOP condition (or another START condition) signals that the device is no longer being addressed. The switches will then remain in their last configuration as long as power is maintained to the chip.

### Power on Reset

A power on reset function is provided on the DG894 to turn all switches off following power up if the I<sup>2</sup>C mode is selected. In the CMOS control mode, the switches are selected according to the state of the control inputs.

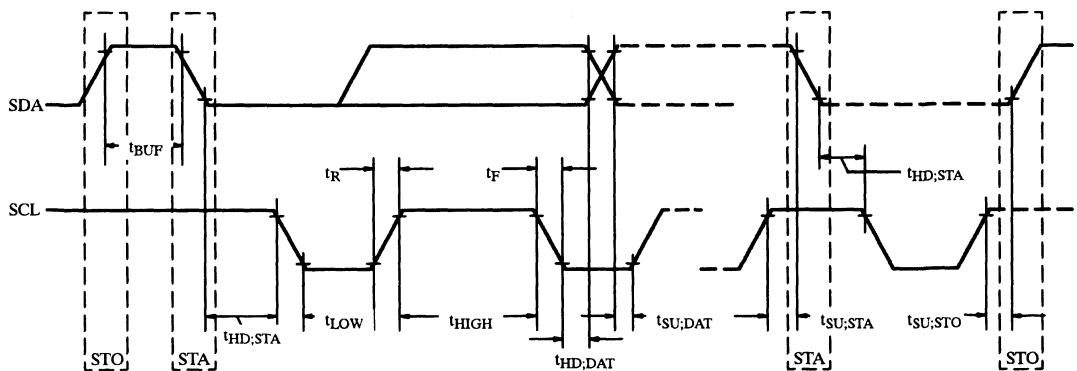


Figure 10. I<sup>2</sup>C Bus Timing Diagram

**Applications (Cont'd)**

**Minimum Bit Stream to Set Up DG894 Switches**

STA	1	1	0	1	1	A <sub>1</sub>	A <sub>0</sub>	R/W	ACK	X	X	X	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	ACK	STO
-----	---	---	---	---	---	----------------	----------------	-----	-----	---	---	---	----------------	----------------	----------------	----------------	----------------	-----	-----



- STA = START CONDITION
- A<sub>1</sub> = 0 (programmable to "1" with metal mask change)
- A<sub>0</sub> =  $\overline{\text{SEL}}$ . Address bit set by use (address is inverse of SEL logic level)
- R/W = READ/WRITE bit (must be "0", only WRITE mode allowed for DG894)
- ACK = Acknowledge bit ("0") generated by DG894
- D<sub>4</sub> = 0 --- R<sub>2</sub>, G<sub>2</sub>, B<sub>2</sub>, and FB<sub>2</sub> switches off
- D<sub>4</sub> = 1 --- R<sub>2</sub>, G<sub>2</sub>, B<sub>2</sub>, and FB<sub>2</sub> switches on
- D<sub>3</sub> = 0 --- R<sub>1</sub>, G<sub>1</sub>, B<sub>1</sub>, and FB<sub>1</sub> switches off
- D<sub>3</sub> = 1 --- R<sub>1</sub>, G<sub>1</sub>, B<sub>1</sub>, and FB<sub>1</sub> switches on
- D<sub>2</sub> = 0 --- Y<sub>2</sub>, C<sub>2</sub>, switches off
- D<sub>2</sub> = 1 --- Y<sub>2</sub>, C<sub>2</sub>, switches on
- D<sub>1</sub> = 0 --- Y<sub>1</sub>, C<sub>1</sub>, switches off
- D<sub>1</sub> = 1 --- Y<sub>1</sub>, C<sub>1</sub>, switches on
- D<sub>0</sub> = 0 --- Y<sub>0</sub> and C<sub>0</sub> switches off
- D<sub>0</sub> = 1 --- Y<sub>0</sub> and C<sub>0</sub> switches on
- STO = STOP CONDITION



<b>General Information</b>	<b>1</b>
<b>Analog Switches</b>	<b>2</b>
<b>Analog Multiplexers</b>	<b>3</b>
<b>Wideband/Video Amplifiers</b>	<b>4</b>
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<b>Worldwide Sales Offices and Distributors</b>	<b>6</b>

## About Siliconix Wideband/Video Amplifiers

The Siliconix family of wideband/video amplifiers works together to provide complete system solutions for such applications as video and data communication, signal switching and routing, and high-resolution workstation buffering. Our Si581 and Si584 unity-gain buffers, as well as the Si582 low-gain amplifier, improve linearity and transmission accuracy, while providing reduced power consumption, flat frequency response, and high color fidelity. With the Si582 amplifier at the output of a switching matrix, the Si581/Si584 buffers at the input, and our wideband multiplexers and switches (DG534A, DG535, DG536, DG538A, DG54X, DG61X, DG64X, DG884, or DG894) at the core, we now provide a complete system solution for broadband distribution and back-terminated line-driving applications.



# Video Amplifiers

Part Number	Min -3 dB Bandwidth (MHz)	Max Offset Voltage (mV)	Min Slew Rate (V/ $\mu$ s)	Max Settling Time (ns)	Package	Configuration	Page
SI581	400	8	500	2	J, Y	Unity Gain Video Buffer	3-1
SI582	150	5	430	4.5	J, Y	Video Amplifier with Disable	3-8
SI584	135	5	200	6	J, Y	Quad Video Buffer	3-16

J = Plastic DIP    Y = SOIC



## Unity-Gain Video Buffer

### Features

- -3 dB-Bandwidth: 730 MHz
- Low Differential Gain: 0.1%
- Low Differential Phase: 0.01°
- Low Power— $P_D$ : 150 mW
- Fast Settling: 0.2% in 5 ns
- Low Distortion: -65 dBc at 20 MHz

### Benefits

- Flat Frequency Response
- High Color Fidelity
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Improved Transmission Accuracy

### Applications

- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Systems
- Line Drivers

### Description

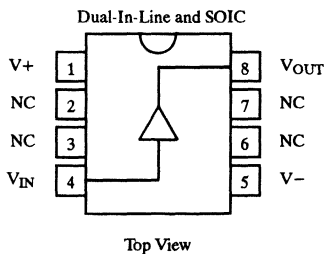
The Si581 is a monolithic closed-loop unity-gain video buffer with a very wide -3-dB bandwidth (730 MHz). Its unique design offers a high-transparency, high-performance alternative to conventional discrete, hybrid and open-loop buffers.

The Si581 features low power dissipation (150 mW, typical), fast settling (0.2% in 5 ns), without signal degradation. Distortion is typically -65 dBc at 20 MHz, gain flatness is less than 0.4 dB from dc to 50 MHz. These

performance specifications allow the designer to improve system bandwidth while reducing power dissipation, board space and design complexity. The output is protected against short circuits to ground.

The Si581 uses a complementary bipolar IC process to achieve excellent high frequency performance. All performance is specified and rated for operation with  $\pm 5$ -V supplies, reducing power consumption compared with traditional  $\pm 15$ -V designs.

### Functional Block Diagrams and Pin Configurations



#### Ordering Information

Temp Range	Package	Part Number
-40 to 85°C	8-Pin Plastic DIP	Si581DJ
	8-Pin Narrow SOIC	Si581DY

### Absolute Maximum Ratings

Supply Voltage .....  $\pm 7$  V  
 Input Voltage Range ..... V- to V+  
 Output Short Circuit Duration ..... Continuous  
 Output Current ..... 70 mA

Storage Temperature ..... -65 to 150°C  
 Lead Temperature (Soldering 10s) ..... 300°C  
 Junction Temperature:  $T_J$  ..... 175°C

## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $R_L = 100\ \Omega, R_S = 50\ \Omega$		Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
					Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Frequency Domain<sup>h</sup></b>								
-3-dB Bandwidth <sup>d</sup>	SSBW	$V_{OUT} < 0.5 V_{p-p}$		Room Full	400 300	730		MHz
	MSBW	$V_{OUT} = < 1 V_{p-p}$		Room Full		450		
	LSBW	$V_{OUT} = 5 V_{p-p}$		Room Full	55 50	90		
Gain Flatness Peaking <sup>e, g</sup>	GFPH	$V_{OUT} < 0.5 V_{p-p}$ , dc to 200 MHz		Room Full		0	0.5 0.8	dB
Gain Flatness Roll Off <sup>e</sup>	GFRH			Room Full		0	0.8 1.2	
Linear Phase Deviation <sup>e</sup>	LPD	dc to 200 MHz		Room Full		0.7	1.5 2	deg
Differential Phase	DP	$R_L = 150\ \Omega$ $V_{Carrier} = 280\text{ mV}$	$f = 3.58\text{ MHz}$	Room Full		0.01		
			$f = 4.43\text{ MHz}$	Room Full		0.01		
Differential Gain	DG	$f = 4.43\text{ MHz}$ $V_{Carrier} = 280\text{ mV}$	$R_L = 150\ \Omega$	Room Full		0.1		%
			$R_L = 1\text{ k}\Omega$	Room Full		0.07		
<b>Time Domain<sup>d, h</sup></b>								
Rise and Fall Time	$t_{RS}$	$V_{IN} = 0.5\text{ V Step}$ Input Rise/Fall time = 300 ps		Room Full		0.4	1 1.4	ns
	$t_{RL}$	$V_{IN} = 5\text{ V Step}$ Input Rise/Fall time $\leq 1\text{ ns}$		Room Full		4.5	7.5 8.5	
Settling Time	$t_{SP}$	$\pm 0.2\%$ , $V_{IN} = 2\text{ V Step}$		Full		5	10	
Slew Rate	SR			Room Full	500 450	800		V/ $\mu$ s
<b>Distortion and Noise</b>								
2nd Harmonic Distortion <sup>g</sup>	HD <sub>2</sub>	$V_{IN} = 2 V_{p-p}$ , $f_{IN} = 20\text{ MHz}$		Room Full		-65	-55 -48	dBc
3rd Harmonic Distortion <sup>g</sup>	HD <sub>3</sub>			Full		-65	-55	
Equivalent Input Noise Floor <sup>d</sup>	SNF	$f > 100\text{ kHz}$		Room Full		-158	-155 -154	dBm (1 Hz)
Equivalent Input Integrated Noise <sup>d</sup>	INV	100 kHz < $f$ < 200 MHz		Room Full		40	57 63	$\mu$ V
<b>Static, dc</b>								
Small Signal Gain <sup>d</sup>	GA			Room Full	0.96 0.95	0.97		V/V
Integral Endpoint Linearity <sup>d</sup>	ILIN	$\pm 2\text{ V Full Scale}$		Room Full		0.2	0.4 0.8	%FS
Input Offset Voltage <sup>f</sup>	VIO			Room Full		2	8 16	mV
Input Offset Voltage Average Temperature Coefficient <sup>d</sup>	DVIO			Room Full		20	- 100	$\mu$ V/°C
Input Bias Current <sup>f</sup>	IBN			Room Full		$\pm 20$	$\pm 50$ $\pm 100$	$\mu$ A
Input Bias Current Average Temperature Coefficient <sup>d</sup>	DIBN			Room Full		200	- 700	nA/°C
Power Supply Rejection Ratio <sup>g</sup>	PSRR			Full	45	50		dB
Supply Current <sup>f</sup>	I+	No Load		Full		15	20	mA

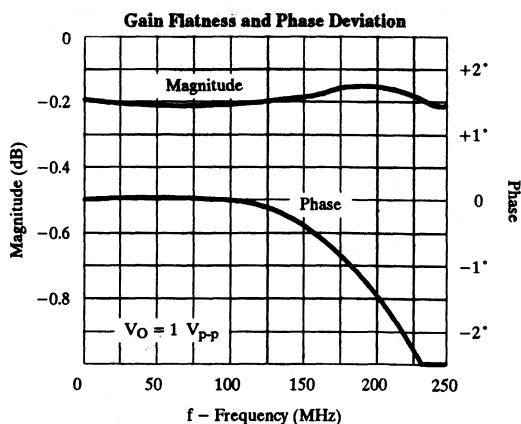
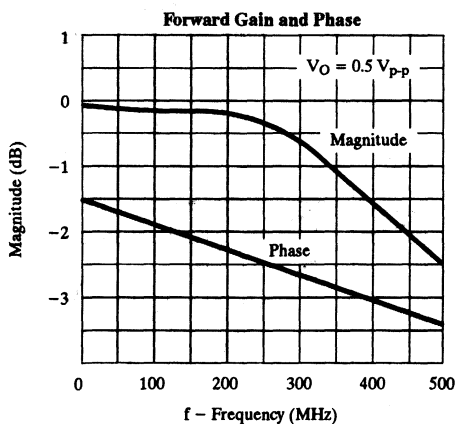
**Specifications**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $R_L = 100\ \Omega, R_S = 50\ \Omega$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Miscellaneous<sup>d</sup></b>							
Input Resistance	$R_{IN}$		Room Full	100 50	160		k $\Omega$
Input Capacitance	$C_{IN}$		Room Full		1.6	2.2 2.5	pF
Output Impedance	$R_O$	At dc	Room Full		2	3 3.5	$\Omega$
Output Voltage Range	$V_O$		Room Full	-3.2 -3	$\pm 4$	3.2 3	V
Output Current	$I_O$		Room Full	-50 -45	$\pm 70$	50 45	mA

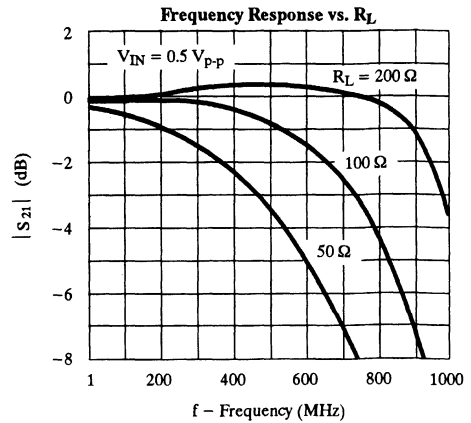
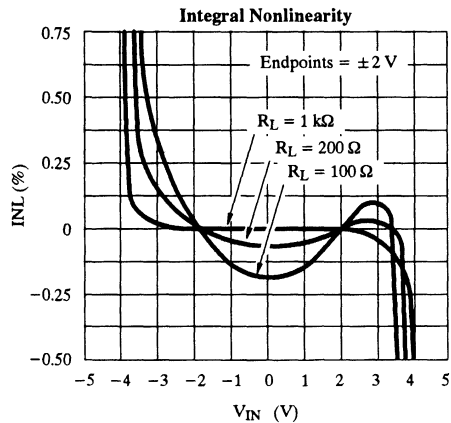
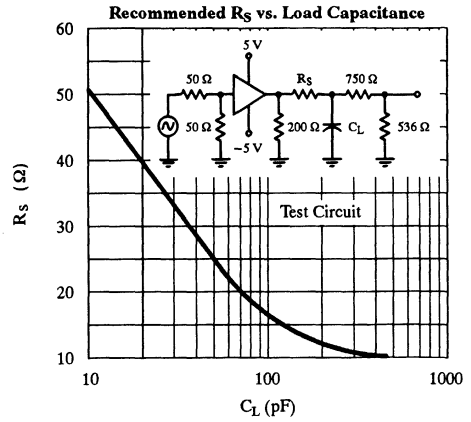
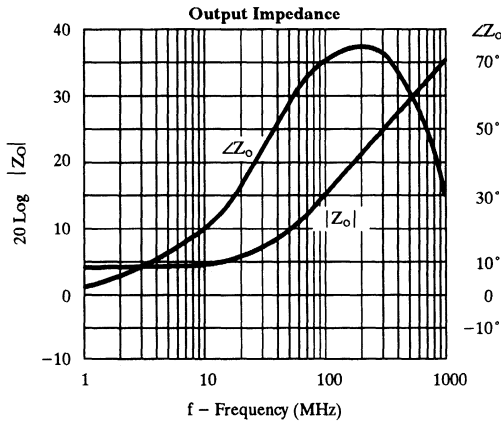
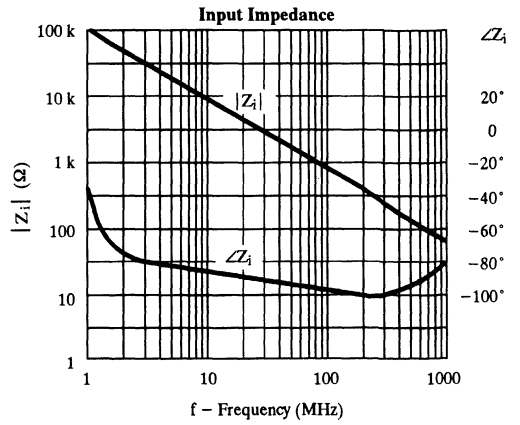
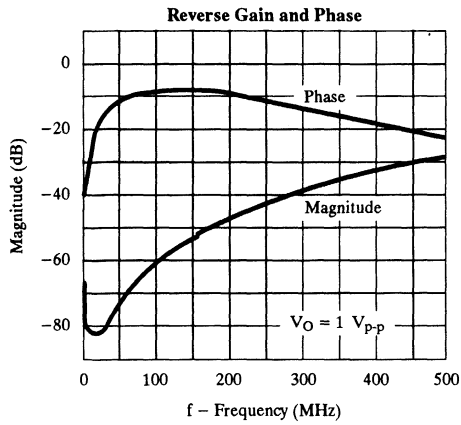
**Notes:**

- a. Room = 25°C, Full = -40 to 85°C.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guaranteed by design, not subject to production test.
- e. Gain flatness tests are performed from 0.1 MHz to 200 MHz.
- f. Parameter is 100% tested at 25°C and sample tested at 85°C.
- g. Parameter is sample tested at 25°C.
- h. AC performance is very dependent on layout. Specifications apply only in a 50- $\Omega$  microstrip environment.

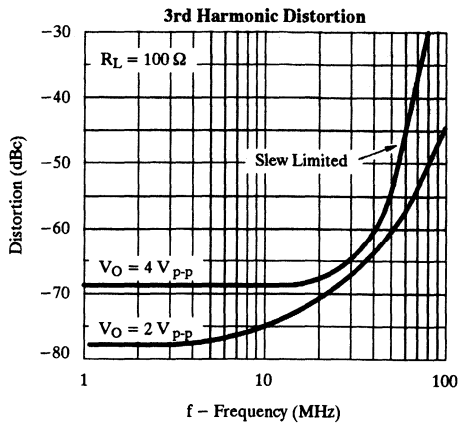
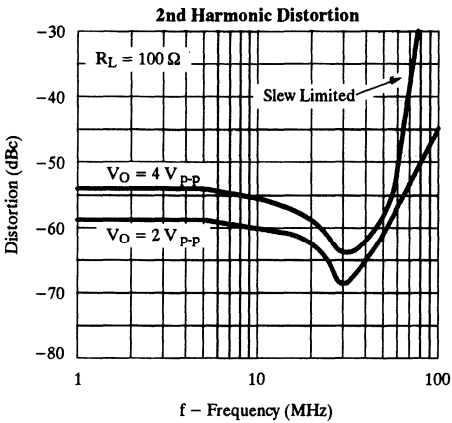
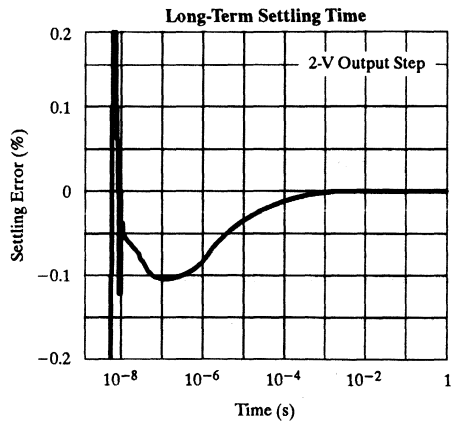
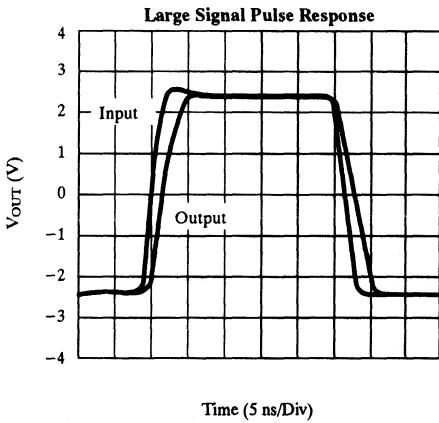
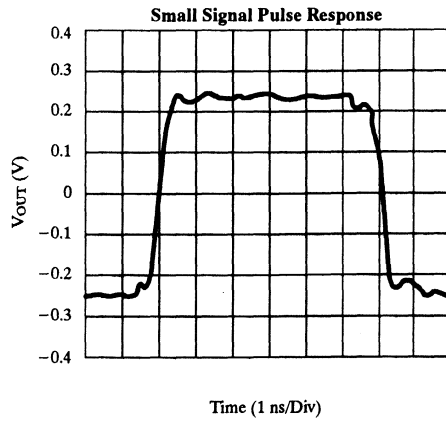
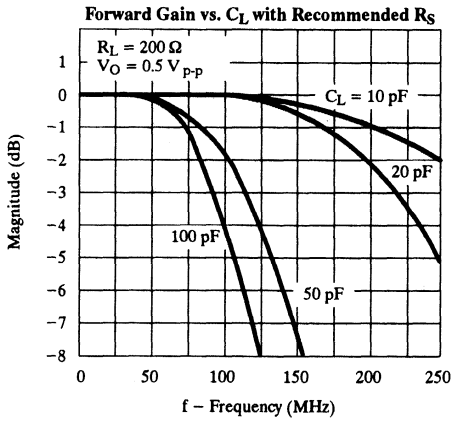
**Typical Characteristics:  $V_{SUP} = \pm 5\text{ V}, R_L = 100\ \Omega, R_S = 50\ \Omega$**



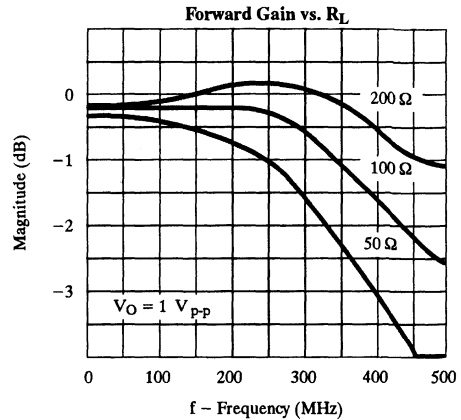
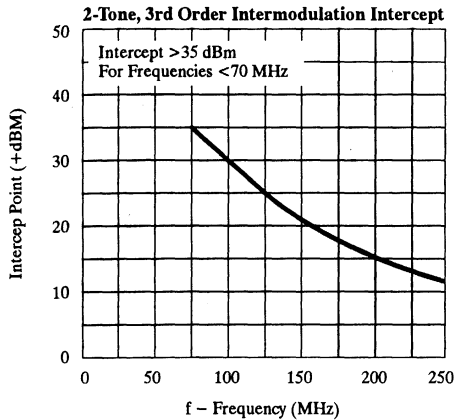
Typical Characteristics:  $V_{SUP} = \pm 5\text{ V}$ ,  $R_L = 100\ \Omega$ ,  $R_S = 50\ \Omega$  (Cont'd)



**Typical Characteristics:  $V_{SUP} = \pm 5\text{ V}$ ,  $R_L = 100\ \Omega$ ,  $R_S = 50\ \Omega$  (Cont'd)**



## Typical Characteristics: $V_{SUP} = \pm 5\text{ V}$ , $R_L = 100\ \Omega$ , $R_S = 50\ \Omega$ (Cont'd)



## Applications

The Si581 provides the accuracy of a closed-loop amplifier plus unmatched dynamic performance.

As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the Si581 which has a typical bandwidth of 730 MHz.

To minimize capacitive feedthrough, the pins which are not connected internally (pins 2, 3, 6, and 7) should be connected to the ground plane. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the Si581. On a 0.065-inch epoxy PCB material, a 50- $\Omega$  transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing. The ferrite beads are optional and are recommended only

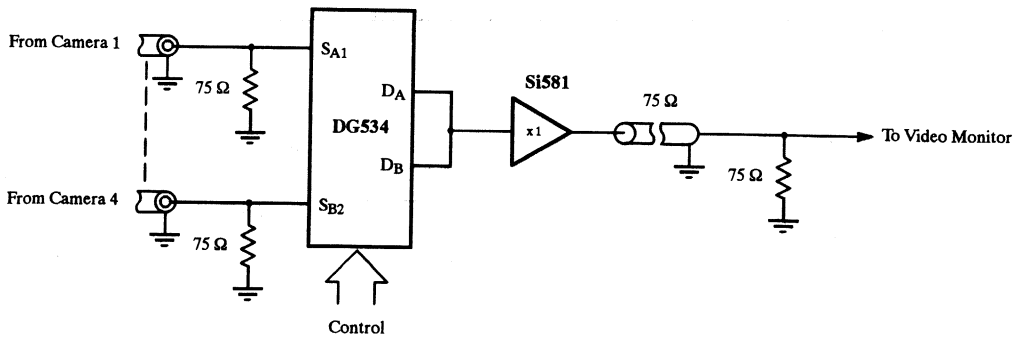
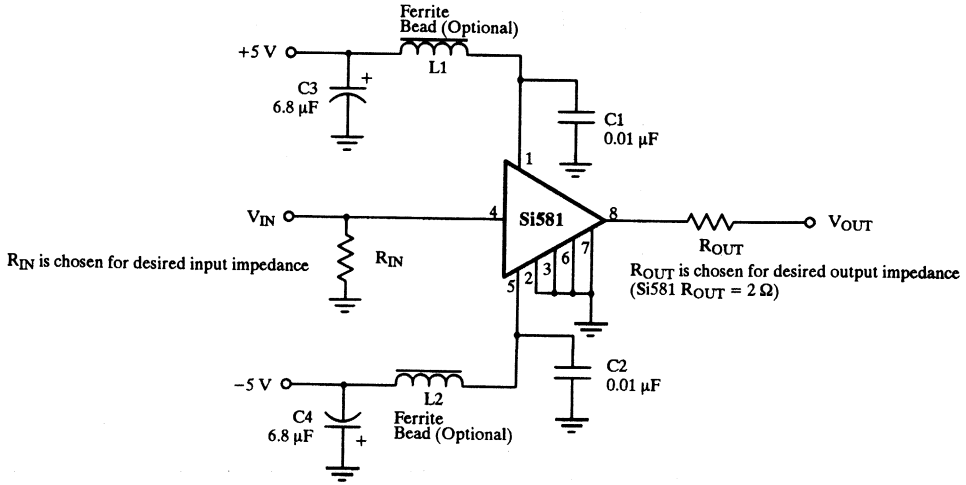
where additional isolation from high-frequency (>400 MHz) resonances of the power supply is needed.

Parasitic or load capacitance directly on the output of the Si581 will introduce additional phase shift in the device, which can lead to decreased phase margin and frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The typical characteristic curves illustrate the required resistor value and the resulting performance vs. capacitance.

Precision resistors with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors or standard spirally-trimmed metal film resistors will work, though they will cause a degradation of ac performance due to their reactive nature at high frequencies.



**Applications (Cont'd)**



## Wideband Video Amplifier

### Features

- -3-dB Bandwidth: 100 MHz
- Low Differential Gain: 0.01%
- Low Differential Phase: 0.01°
- ±1 to ±8 Closed-Loop Gain Range
- Low Power— $P_D$ : 160 mW
- Fast Settling: 0.05% in 12 ns
- Low Distortion: -60 dBc at 20 MHz
- DISABLE Function

### Benefits

- Flat Frequency Response
- High Color Fidelity
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Improved Transmission Accuracy
- Small Size
- Automatic Power-Down

### Applications

- Coaxial Cable Drivers
- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Systems

### Description

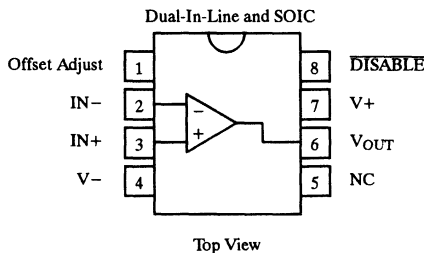
The Si582 is a monolithic video amplifier with a -3-dB bandwidth of 100 MHz. Its unique current-feedback design offers a high-transparency, high-performance alternative to conventional discrete, hybrid and other video amplifiers.

The Si582 features wide bandwidth, low power dissipation (150 mW; typ) and fast settling (0.05% in 12 ns). Distortion is typically -60 dBc at 20 MHz, gain flatness is less than 0.3 dB from dc to 40 MHz. These performance specifications allow the designer to improve system bandwidth while reducing power dissipation, board space and design complexity. The wide bandwidth combined with

a 50-mA output current at a gain of 2 provides an excellent high performance solution for video distribution and line driving applications. In addition, digital transmission systems will benefit from its superior pulse response. The output is protected against short circuits to ground.

The Si582 uses a complementary bipolar IC process to achieve excellent high frequency performance. All parameters are specified and rated for operation with ±5 V supplies, reducing power consumption compared with traditional ±15 V designs.

### Functional Block Diagrams and Pin Configurations



#### Ordering Information

Temp Range	Package	Part Number
-40 to 85°C	8-Pin Plastic DIP	Si582DJ
	8-Pin Narrow SOIC	Si582DY

### Absolute Maximum Ratings

Supply Voltage ..... ±7 V  
 Input Voltage Range ..... V- to V+  
 Output Short Circuit Duration ..... Continuous  
 Output Current ..... 70 mA  
 Common Mode Input Voltage ..... V- to V+

Differential Input Voltage ..... 5 V  
 Disable Input Voltage ..... V- to V+  
 Storage Temperature ..... -65 to 150°C  
 Lead Temperature (Soldering 10s) ..... 300°C  
 Junction Temperature:  $T_J$  ..... 175°C

**Specifications**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $R_L = 100\ \Omega, R_F = 250\ \Omega, A_V = 2$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit	
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>		
<b>Frequency Domain<sup>b</sup></b>								
-3 dB Bandwidth <sup>d</sup>	SSBW	$V_{OUT} = \leq 0.5 V_{p-p}$	Room Full	150 120	200		MHz	
	MSBW	$V_{OUT} = \leq 2 V_{p-p}$	Room		100			
	LSBW	$V_{OUT} = 5 V_{p-p}, A_V = 5$	Full	35	50			
Gain Flatness Peaking <sup>f, h</sup>	GFPL	$V_{OUT} \leq 0.5 V_{p-p}$	dc to 40 MHz	Room		0	0.3	dB
	GFPH		>40 MHz	Room Full		0	0.5 0.7	
GFR			dc to 75 MHz	Room Full		0.6	1 1.3	
Linear Phase Deviation	LPD	dc to 75 MHz	Room Full		0.2	1 1.2	deg	
Differential Phase	DP	$A_V = 2, R_F = 250\ \Omega, R_L = 150\ \Omega$ 1 $V_{p-p}$ Video Signal, 3.58 MHz	Room Full		0.01	0.02 0.1	%	
Differential Gain	DG		Room Full		0.01	0.04 0.05		
<b>Time Domain<sup>f, h</sup></b>								
Rise and Fall Time <sup>d</sup>	$t_{RS}$	$V_{IN} = 0.5\text{ V Step}$	Full		1.6	2.4	ns	
	$t_{RL}$	$V_{IN} = 5\text{ V Step}$	Full		6.5	10		
Settling Time <sup>d</sup>	$t_S$	To $\pm 0.05\%$ , $V_{IN} = 2\text{ V Step}$	Full		12	15		
Slew Rate <sup>d</sup>	SR	$A_V = 2$	Full	430	700		V/ $\mu$ s	
	SR <sub>1</sub>	$A_V = -2$	Full		1600			
<b>Distortion and Noise</b>								
2nd Harmonic Distortion <sup>f, h</sup>	HD <sub>2</sub>	$V_{IN} = 2 V_{p-p}, f_{IN} = 20\text{ MHz}$	Room Full		-60	-45 -40	dBc	
3rd Harmonic Distortion <sup>f, h</sup>	HD <sub>3</sub>		Full		-60	-50		
Equivalent Input Noise Floor <sup>d</sup>	SNF	$f > 100\text{ kHz}, 50\ \Omega$ on Input	Room Full		-157	-154 -153	dBm (1 Hz)	
Equivalent Input Integrated Noise <sup>d</sup>	INV	100 kHz < $f$ < 200 MHz	Room Full		40	57 54	$\mu$ V	
<b>Switching (Disable)</b>								
Turn On Time	$t_{ON}$		Full		100	200	ns	
Turn Off Time	$t_{OFF}$	To 50 dB Attenuation @ 10 MHz	Full		0.2	1	$\mu$ s	
Off Isolation <sup>d</sup>	OI	$f_{IN} = 10\text{ MHz}, \text{DISABLE} = "0"$	Full	-55	-59		dB	
Current to Disable	$I_{DIS}$		Full	-250	-200		$\mu$ A	
Current to Enable			Full		-80	-60		
Disable Drive Voltage	$V_{DISL}$	$\text{DISABLE} = "0", I_{DIS} = 250\ \mu\text{A}$	Full		1	0.5	V	
Voltage to Enable	$V_{DISH}$	$\text{DISABLE} = "1"$	Room Full	3.2 4	2.6			
<b>Static, dc</b>								
Input Offset Voltage <sup>f</sup>	VIO		Room Full	-5 -9	$\pm 2$	5 9	mV	
Input Offset Voltage Average Temperature Coefficient <sup>d</sup>	DVIO		Room Full	-40	$\pm 20$	40	$\mu\text{V}/^\circ\text{C}$	
Input Bias Current Non-inverting <sup>f</sup>	IBN		Room Full	-20 -36	10	20 36	$\mu\text{A}$	

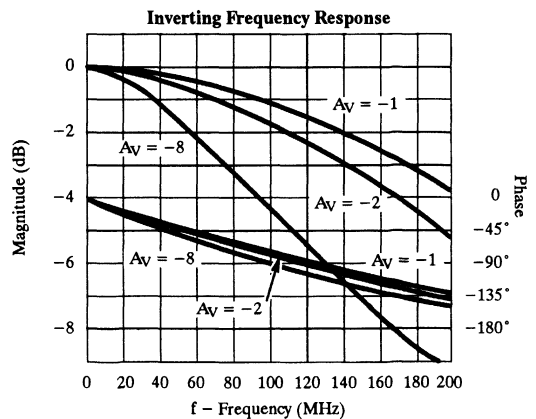
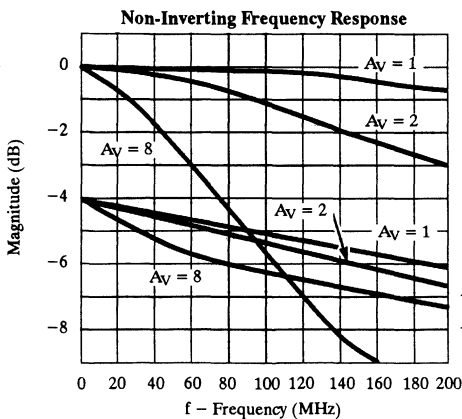
## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $R_L = 100\ \Omega, R_F = 250\ \Omega, A_V = 2$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Static, dc (Cont'd)</b>							
Input Bias Current Non-inverting Temperature Coefficient <sup>d</sup>	DIBN		Room Full	-200	100	200	nA/°C
Input Bias Current Inverting <sup>f</sup>	IBI		Room Full	-20 -36	±10	20 36	µA
Input Bias Current Inverting Temperature Coefficient <sup>d</sup>	DIBI		Room Full	-200	±50	200	nA/°C
Power Supply Rejection Ratio <sup>g</sup>	PSRR		Full	45			dB
Common Mode Rejection Ratio	CMRR		Full	45			
Supply Current <sup>f</sup>	I+	No Load	Full		16	18	mA
		Disabled, No Load	Full		4	6	
<b>Miscellaneous</b>							
Non-inverting Input Resistance	R <sub>IN</sub>		Room Full	100 50	200		kΩ
Non-inverting Input Capacitance	C <sub>IN</sub>		Full		0.5	2	pF
Output Impedance	R <sub>O</sub>	At dc	Full		0.1	0.2	Ω
Output Voltage Range	V <sub>O</sub>	No Load	Room Full	-3.2 -3	±3.5	3.2 3	V
Common Mode Input Range For Rated Performance	CMIR		Room Full	-2 -1.2	±2.1	2 1.2	
Output Current <sup>d</sup>	I <sub>O</sub>		Room Full	-50 -35	±70	50 35	mA

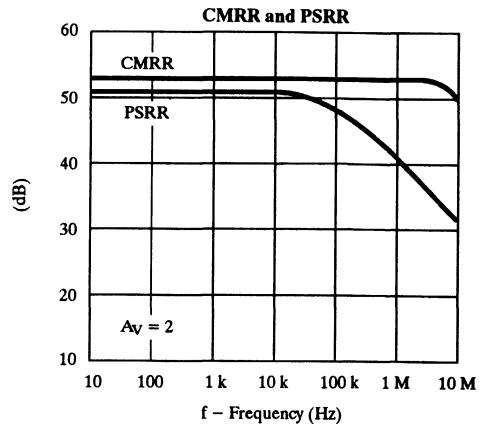
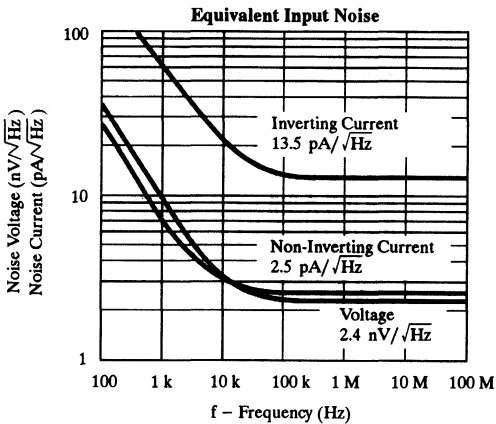
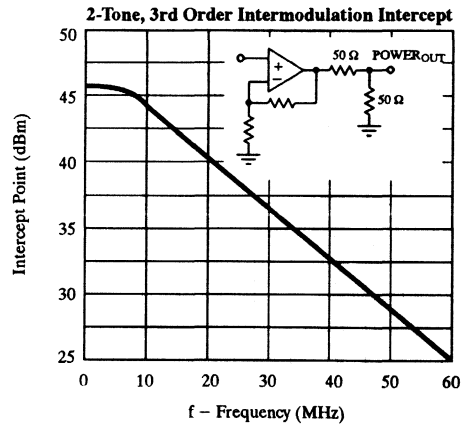
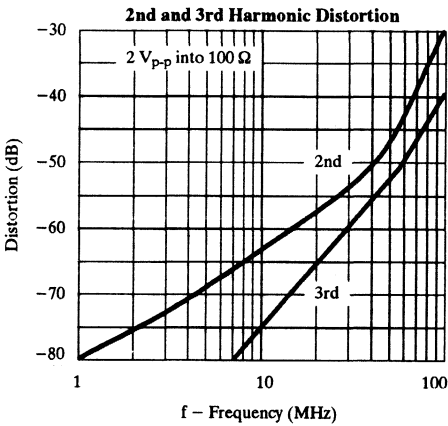
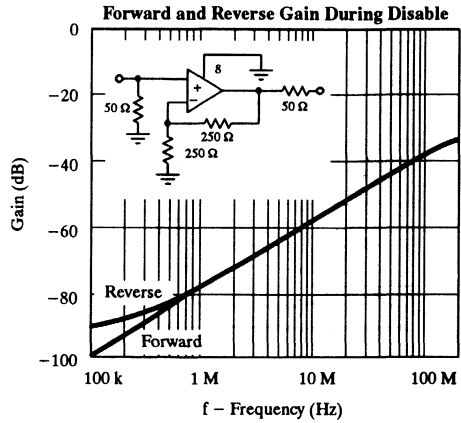
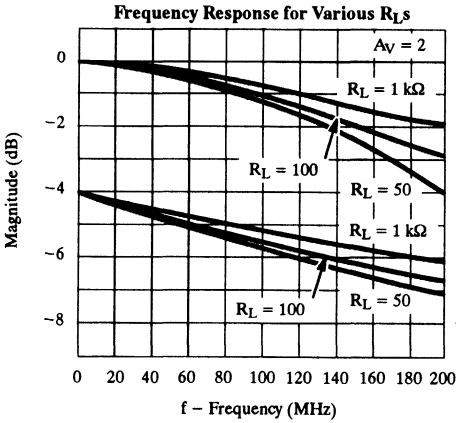
**Notes:**

- Room = 25°C, Full = -40 to 85°C.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production testing.
- Gain flatness tests are performed from 0.1 MHz to 50 MHz, and specifications are guaranteed from dc to 50 MHz.
- Parameter is 100% tested at 25°C and sample tested at 85°C.
- Parameter is sample tested at 25°C.
- Ac performance is very dependent on layout. Specifications apply only in a 50-Ω microstrip environment.

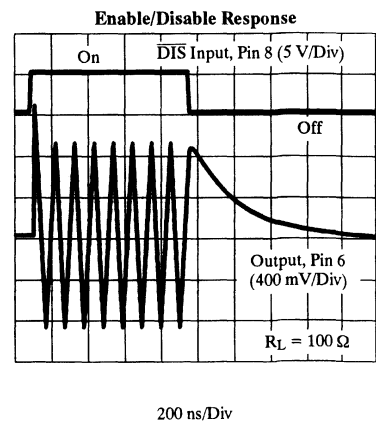
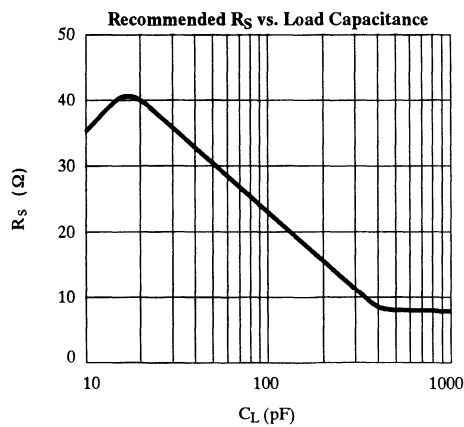
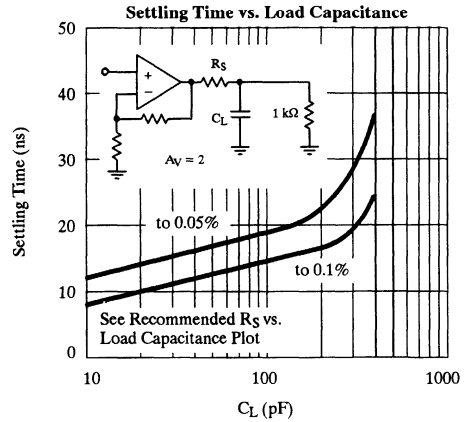
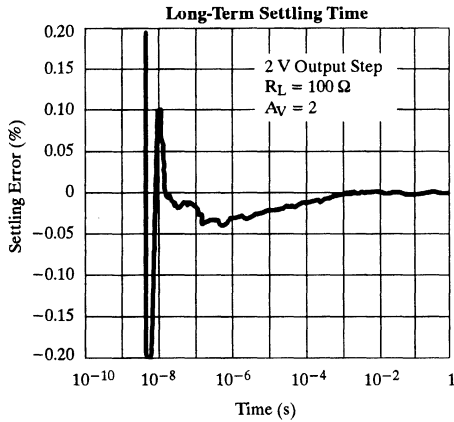
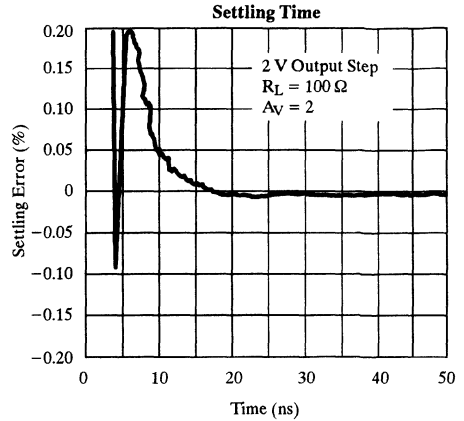
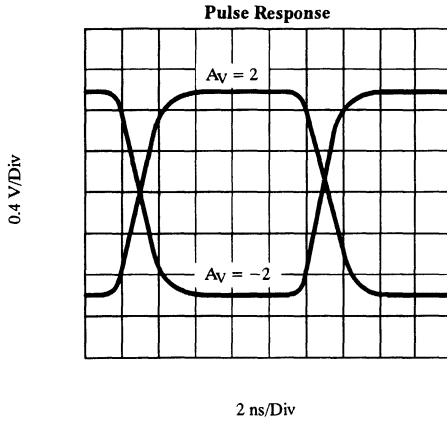
## Typical Characteristics



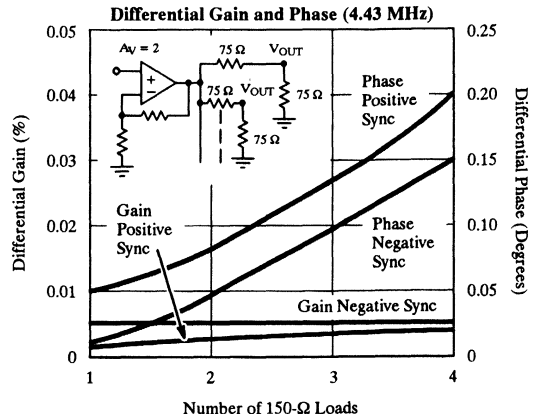
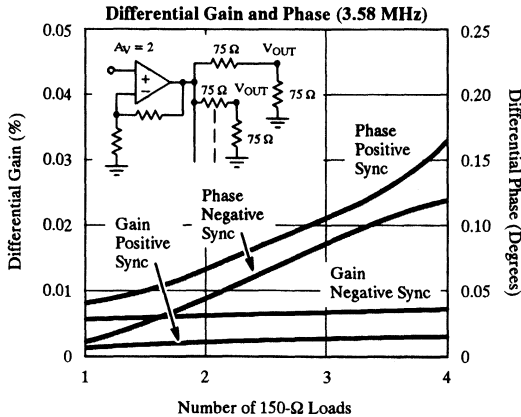
**Typical Characteristics**



## Typical Characteristics



## Typical Characteristics



## Applications

### Setting Loop Gain

The Si582 uses a current feedback topology instead of the more common voltage feedback, meaning that the closed loop bandwidth and settling time are relatively independent of closed loop gain.

Optimum bandwidth is achieved with a feedback resistor of 220 to 270  $\Omega$ . Closed loop gain is then set by a suitable choice of input resistor value. Figure 1 shows the connections for inverting and non-inverting gains. Feedback resistors greater than 270  $\Omega$  may be used, but at the expense of bandwidth. Values lower than 220  $\Omega$  will cause amplitude peaking in the passband. For example, a feedback resistor value of 100  $\Omega$  will create a peak of approximately 4 dB as roll-off is approached.

Under no circumstances should the output be connected directly to the inverting input in the hope of achieving unity gain. This will cause the device to oscillate and draw significant current from the power supply. Unity gain may be achieved with a 220- to 270- $\Omega$  resistor in the feedback path with no input resistor. Similarly, capacitive feedback should not be used with the Si582.

### Offset Correction

Since the two inputs to the Si582 are quite different internally, the noise and offset performance differs from that of a differential input op-amp. The two input bias currents are unrelated, so that the technique of bias current error cancellation by matching of the inverting and non-inverting input resistances is ineffective.

The equation for output offset is shown in Figure 1, and is the algebraic sum of the equivalent input voltage and current sources which influence dc operation. Pin 1 may be used to correct for the  $\pm 10$ -mV offset by connecting as shown in Figure 1. When not used, pin 1 should be bypassed to signal ground with a 0.1- $\mu$ F low inductance capacitor.

### Disable Operation

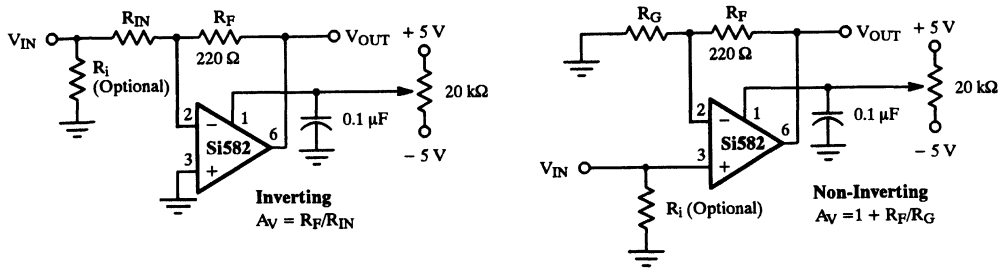
The disable function of the Si582 is obtained by taking pin 8 to ground. A minimum current of 250  $\mu$ A needs to be sunk, and a maximum voltage of 0.5 V is required for full disable. When the disable function is not required, pin 8 may be left open or could be tied to the +5-V rail.

Disabling the amplifier reduces power supply current and places the output and inverting input pins in a high impedance state (200 k $\Omega$  || 0.5 pF)

### PCB Layout and Supply Bypassing

The Si582 bandwidth and pulse response are dependent upon good layout and decoupling techniques. Ground plane construction is recommended to preserve as low a ground impedance as possible. Power supply decoupling components should be mounted close to the package and should have good high frequency characteristics to preserve the excellent pulse performance of the device. Figure 2 shows the recommended decoupling circuit. The 10- $\mu$ F capacitor should be Tantalum or other low ESR/ESL type. For the 0.1- $\mu$ F capacitor, multi-layer ceramic capacitors are recommended. A low value resistor in series with the 10- $\mu$ F capacitor's ground lead may be required to reduce output pulse ringing.

## Applications



$$\text{Output Offset} = \pm I_{BN} \times R_S(1 + R_F/R_{IN}) \pm V_{IO}(1 + R_F/R_{IN}) \pm I_{BI} \times R_F$$

Where:

- $I_{BI}$  = Inverting Input Bias Current
- $I_{BN}$  = Non-Inverting Input Bias Current
- $R_S$  = Non-Inverting Pin Resistance
- $V_{IO}$  = Input Offset Voltage
- $R_i$  sets the impedance

Figure 1. Si582 Gain Circuits

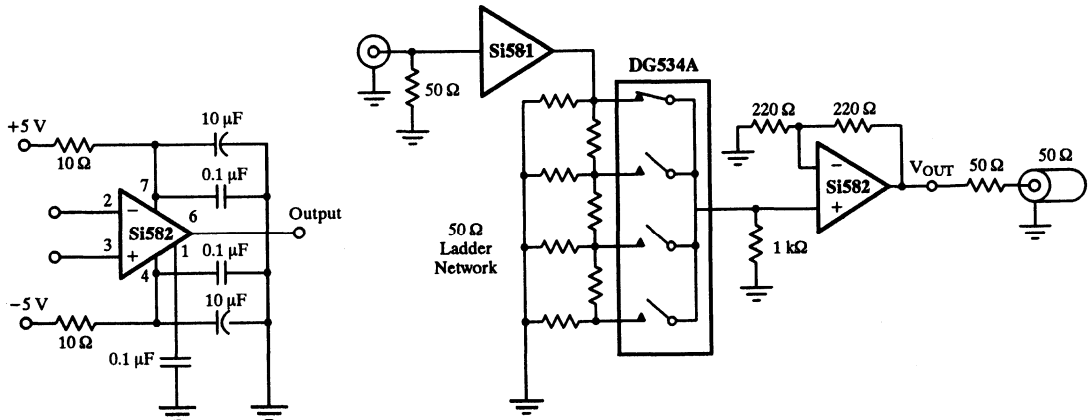


Figure 2. Decoupling the Si582

Figure 3. 4-Step Wideband Digitally Controlled Attenuator

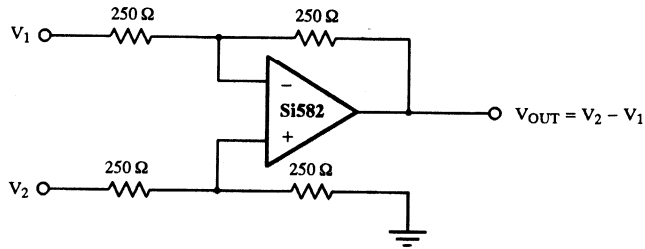
### Digitally Controlled Attenuator

Figure 3 shows the Si582 in a wideband, digitally controlled attenuator circuit employing the DG534A, a 4 to 1 D/CMOS multiplexer. The Si581 buffers the input and drives the 50-Ω ladder attenuator. Taps are chosen to suit

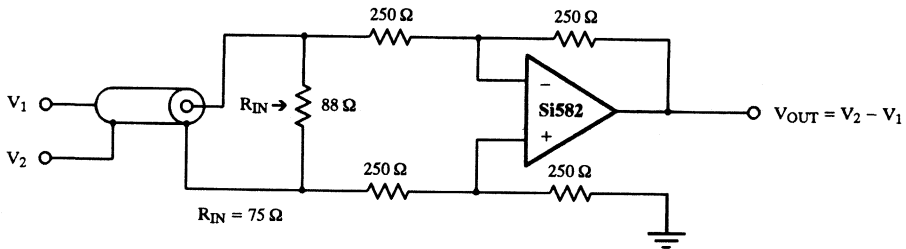
the application, i.e., 0.1-dB or 1-dB steps. The second Si582 buffers the multiplexer for good linearity and, at a gain of two, provides “lossless” cable termination at the output.



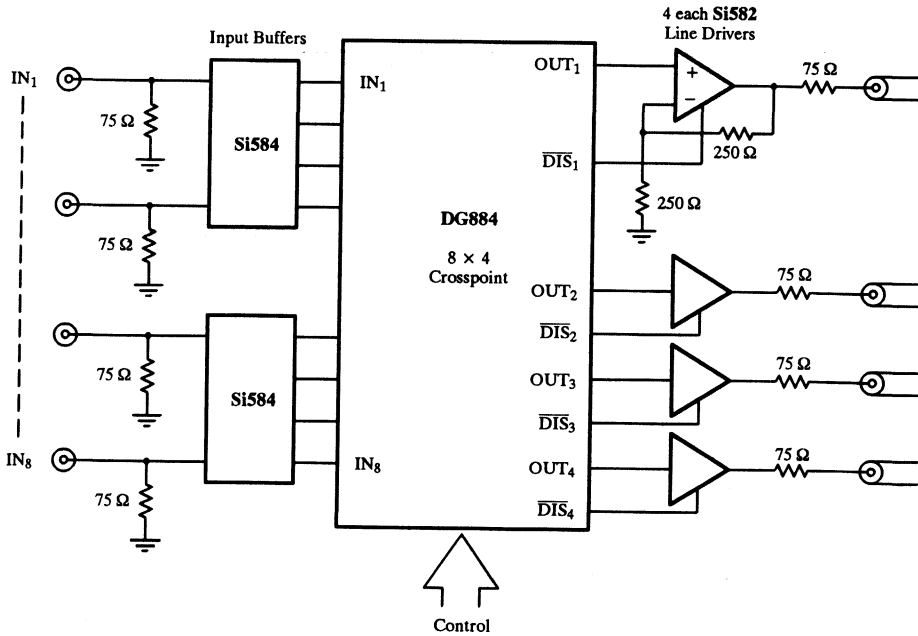
**Applications**



**Figure 4. Differential Amplifier**



**Figure 5. Differential Line Receiver**



**Figure 6. 50 MHz 8 x 4 Video Crosspoint Switch**

## Quad Unity-Gain Video Buffer

### Features

- -3-dB Bandwidth: 120 MHz
- 30-MHz Gain Flatness: 0.1 dB
- High Channel Isolation: 62 dB @ 10 MHz
- Low Differential Gain—0.08%
- Low Differential Phase—0.1°
- Low Power— $P_D$ : 30 mW/Channel
- Fast Settling: 0.1% in 10 ns
- Low Distortion: -58 dBc @ 20 MHz

### Benefits

- Flat Frequency Response
- High Color Fidelity
- Improved Transmission Accuracy
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Small Size

### Applications

- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Systems

### Description

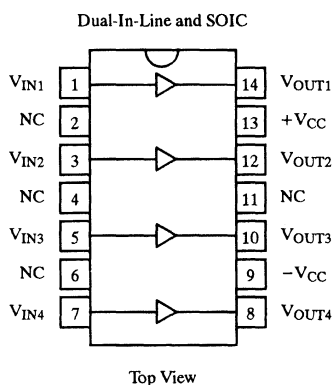
The Si584 is a monolithic closed-loop quad video buffer with a wide -3-dB bandwidth (120 MHz). Its unique design, optimized for high quality video switching, offers a high-performance alternative to conventional discrete, hybrid and open-loop buffers.

The Si584 features wide bandwidth, low power consumption, fast settling (0.1% in 10 ns), without signal degradation. Third harmonic distortion is typically -58 dBc at 20 MHz, gain flatness is typically 0.1 dB from dc to 30 MHz. These performance specifications allow the

designer to improve system bandwidth while reducing system power consumption, board space and design complexity. The outputs are protected against short circuits to ground.

The Si584 is built on an advanced complementary bipolar process to achieve excellent high frequency performance. All performance is specified and rated for operation with  $\pm 5$ -V supplies, reducing power consumption compared with traditional  $\pm 15$ -V designs.

### Functional Block Diagrams and Pin Configurations



#### Ordering Information

Temp Range	Package	Part Number
-40 to 85°C	14-Pin Plastic DIP	Si584DJ
	14-Pin Narrow SOIC	Si584DY

### Absolute Maximum Ratings

Supply Voltage .....  $\pm 7$  V  
 Input Voltage Range ..... V- to V+  
 Output Current ..... 35 mA

Storage Temperature ..... -65 to 150°C  
 Lead Temperature (Soldering 10s) ..... 300°C  
 Junction Temperature:  $T_J$  ..... 175°C

**Specifications**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $R_L = 100\ \Omega, R_S = 50\ \Omega$		Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
					Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Frequency Domain<sup>g</sup></b>								
-3 dB Bandwidth <sup>f</sup>	SSBW	$V_{OUT} \leq 0.5\text{ V}_{p-p}$		Room Full	135 120	200		MHz
	MSBW	$V_{OUT} = 1\text{ V}_{p-p}$		Room		120		
	LSBW	$V_{OUT} = 2\text{ V}_{p-p}$		Full	70	95		
Gain Flatness Peaking <sup>f</sup>	GFPL	$V_{OUT} \leq 0.5\text{ V}_{p-p}$	0.1 to 30 MHz	Room Full		0	0.2 0.3	dB
	GFPH		>30 MHz	Room Full		0	0.4 0.7	
Crosstalk	X-TALK	$f = 10\text{ MHz}$		Room		62		
<b>Time Domain<sup>d, g</sup></b>								
Rise and Fall Time	$t_{RS1}$	$V_{IN} = 0.5\text{ V Step}$		Room Full		1.8 2.8	3.0	ns
	$t_{RS2}$	$V_{IN} = 2\text{ V Step}$		Room Full		5 7	8	
Settling Time	$t_s$			Room Full		10 15	20	
Overshoot	OS	$V_{IN} = 0.5\text{ V Step}$		Room Full		3	10 15	%
Slew Rate	SR			Room Full	200 180	450		V/ $\mu$ s
<b>Static, dc</b>								
Small Signal Gain <sup>d</sup>	GA			Room Full	0.96 0.95	0.97		V/V
Integral Endpoint Linearity <sup>d</sup>	$I_{LIN}$	$\pm 1\text{ V Full Scale}$		Room		0.4	0.6	%
Output Offset Voltage <sup>e</sup>	VIO			Room Full		$\pm 0.5$	$\pm 5$ $\pm 8.2$	mV
Input Offset Voltage Average Temperature Coefficient <sup>e</sup>	DVIO			Room Full		$\pm 9$	$\pm 40$	$\mu$ V/ $^{\circ}$ C
Input Bias Current <sup>e</sup>	$I_B$			Room Full		$\pm 1$	$\pm 5$ $\pm 10$	$\mu$ A
Power Supply Rejection Ratio <sup>e</sup>	PSRR			Room Full	48 46	56		dB
Supply Current, Total <sup>e</sup>	$I_+$	No Load		Room Full		12	16.5 17	mA
<b>Miscellaneous</b>								
Input Resistance	$R_{IN}$			Room Full	1 0.3	1.5		M $\Omega$
Input Capacitance	$C_{IN}$			Room Full		1.8	3 3.5	pF
Output Impedance	$R_O$	At dc		Room Full		2.5	3.5 5	$\Omega$
Output Voltage Range	$V_O$	No Load		Room Full	$\pm 3.8$ $\pm 3.6$	$\pm 4$		V
Output Current, per Buffer <sup>d</sup>	$I_O$			Room Full	$\pm 20$ $\pm 12$	$\pm 25$		mA
2nd Harmonic Distortion <sup>f</sup>	HD <sub>2</sub>	$V_{IN} = 2\text{ V}_{p-p}, f_{IN} = 20\text{ MHz}$		Room Full		-50	-38 -36	dBc
3rd Harmonic Distortion <sup>f</sup>	HD <sub>3</sub>			Room Full		-58	-50 -45	
Equivalent Input Noise Floor <sup>d</sup>	SNF	$f > 100\text{ kHz}, 50\ \Omega$ on Input		Room Full		-155	-153 -152	dBm (1 Hz)

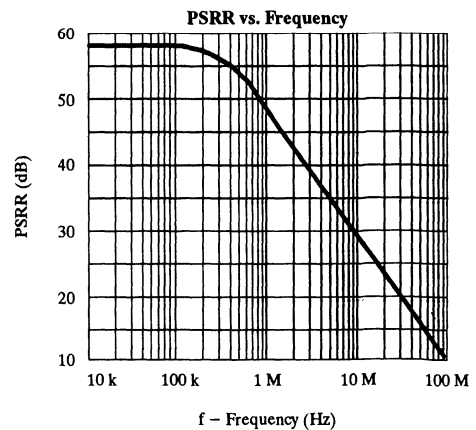
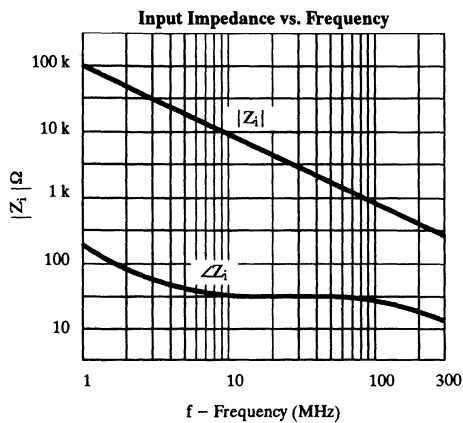
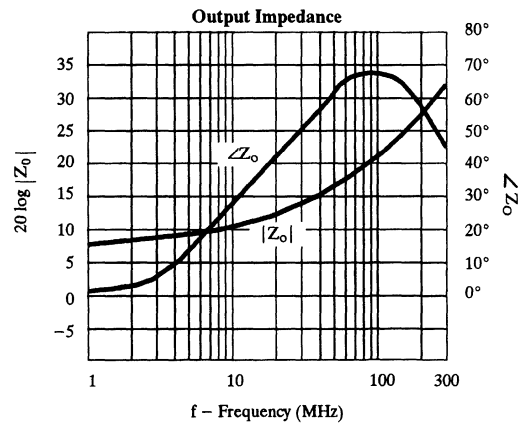
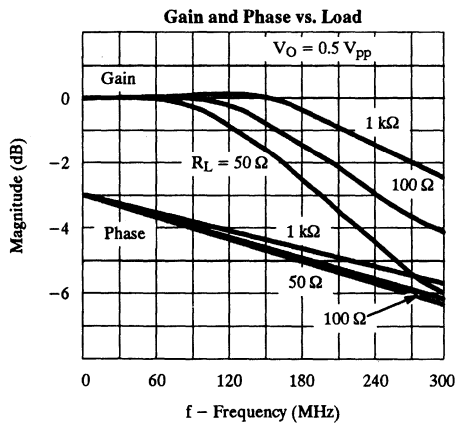
## Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $R_L = 100\ \Omega, R_S = 50\ \Omega$	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Performance Driving a DG884 Crosspoint Switch<sup>4, 8</sup></b>							
2nd Harmonic Distortion	HD <sub>2</sub>	See Test Load See Figure 1	$V_{IN} = 2\text{ V}_{p-p}$ $f_{IN} = 5\text{ MHz}$	Room	-60		dBc
3rd Harmonic Distortion	HD <sub>3</sub>			Room	-58		
Differential Phase	DP			Room	0.1		deg
Differential Gain	DG			Room	0.08		%
Crosstalk (All Hostile)	X <sub>TALK(AH)</sub>			Room	-54		dB

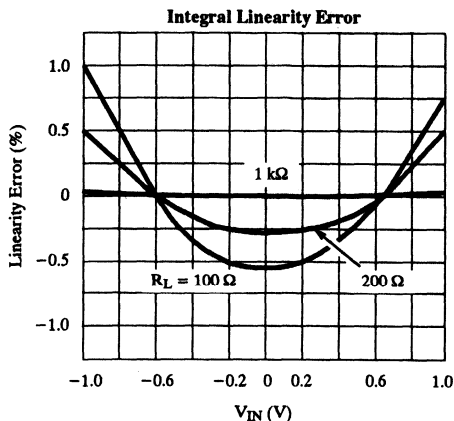
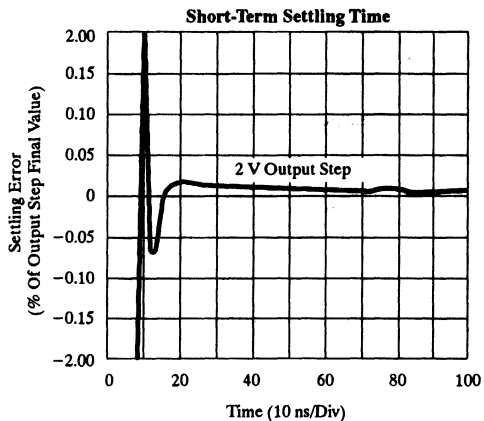
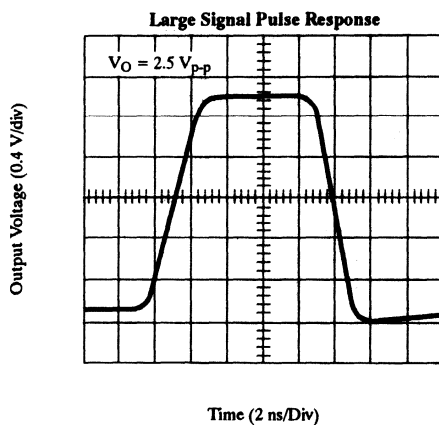
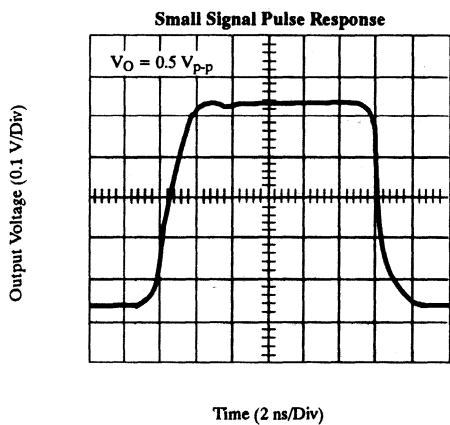
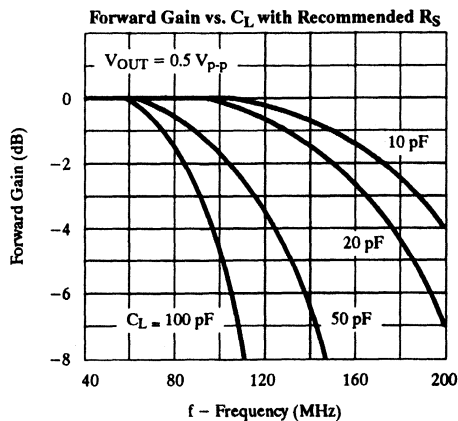
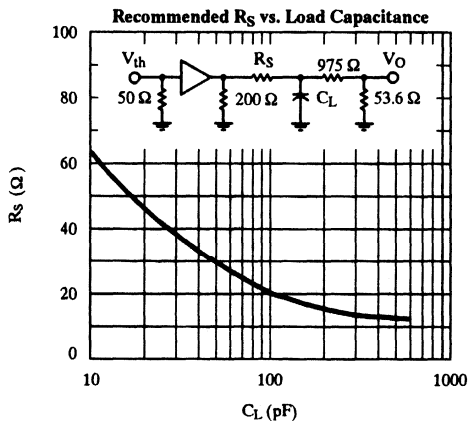
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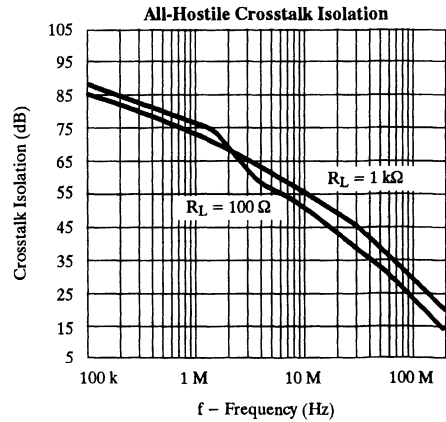
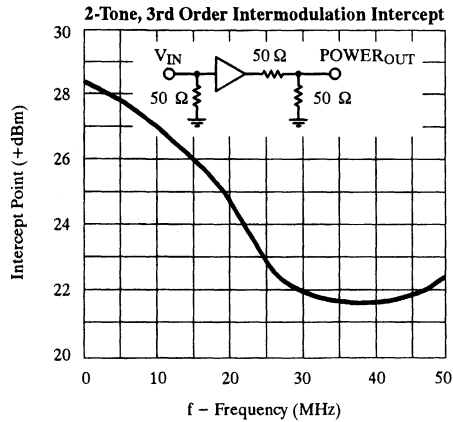
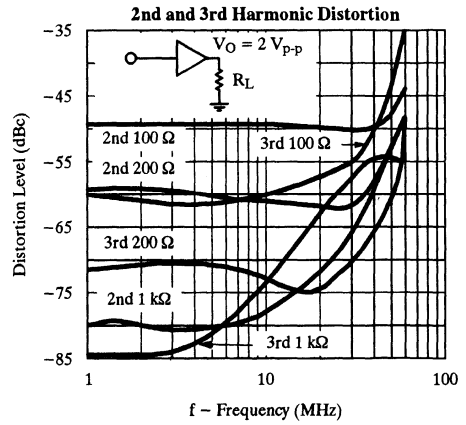
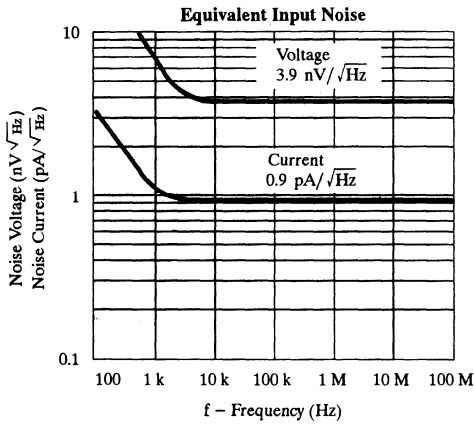
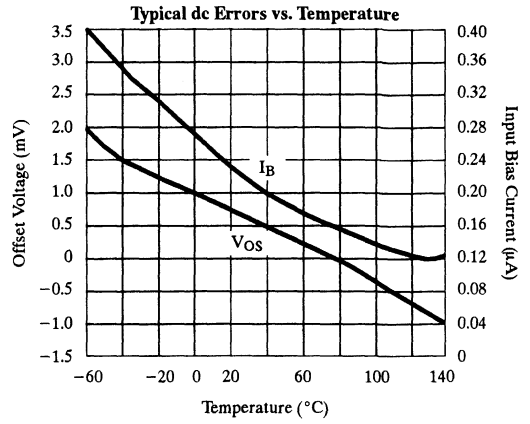
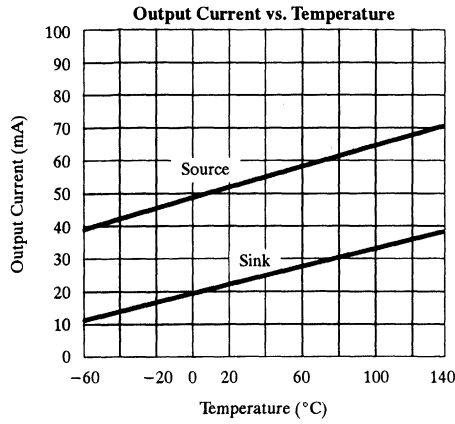
### Typical Characteristics: $T_A = 25^\circ\text{C}, V_{CC} = \pm 5\text{ V}, R_L = 100\ \Omega$



**Typical Characteristics:  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \pm 5\text{ V}$ ,  $R_L = 100\ \Omega$  (Cont'd)**



## Typical Characteristics: $T_A = 25^\circ\text{C}$ , $V_{CC} = \pm 5\text{ V}$ , $R_L = 100\ \Omega$ (Cont'd)



**Test Circuit**

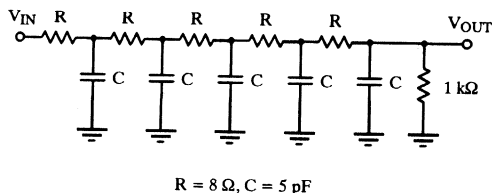


Figure 1. Test Load

**Applications**

**Operation**

The Si584 is a quad unity gain buffer that offers high-speed and low-power operation. Its closed loop topology provides higher accuracy than that normally found in open loop designs. The Si584 was designed to optimize differential gain and phase when driving the distributed capacitance of a video multiplexer or crosspoint such as the DG884.

**Board Layout and Crosstalk**

High frequency designs demand good PC board layout for best performance. A ground plane and power supply bypassing with high-frequency ceramic capacitors adjacent to the power supply pins are essential. Second harmonic distortion can be improved by ensuring equal current return paths for both the positive and negative supplies. This is accomplished by connecting one side of the bypass capacitors at the same point in the ground plane while keeping the supply sides within 0.1" of the Si584 supply pins.

Crosstalk is strongly dependent on board layout. Closely spaced signal traces on the board will degrade crosstalk due to capacitive coupling. A grounded guard trace between signal traces will reduce crosstalk by reducing intertrace capacitance. For this same reason it is recommended that unused pins (2, 4, 6, 11) be connected to the ground plane.

"All-Hostile" crosstalk is measured by driving three of the four buffers simultaneously while observing the fourth, undriven, channel.

**Unused Buffers**

It is recommended that the inputs of any unused buffers be tied to ground through 50-Ω resistors.

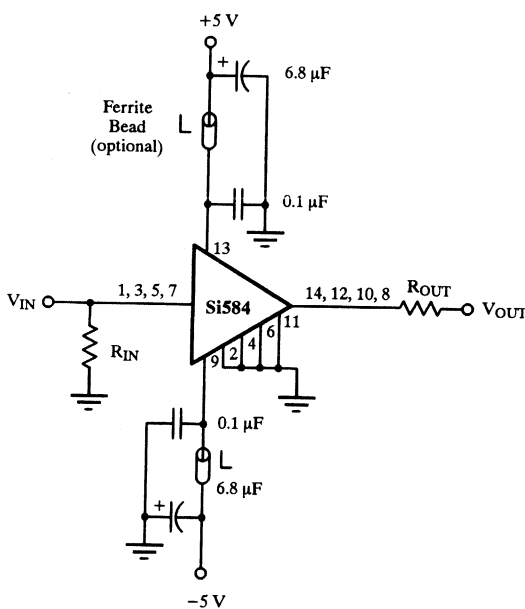


Figure 2. Decoupling the Si584

**Minimum Parts Count 80-MHz Video Switcher**

Figure 3 illustrates a fully buffered 8 × 4 video switching matrix capable of handling 80-MHz signals with only four ICs. At the heart of this circuit is the DG884 crosspoint. U1 and U2 buffer all eight inputs while U4 can drive a second level of switching elements.

## Applications (Cont'd)

It is worth noting that every time a video signal is processed by an active or passive component, its bandwidth is subject to a reduction due to each individual processing element's own bandwidth. That is why, even when switching baseband video, it is better to use a broadband switcher in order to preserve signal quality and fidelity.

For lower bandwidth applications one Si584 output can drive up to four DG884 inputs. This is useful when building larger matrices ( $8 \times 8$ ,  $8 \times 16$ , etc.).

Providing the receiving end is properly terminated, the Si584 can also be used as a cable driver for short distances. When driving long cables that may or may not be properly terminated it is better to use a back terminated cable driver with a 6-dB gain. This driving method reduces transmission line reflections. The Si584 is recommended for this type of application.

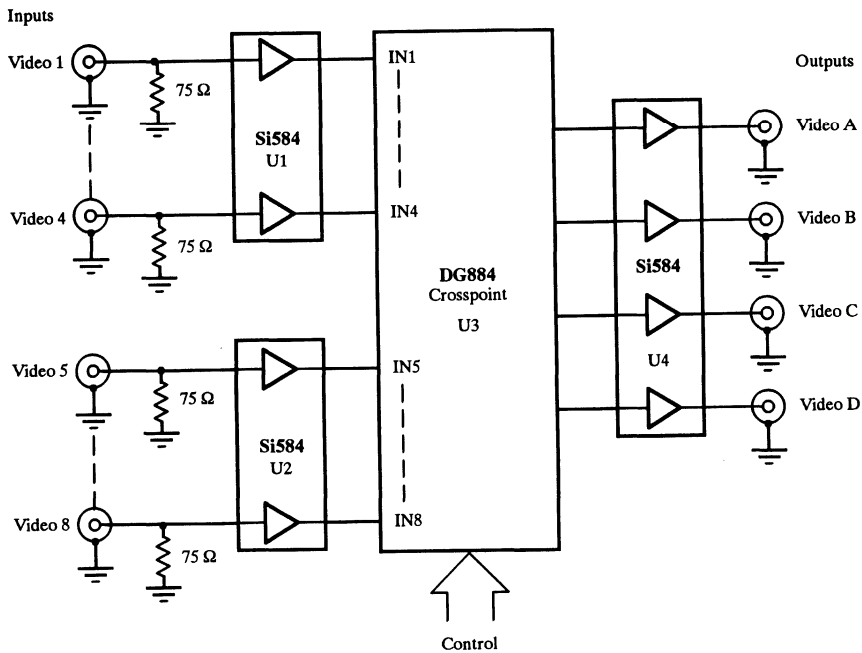


Figure 3. Minimum Parts Count 80 MHz  $8 \times 4$  Video Switching Matrix



<b>General Information</b>	<b>1</b>
<b>    Analog Switches</b>	<b>2</b>
<b>    Analog Multiplexers</b>	<b>3</b>
<b>    Wideband/Video Amplifiers</b>	<b>4</b>
<b>    Voltage Converters</b>	<b>5</b>
<b>    Appendix</b>	<b>6</b>
<b>Worldwide Sales Offices and Distributors</b>	<b>6</b>

## About Siliconix Voltage Converters

Siliconix presently supplies three types of power conversion circuits: charge pump voltage converters, high-voltage switchmode regulators, and high-voltage switchmode controllers.

Our family of low-cost switched capacitor voltage converters are used in applications where a single dc supply is available. These monolithic products feature high conversion efficiency, minimum noise and distortion, and minimum space requirements. They can be configured for voltage inversion or voltage doubling, and require only a few external components (typically two electrolytic capacitors). A typical application would be negative rail generation in a circuit with a battery supply.

The Si7660 is a voltage converter that inverts or boosts input voltages from the 1.5- to 10-V range. It features power conversion efficiencies up to 98%. The Si7661 is a higher-voltage version of the Si7660 intended for input voltages from 7.5 V to 20 V.

The high-voltage switchmode regulators and controllers made by Siliconix employ high-performance D/CMOS power IC technology to combine CMOS current-mode controllers with high-voltage input regulation and output switching. This design allows Siliconix to build extremely high efficiency switchmode power supply circuits that can run directly from high-voltage inputs such as PBX or ISDN phone lines, or 100-VAC power lines.

The data sheets for Si91xx family of switchmode regulators and controllers may be found in the *Siliconix Power Products Data Book*.

# Voltage Converters

Part Number	Max Supply Current (mA)	Min Supply Voltage (V)	Max Supply Voltage (V)	Min Output Voltage (V)	Max Output Voltage (V)	Package	Page
SI7660	0.175	1.5	10	-10	20	J, Y	4-1
SI7661	2	4.5	20	-20	40	J	4-7

J = Plastic DIP    Y = SOIC



## Switched-Capacitor Voltage Converter

### Features

- 99.7% Open Circuit Voltage Conversion Efficiency
- 98% Power Efficiency
- Operating Voltage Range of 1.5 to 10 V
- Requires Only Two Capacitors

### Benefits

- Inexpensive Negative Supply from Positive Supply
- Easy to Use
- Minimum Parts Count
- Small Size
- No Diode Drop at Output
- Low Cost

### Applications

- Conversion of 5-V Logic Supply to  $\pm 5$ -V Supplies
- Negative Supply for Dynamic RAMs
- RS-232 Power Supply
- Negative Supplies for Analog Circuits
- Data Acquisition Systems
- Hand-Held Instruments
- High-Side Load Switches

### Description

The Si7660 is a monolithic CMOS switched-capacitor voltage converter that inverts ( $V_{OUT} = -V_{IN}$ ), doubles ( $V_{OUT} = 2 V_{IN}$ ), divides ( $V_{OUT} = V_{IN}/2$ ), or multiplies ( $V_{OUT} = \pm n V_{IN}$ ) an input voltage. Operation with no external diode is guaranteed over the full temperature range for input voltages ranging from 1.5 V to 10 V.

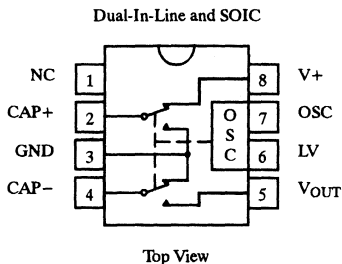
The Si7660 combines low quiescent current with high efficiency and reliability. Included on chip are an oscillator, control circuitry and four power MOS switches. An epitaxial layer prevents latchup.

The oscillator, when unloaded, runs at a nominal 12 kHz. The OSC pin may be used to change the running frequency. The LV pin should be tied to ground to improve low voltage operation ( $V^+ \leq 3.5$  V). For  $V^+ > 3.5$  V, the LV pin should be left disconnected.

Typical applications include generating a  $-5$ -V supply from a 5-V logic supply to power analog circuits, generating 6 V from a 3-V lithium cell, or 3 V from a single 1.5-V cell.

For additional information please refer to Applications Note AN401.

### Functional Block Diagram and Pin Configuration



#### Ordering Information

Temp Range	Package	Part Number
0 to 70°C	8-Pin Plastic MiniDIP	Si7660CJ
-40 to 85°C	8-Pin Plastic MiniDIP	Si7660DJ
	8-Pin Narrow SOIC	Si7660DY

## Absolute Maximum Ratings

Supply Voltage ( $V+$ to GND or GND to $V_{OUT}$ )	11 V
Oscillator Input Voltage:	
( $V+ < 5.5$ V)	-0.3 V to ( $V+$ ) +0.3 V
( $V+ > 5.5$ V)	( $V+$ ) -5.5 V to ( $V+$ ) +0.3 V
LV	No connection for $V+ > 3.5$ V
Storage Temperature	-65 to 125°C

Power Dissipation: <sup>a</sup>	
8-Pin Plastic DIP <sup>b</sup>	300 mW
8-Pin SOIC <sup>b</sup>	300 mW

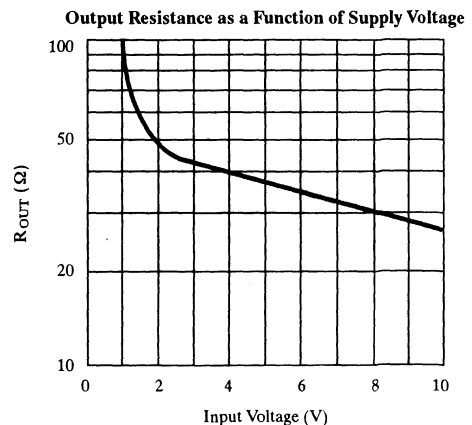
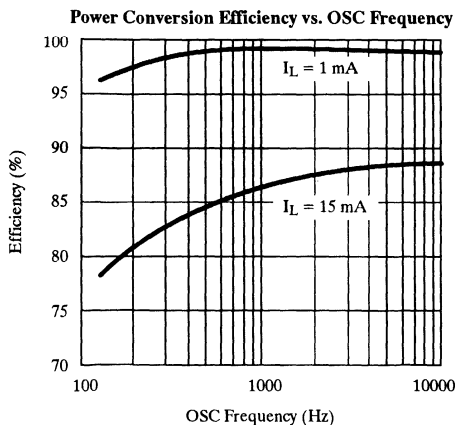
- Notes:  
a. All leads soldered or welded to PC board.  
b. Derate 10 mW/°C above 75°C

## Specifications

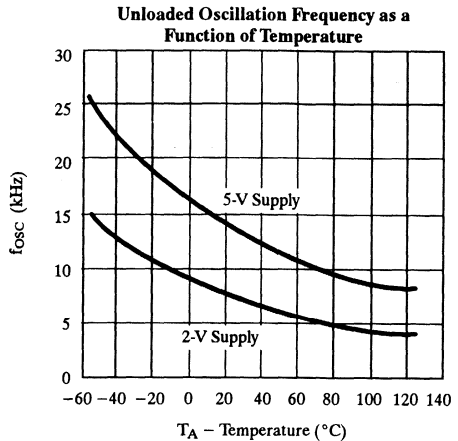
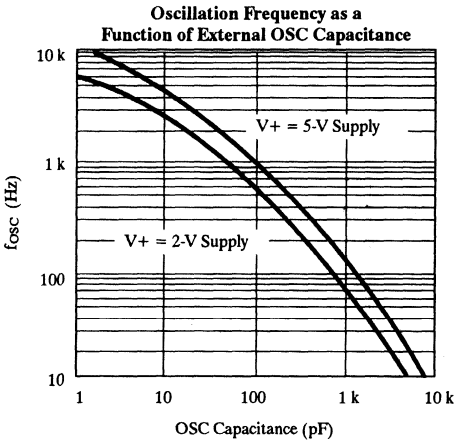
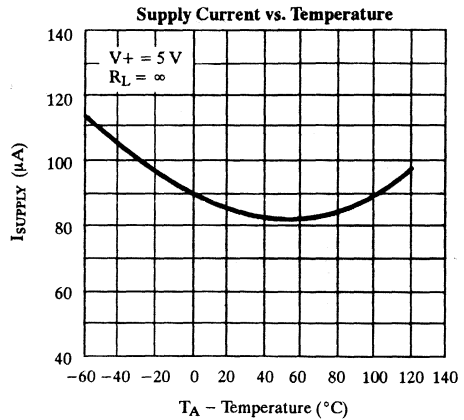
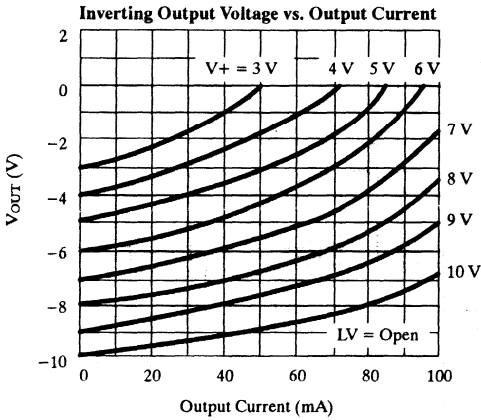
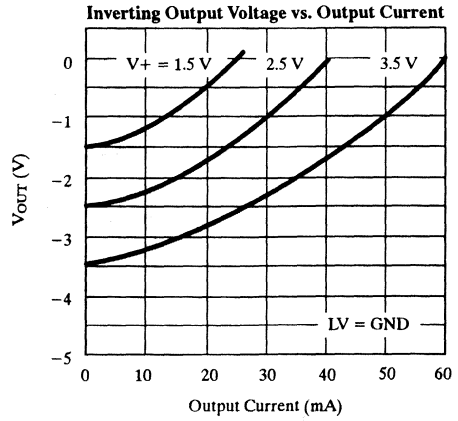
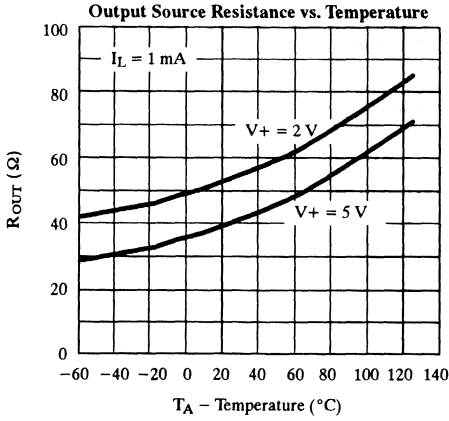
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V+ = 5$ V, $C_{OSC} = 0^d$	Temp <sup>a</sup>	Limits			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Input</b>							
Supply Voltage Range Low	$V+L$	$R_L = 10$ k $\Omega$ , LV = GND	Full	1.5		3.5	V
Supply Voltage Range High	$V+H$	$R_L = 10$ k $\Omega$ , LV = Open	Full	3		10	
Supply Current	I+	$R_L = \infty$ , LV = Open	Full		100	175	$\mu$ A
<b>Output</b>							
Output Source Resistance	$R_{OUT}$	$V+ = 5$ V, LV = Open, $I_O = 20$ mA	Room Full		55	100 120	$\Omega$
		$V+ = 2$ V, LV = GND, $I_O = 3$ mA	Full			300	
Power Conversion Efficiency	$PE_1$	$R_L = 5$ k $\Omega$	Room	95	98		%
Voltage Conversion Efficiency	$V_{OUT}E_1$	$R_L = \infty$	Room	99	99.9		
<b>Dynamic</b>							
Oscillator Frequency <sup>d</sup>	$f_{OSC}$		Room		12		kHz
Oscillator Impedance	$Z_{OSC}$	$V+ = 2$ V, LV = GND	Room		1		M $\Omega$
		$V+ = 5$ V	Room		100		k $\Omega$

- Notes:  
a. Room = 25°C, Full = as determined by the operating temperature suffix.  
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.  
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
d. For  $C_{OSC} > 1000$  pF,  $C_1$  and  $C_2$  should be increased to 100  $\mu$ F.  $C_1$  = Pump Capacitor,  $C_2$  = Reservoir Capacitor.

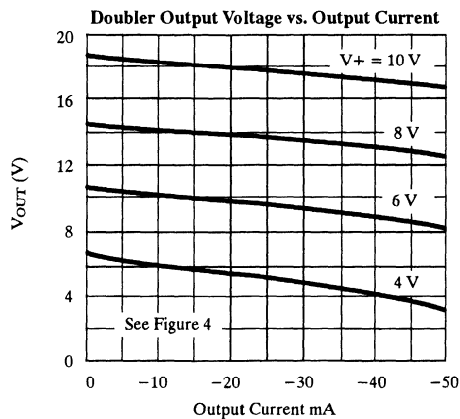
## Typical Characteristics



**Typical Characteristics (Cont'd)**



## Typical Characteristics (Cont'd)



## Schematic Diagram

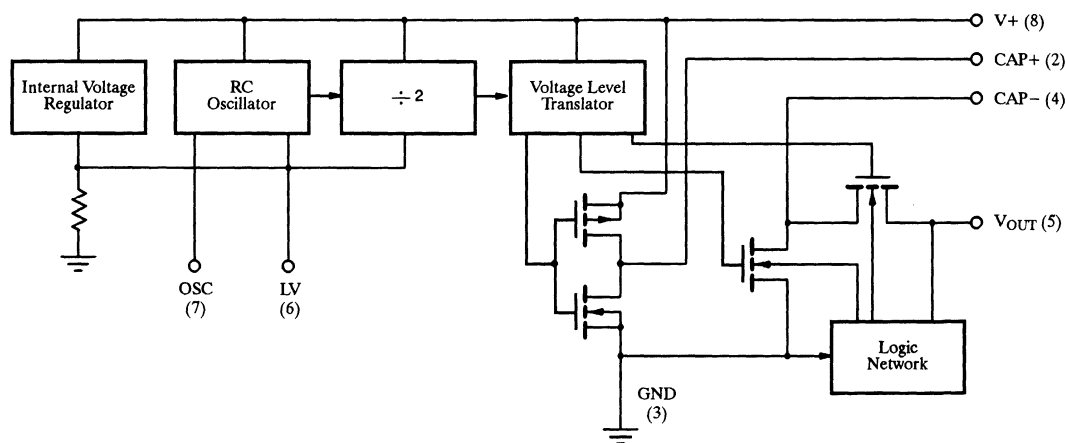


Figure 1.

## Test Circuit

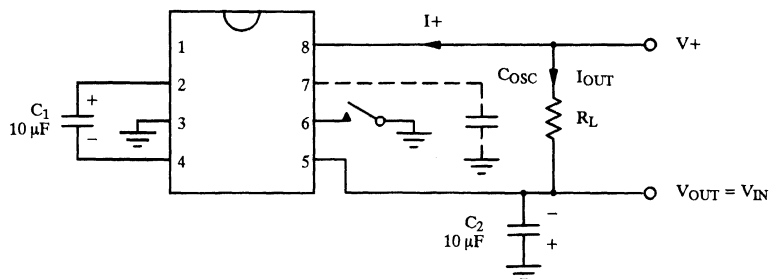


Figure 2.



**Applications**

There are many applications where a low current supply made with a charge pump does just as well as a conventional, fully regulated negative supply or dc-to-dc converter module. The Si7660 contains all the circuitry necessary to make a charge pump for voltage inversion, doubling, division, multiplication, etc. Only two external capacitors are needed and they may be inexpensive electrolytics. Since the output resistance is in the tens of ohms, heavy load currents will reduce the output voltage and eventually may cause the device to go into shutdown.

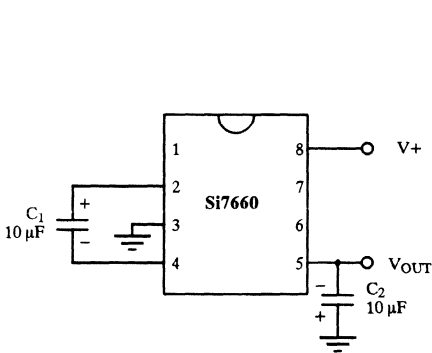
If the output ripple of the Si7660 is too great for a particular application, the value of the pump ( $C_1$ , Figure 3) and reservoir ( $C_2$ , Figure 3) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of

the device can be exceeded. The maximum recommended capacitor size is 1000  $\mu\text{F}$ .

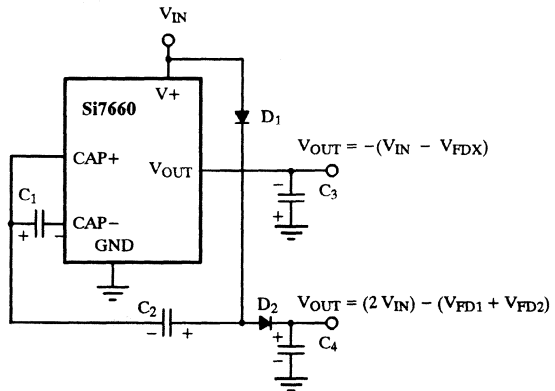
A previous version of the Si7660 required a diode in series with Pin 5 when operating above 6.5 V. The current Si7660 does not require this diode, but will work in existing circuits which have the diode.

Figure 4 shows a circuit that will produce two output voltages utilizing both of the Si7660 features (i.e. inversion and doubling). The combined output current must be limited so the maximum device dissipation is not exceeded.

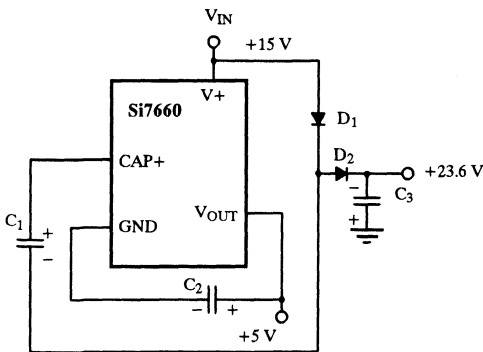
Two Si7660s can be paralleled to reduce the effective output resistance of the converter. The output voltage at a given current is increased since the voltage drop is halved when the devices are connected as shown in Figure 6.



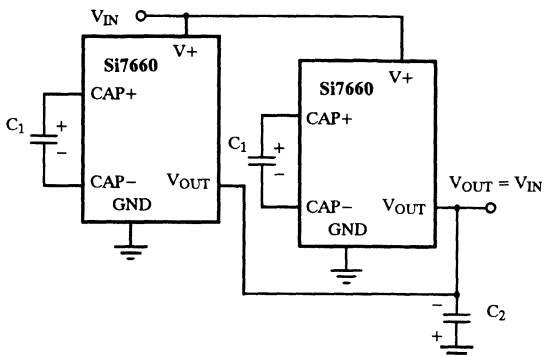
**Figure 3.** Basic Inverter Circuit



**Figure 4.** Combination Inverter/Doubler Circuit



**Figure 5.** Creating +23.6 V from +15 V and +5 V



**Figure 6.** Paralleling Two Si7660s to Reduce the Effective Output Resistance

## Applications (Cont'd)

### Battery Splitter

To obtain supplies from a single battery or power supply, the circuit shown in Figure 7 offers a simple solution. It generates symmetrical  $\pm$  output voltages equal to one-half the input voltage. Both output voltages are referenced to Pin 3 (output common). To improve low voltage operation, Pin 6 should be connected to Pin 3 when the input voltage is less than 3.5 V.

### High Precision Voltage Divider

A high precision voltage divider is shown in Figure 8. Increasing the load current beyond 100 nA will cause a small loss in accuracy.

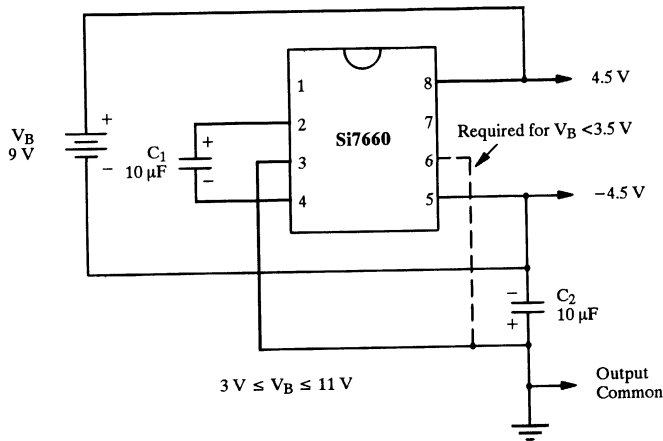


Figure 7. Battery Splitter

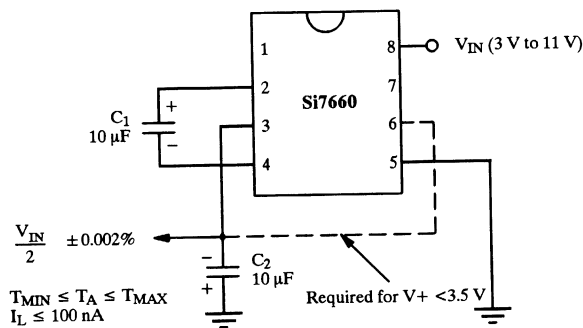


Figure 8. High Precision Voltage Divider

## Switched-Capacitor Voltage Converter

### Features

- Wide Operating Supply Voltage Range: 4.5 V to 20 V
- 99.7% Open Circuit Voltage Conversion Efficiency
- 95% Power Conversion Efficiency

### Benefits

- Inexpensive Negative Supply Generation
- Easy to Use, Requires Only Two External Capacitors
- Minimum Parts Count
- Small Size

### Applications

- Conversion of +12-V to  $\pm 12$ -V Supplies
- RS-232 Power Supply
- Negative Supplies for Analog Circuits
- Data Acquisition Systems
- Handheld Instruments
- High-Side Load Switches

### Description

The Si7661 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The Si7661 performs a supply voltage conversion from positive to negative for an input range of +4.5 V to +20 V, resulting in a complementary output voltage of -4.5 V to -20 V with the addition of only two capacitors.

Typical applications for the Si7661 are data acquisition and microprocessor based systems, where a +5- to +20-V supply is available for the digital functions, and an additional -5- to -20-V supply is required for analog devices, such as op amps. The Si7661 is also ideally suited for providing low current, -5-V body bias supply for dynamic RAMs.

oscillator, voltage level translator, four power MOS switches, and a logic network. This logic network senses the most negative voltage in the device and ensures that the output n-channel switch substrates are not forward-biased. An epitaxial layer prevents latchup.

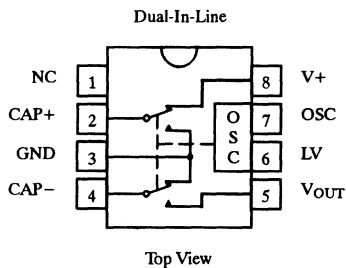
The oscillator, when unloaded, runs at a nominal frequency of 10 kHz for an input supply voltage of 4.5 to 20 V. The "OSC" terminal may be connected to an external capacitor to lower the frequency or it may be driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal regulator and improve low voltage (LV) operation. At high voltages (+8 to +20 V), the "LV" pin should be left disconnected.

Contained on the chip are a voltage regulator, RC

For applications information refer to AN401.

### Functional Block Diagram and Pin Configuration



#### Ordering Information

Temp Range	Package	Part Number
0 to 70°C	8-Pin Plastic MiniDIP	Si7661CJ
-40 to 85°C		Si7661DJ

## Absolute Maximum Ratings

Supply Voltage (V+ to GND or GND to V<sub>OUT</sub>) ..... 22 V  
 Oscillator Input Voltage  
 V+ < 8 V ..... -0.3 V to (V+) + 0.3 V  
 V+ > 8 V ..... (V+) - 8 V to (V+) + 0.2 V  
 LV ..... No connection for V+ > 9 V  
 Storage Temperature ..... -65 to 125°C

Power Dissipation:<sup>a</sup>  
 8-Pin Plastic MiniDIP<sup>b</sup> ..... 500 mW

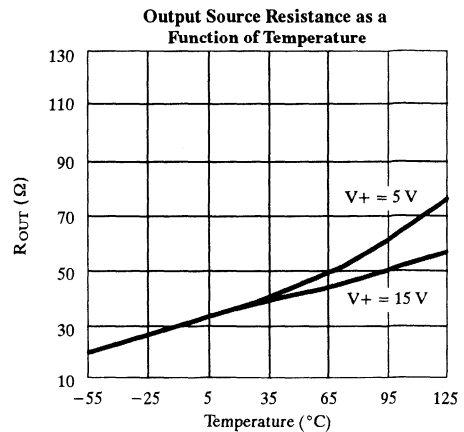
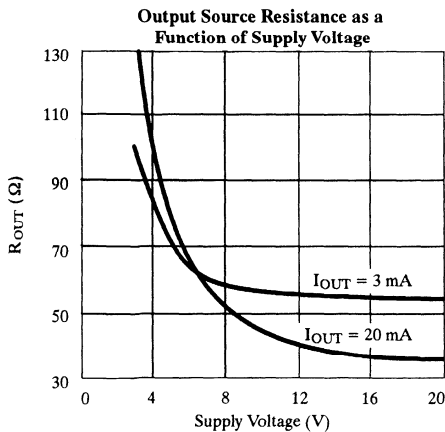
Notes:  
 a. All leads welded or soldered to PC board.  
 b. Derate 6.6 mW/°C above 25°C.

## Specifications

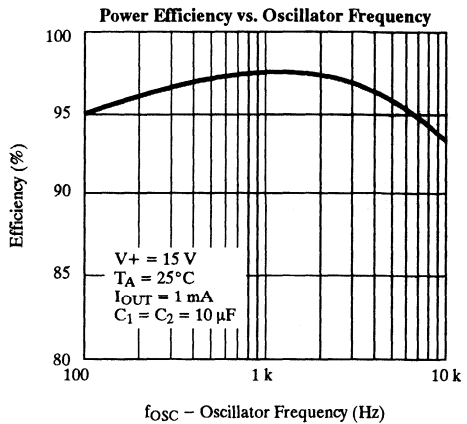
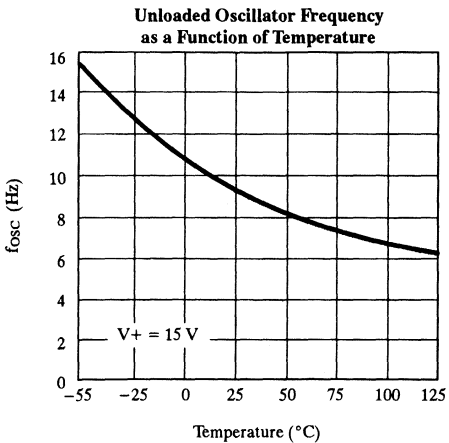
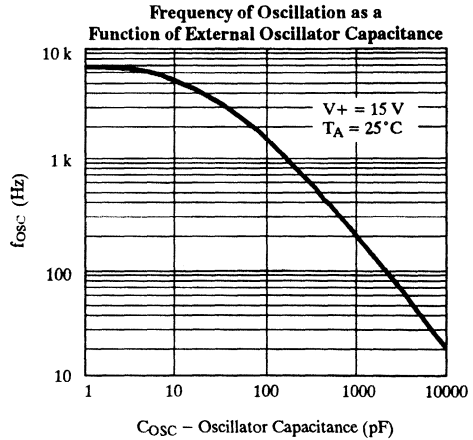
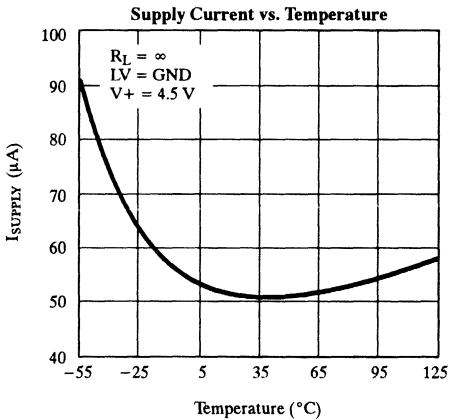
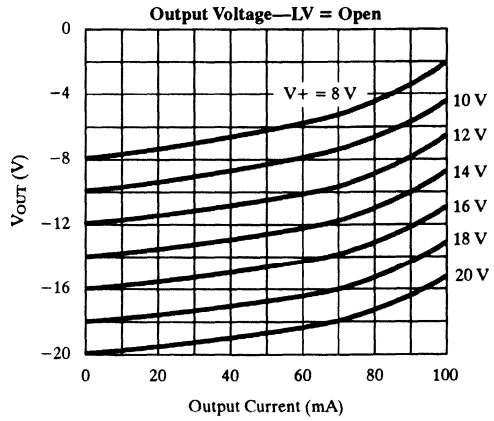
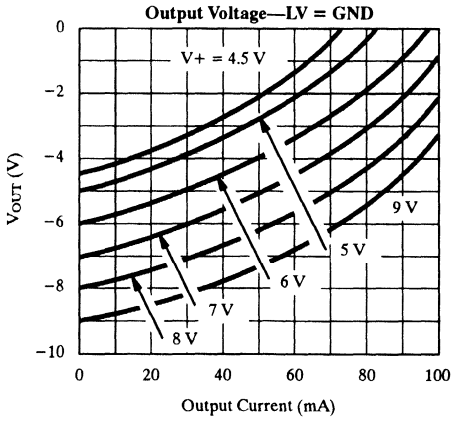
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, C <sub>OSC</sub> = 0 <sup>d</sup>	Temp <sup>a</sup>	Limits			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Input</b>							
Supply Voltage Range Low	V <sub>L</sub>	R <sub>L</sub> = 10 kΩ, LV = GND	Full	4.5		9	V
Supply Voltage Range High	V <sub>H</sub>	R <sub>L</sub> = 10 kΩ, LV = Open	Full	8		20	
Supply Current	I+	V+ = 4.5 V, R <sub>L</sub> = ∞, LV = GND	Full		100	200	μA
		V+ = 15 V, R <sub>L</sub> = ∞, LV = Open	Full		0.7	2	mA
<b>Output</b>							
Output Source Resistance	R <sub>OUT</sub>	V+ = 4.5 V, LV = GND, I <sub>OUT</sub> = 3 mA	Room		35		Ω
		V+ = 15 V, LV = Open, I <sub>OUT</sub> = 20 mA	Room		30	100	
			Full			120	
Power Conversion Efficiency	P <sub>EF</sub>	V+ = 15 V, R <sub>L</sub> = 2 kΩ	Room		92		%
Voltage Conversion Efficiency	V <sub>EF</sub>	V+ = 15 V, R <sub>L</sub> = ∞	Room	97	99.7		
<b>Dynamic</b>							
Oscillator Frequency <sup>d</sup>	f <sub>OSC</sub>	V+ = 15 V	Room		10		kHz
Oscillator Impedance	Z <sub>OSC</sub>	V+ = 4.5 V, LV = GND	Room		1		MΩ
		V+ = 15 V	Room		100		kΩ

- Notes:  
 a. Room = 25°C, Full = as determined by the operating temperature suffix.  
 b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.  
 c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
 d. For C<sub>OSC</sub> > 1000 pF, C<sub>1</sub> and C<sub>2</sub> should be increased to 100 μF. C<sub>1</sub> = Pump Capacitor, C<sub>2</sub> = Reservoir Capacitor.

## Typical Characteristics



**Typical Characteristics (Cont'd)**



## Schematic Diagram

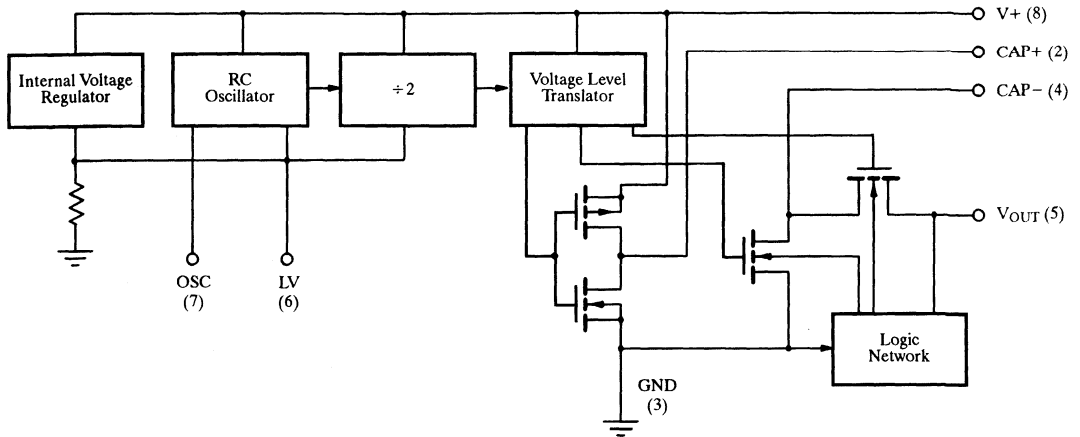


Figure 1.

## Test Circuit

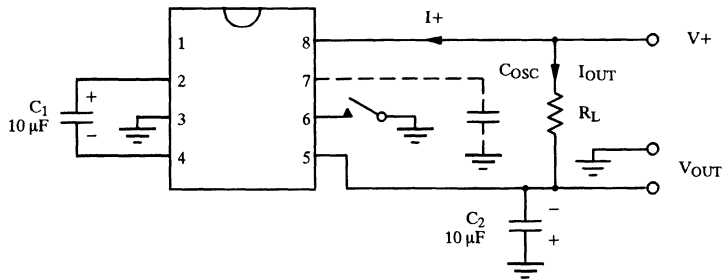


Figure 2.

## Applications

The Si7661 contains all the circuitry necessary to make a charge pump for voltage inversion, doubling, division, multiplication, etc. Only two external capacitors are needed and they may be inexpensive electrolytics. Since the output resistance is in the tens of ohms, heavy load currents will reduce the output voltage and eventually may cause the device to go into shutdown.

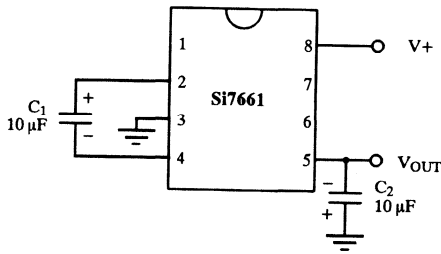
There are many applications where a low current supply made with a charge pump does just as well as a conventional, fully regulated negative supply or dc-to-dc converter module. Some examples are negative power supplies for microprocessors, dynamic RAMs, or data acquisition systems. In addition, the extended input voltage range of the Si7661 lends itself for use as a negative generator for most op-amp applications.

**Applications (Cont'd)**

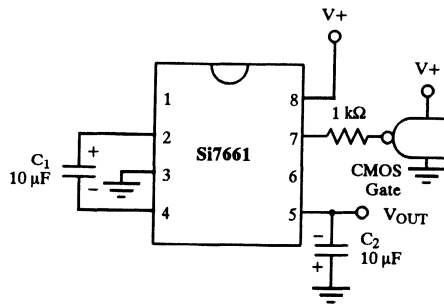
If the output ripple of the Si7661 is too great for a particular application, the value of the pump ( $C_1$ , Figure 3) and reservoir ( $C_2$ ) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded, causing destruction of the device. The maximum recommended capacitor size is 1000  $\mu\text{F}$ .

When an external clock is used to drive the Si7661 a 1-k $\Omega$  resistor should be used between the clock source and the OSC input (Pin 7) as shown in Figure 4.

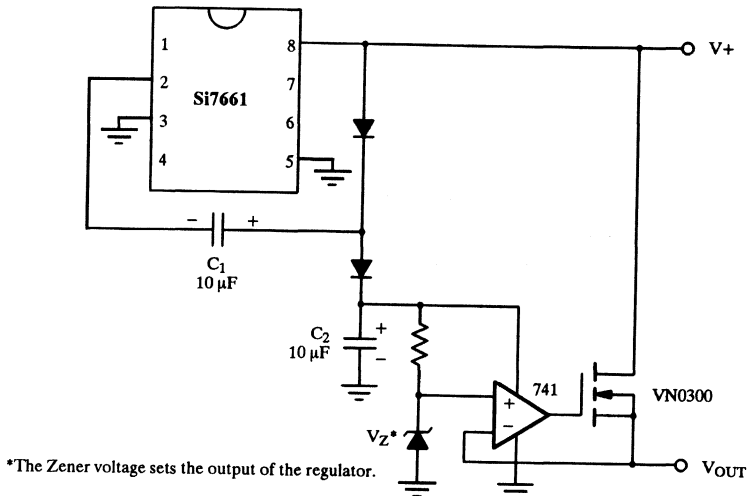
Figure 5 shows a regulator that will operate with much less than 1-V drop between  $V_+$  and  $V_{OUT}$  at large output currents. Most three-terminal voltage regulators would exhibit a drop of a volt or more under these conditions.



**Figure 3.** Basic Inverter Circuit



**Figure 4.** Driving the Si7661 with an External Clock



\*The Zener voltage sets the output of the regulator.

**Figure 5.** Low Loss Regulator Circuit

## Applications (Cont'd)

### Battery Splitter

To obtain supplies from a single battery or power supply, the circuit shown in Figure 6 offers a simple solution. It generates symmetrical  $\pm$  output voltages equal to one-half the input voltage. Both output voltages are referenced to Pin 3 (output common). To improve low-voltage operation, Pin 6 should be connected to Pin 3 when the input voltage is less than 9 V.

### High Precision Voltage Divider

A high precision voltage divider is shown in Figure 7. Increasing the load current beyond 100 nA will cause a small loss in accuracy.

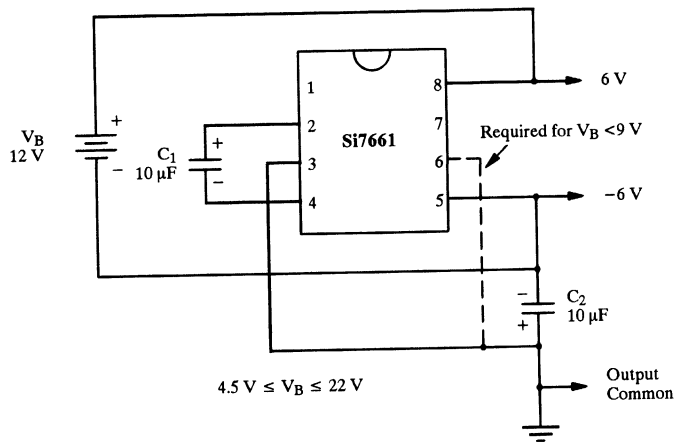


Figure 6. Battery Splitter

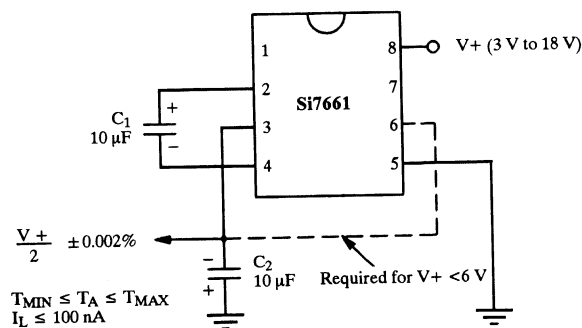


Figure 7. High Precision Voltage Divider



<b>General Information</b>	<b>1</b>
<b>Analog Switches</b>	<b>2</b>
<b>Analog Multiplexers</b>	<b>3</b>
<b>Wideband/Video Amplifiers</b>	<b>4</b>
<b>Voltage Converters</b>	<b>5</b>
<b>Appendix</b>	<b>6</b>
<b>Worldwide Sales Offices and Distributors</b>	<b>6</b>



The following literature is designed to help you use Siliconix products in your applications. Call our FaxBack system (408-970-5600) to have the document sent to you immediately via facsimile, or to order a copy to be sent by mail, call 800-554-5565.

Application Note Number	FaxBack Code Number	Title
<b>Analog Switches and Multiplexers</b>		
TA201	9201	High-Performance Multiplexing with the DG408
AN203	9203	Silicon-Gate Switching Functions Optimize Data Acquisition Front Ends
AN204	9204	Serially-Controlled Eight-Channel Analog Switch Array Simplifies Signal Conditioning and Routing
AN205	9205	Overvoltage Protection for CMOS Switches and Multiplexers
AN206	9206	DG406 Multiplexer Optimizes Medical Simulator
AN207	9207	15-ns DG611 Switch Family Combines Benefits of CMOS and DMOS Technologies
<b>DMOS</b>		
AN301	9301	DMOS FET Analog Switches and Switch Arrays
<b>JFETs</b>		
AN101	9101	An Introduction to FETs
AN102	9102	FET Biasing
AN103	9103	The FET Constant-Current Source
AN104	9104	SPICE Parameters for Select JFETs
AN105	9105	FETs As Voltage-Controlled Resistors
<b>LITTLE FOOT® MOSFETs</b>		
AN801	8801	Designing with Complementary Power MOSFETs in Surface-Mount (SO-8) Packages
AN802	8802	Low-Voltage Motor Drive Designs Using N-Channel Dual MOSFETs in Surface-Mount Packages
AN803	8803	Thermal Characteristics of Siliconix's LITTLE FOOT Family of Surface-Mount MOSFETs
AN804	8804	P-Channel MOSFETs, the Best Choice for High-Side Switching
<b>Low-Power FETs</b>		
AN901	8901	Depletion-Mode MOSFETs Expand Circuit Opportunities
<b>Power MOSFETs</b>		
AN601	8601	Unclamped Inductive Switching Rugged MOSFETs for Rugged Environments
<b>Power ICs</b>		
AN701	8701	A 1-Watt Flyback Converter Using the Si9100
AN702	8702	Efficient ISDN Power Converters Using the Si9100
AN703	8703	Designing DC/DC Converters with the Si9110 Switchmode Controller
AN704	8704	Designing DC/DC Converters to Meet CCITT Specifications for ISDN Terminals
AN705	8705	The Si9910 Adaptive Power MOSFET Driver Improves Performance in High-Voltage Half-Bridge Applications
AN706	8706	Motor Drive Circuits Using the D469A
AN707	8707	Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC
AN708	8708	Low-Power Universal-Input Power Supply Achieves High Efficiency
AN709	8709	Designing with the Si9976DY N-Channel Half-Bridge Driver and LITTLE FOOT Dual MOSFETs
AN710	8710	High-Efficiency Buck Converter for Notebook Computers
AN711	8711	HDD Servo Design Using the Si9990CS
AN712	8712	A High-Voltage Half-Bridge Using the Si9901 with the Si9911 or Si9914
<b>Video ICs</b>		
AN501	9501	The DG535/536 Wideband Multiplexers Suit a Wide Variety of Applications
AN502	9502	Microprocessor-Compatible Multiplexers Facilitate Video Switching Designs
AN503	9503	Si581 Wideband Buffer Applications
AN504	9504	Video Crosspoint Switch Simplifies Large Matrix Designs
<b>Voltage Converters</b>		
AN401	9401	Theory and Applications of the Si7660 and Si7661 Voltage Converters

## Introduction

Reliability at Siliconix is ensured with two primary programs: the Reliability Qualification Program and the Reliability Monitoring Program. Siliconix publishes this data by product family and it can be obtained by request through your local sales office.

## Qualification Program

Qualification programs of accelerated stress testing are developed for the introduction of new devices (die qualifications), packages, major process changes, new materials or suppliers, new manufacturing equipment, and new manufacturing locations.

A qualification starts after a qualification test plan is developed. This plan specifies the following:

- Purpose and scope
- Device or geometry types and packages being qualified
- Process and assembly specs involved
- Test vehicles and location
- Tests and stresses
- Duration of each stress
- Sample sizes
- Acceptance criteria
- Number of lots required

## Monitoring Program

The Reliability Monitoring Program, which includes accelerated life tests, is designed to continuously monitor product reliability. The program furnishes up-to-date failure-rate and failure-mechanism data which can be used to predict and improve long-term reliability performance. The Monitoring Program covers a wide range of technologies and product lines manufactured by Siliconix. In order to accomplish this, products are grouped by similar technologies. For example, components built in the same wafer fab, using the same manufacturing processes, having similar complexity, functionality, and package types are grouped into a technology family. One component or more representing each technology group is monitored according to a quarterly schedule. An internal Reliability Performance Monitor report is issued monthly and is reviewed by all engineering groups to ensure improvement of product reliability.

The short-term and long-term monitor tests are outlined in Tables 1 and 2. Also, the Reliability Monitor Program is

summarized in general outline form as a flow chart in Figure 1 and with operating life data in Table 3.

## Accelerated Reliability

Accelerated tests were developed to shorten the time required for reliability testing. The life cycle of a component is accelerated by applying stress that is more severe than that encountered under normal operating conditions. This acceleration is produced by elevating temperatures, increasing humidity or pressure, alternating hot and cold temperature, switching power on and off, or some combination of these conditions. The test results are used to predict normal operating performance. In the sections below we present a brief description of each stress.

## Summary of Tests

### High Temperature Operating Life

The high-temperature operating life accelerated test, commonly referred to as "burn-in," is performed at typically 125°C and 150°C under electrical bias.

The steady state and dynamic life tests determine the ability of a product to survive a host of potential failure modes, surface inversion, dielectric breakdown, and electromigration being typical examples.

### Temperature Cycling Test

Temperature cycling exploits the differences in thermal coefficients of expansion between silicon and the other materials used in die fabrication and packaging. Each cycle consists of 10-minute exposures at -65°C and 150°C with a 1-minute transfer at room temperature between the temperature extremes. This test reveals potential weaknesses in die and package materials and construction and in the integration of the die and package.

### Thermal Shock Test

The purpose of the thermal shock test is similar to that of temperature cycling. This stress is more extreme, however, due to the fact that the ambient medium is liquid and not air, and the transition time is much shorter than for temperature cycling.

Each cycle consists of a 5-minute exposure at -65°C and 150°C with a maximum 10-second transfer time between the temperature extremes.

# Reliability Information

## Bias Humidity Test

The bias humidity test is used to test plastic packaged devices for the effects of moisture penetration while electrical potentials are applied. The components are placed in a biased condition and then are subjected for 1000 hours to a temperature of 85°C and a relative humidity 85%. This test confirms package integrity.

## Pressure Pot Test

In the pressure pot test, water vapor is forced into non-hermetic packages via micro gaps in the package-lead seal. Water is then carried to the die surface via capillary action of the bond wires. Electrical leakage may result. External contamination of the package or lead finish may be transported to the die or may directly cause corrosion of the leads.

**Table 1. Short-Term Reliability Monitor**

Test	Condition	Sample Size	Test Points
Static Operating Life	125°C or 150°C	50	168 hours
Dynamic Operating Life			48 hours (Plastic)
Pressure Pot	121°C, 15 PSIG		100 cycles
Thermal Shock	Liquid to liquid. -65°C to 150°C		(245°C ± 5°C)
Solderability	MIL-STD-883D, M2003	15 leads	(Hermetic)
Lead Integrity	MIL-STD-883D, M2004		
Lid Torque	MIL-STD-883D, M2024		
Marking Permanency	MIL-STD-883D, M2015	16 leads	
Salt Atmosphere	MIL-STD-883D, M1009	15 leads	24 hours (Hermetic)
ESD, Human Body Model	MIL-STD-883D, M3015	12 leads	

**Table 2. Long-Term Reliability Monitor**

Test	Condition	Sample Size	Test Points
Static Operating Life	125°C or 150°C	50	0, 168, 1000 hours
Dynamic Operating Life			0, 500, 1000 hours
Biased Humidity (Plastic)	85°C, 85% relative humidity		0, 250, 1000 cycles
Temperature Cycling	Air-to-air -65°C to 150°C		0, 2000, 6000 cycles
Power Cycling	$\Delta T_j = 100^\circ\text{C}$	30	

**Table 3.**

High Temperature Operating Life Technology	Number of Units	Equivalent Device Hours at 55°C and 1.0 eV	FTTs <sup>a</sup> at 60% CL <sup>b</sup>
Metal-Gate, HVMG	5605	4,618,752,555	0.43
Silicon-Gate, HVSG	4787	3,569,237,924	0.25

**Notes:**

- a. 1 failure per billion device hours
- b. Confidence Level

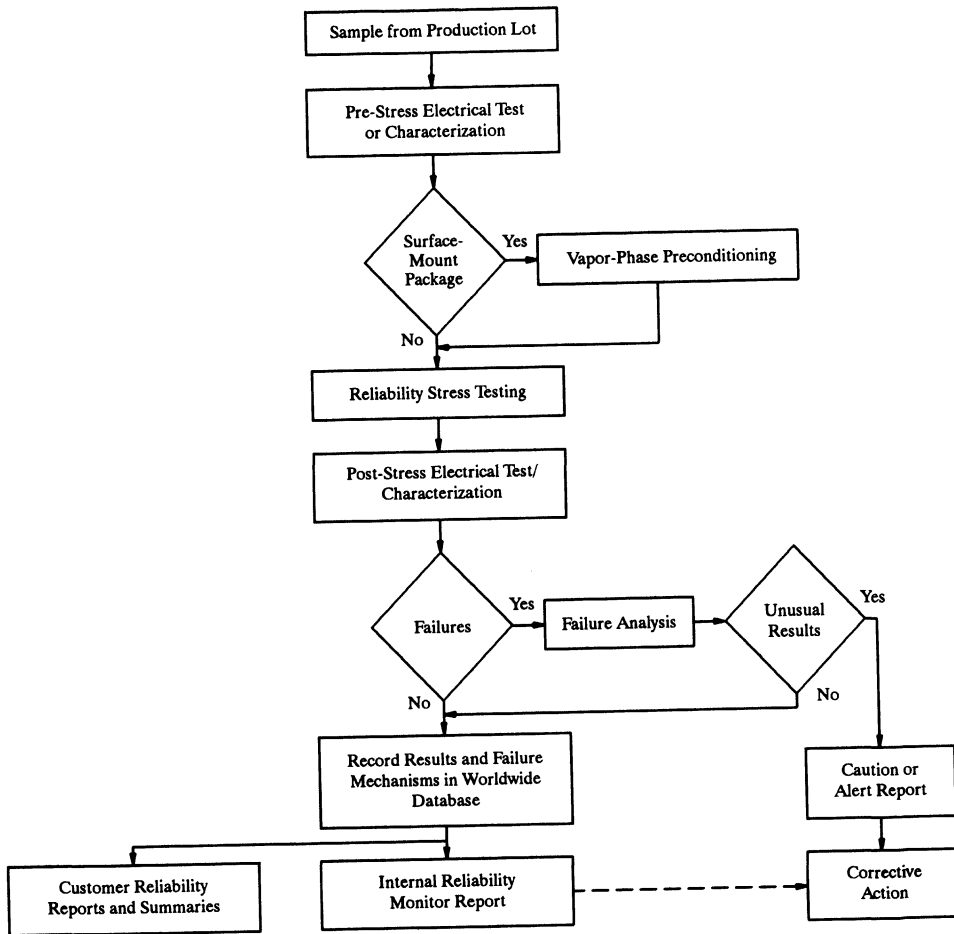
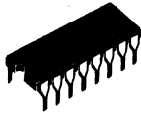
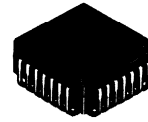


Figure 1. Reliability Monitor Flow (Short- and Long-Term Monitors)

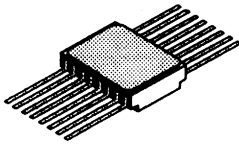
# Package Information



**CerDIP**  
8- to 16-Pin



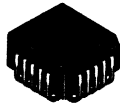
**CerQuad**  
28- and 44-Pin



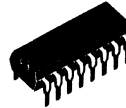
**Flatpak**  
14- and 16-Pin



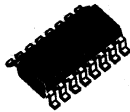
**LCC**  
20- to 28-Pin



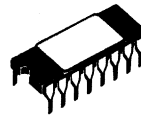
**PLCC**  
20- to 44-Pin



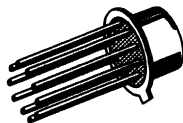
**Plastic DIP**  
8- to 20-Pin



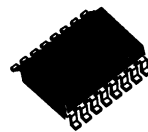
**SOIC**  
8- to 16-Pin



**Sidebrazed Ceramic**  
14- to 24-Pin



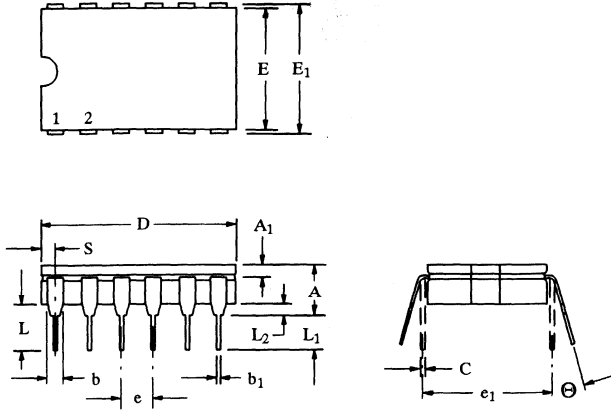
**TO-100 Metal Can**  
10-Pin



**Wide-Body SOIC**  
16- to 28-Pin

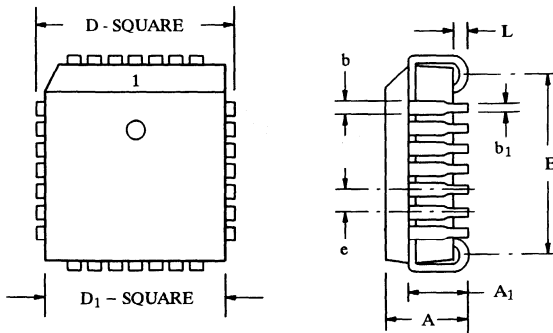
# Package Information

## ■ CerDIP, 8- to 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A <sub>1</sub>	1.27	2.16	0.050	0.085
b	1.14	1.65	0.045	0.065
b <sub>1</sub>	0.38	0.51	0.015	0.020
C	0.20	0.30	0.008	0.012
D-8	9.40	10.16	0.370	0.400
D-14	19.05	19.56	0.750	0.770
D-16	19.05	19.56	0.750	0.770
E	6.60	7.62	0.260	0.300
E <sub>1</sub>	7.62	8.26	0.300	0.325
e	2.54 BSC		0.100 BSC	
e <sub>1</sub>	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L <sub>1</sub>	3.18	3.81	0.125	0.150
L <sub>2</sub>	0.51	1.14	0.020	0.045
S-8	0.64	1.52	0.025	0.060
S-14	1.65	2.41	0.065	0.095
S-16	0.38	1.14	0.015	0.045
Θ	0°	15°	0°	15°

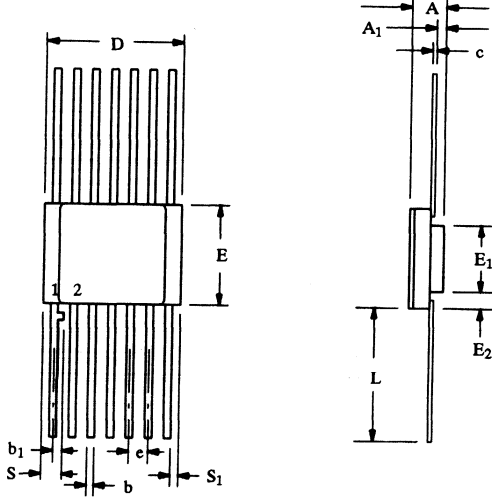
## ■ CerQuad Package, 28- and 44-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.20	4.83	0.165	0.190
A <sub>1</sub>	2.29	3.04	0.090	0.120
b	0.66	0.81	0.026	0.032
b <sub>1</sub>	0.46	0.56	0.018	0.022
D-28	12.32	12.57	0.485	0.495
D-44	17.40	17.65	0.685	0.695
D <sub>1</sub> -28	11.23	11.63	0.442	0.458
D <sub>1</sub> -44	16.31	16.71	0.642	0.658
E-28	9.91	10.92	0.390	0.430
E-44	14.99	16.00	0.590	0.630
e	1.27 BSC		0.050 BSC	
L	0.51	-	0.020	-

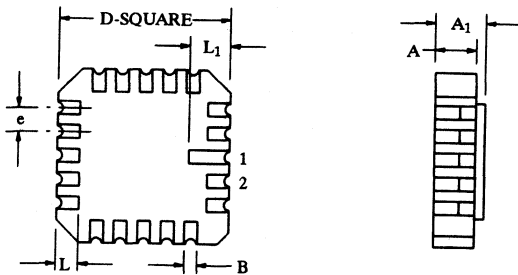


## ■ Flat Package, 14- and 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.03	2.54	0.080	0.100
A <sub>1</sub>	0.66	1.14	0.026	0.045
b	0.38	0.48	0.015	0.019
b <sub>1</sub>	0.20	0.38	0.008	0.015
c	0.10	0.15	0.004	0.006
D-14	8.64	9.14	0.340	0.360
D-16	9.91	10.41	0.390	0.410
E-14	6.10	6.60	0.240	0.260
E-16	6.60	7.11	0.260	0.280
E <sub>1</sub>	4.45	4.95	0.175	0.195
E <sub>2</sub>	0.76	1.27	0.030	0.050
e	1.27 BSC		0.050 BSC	
L	7.62	8.89	0.300	0.350
S	-	1.14	-	0.045
S <sub>1</sub>	0.13	-	0.005	-

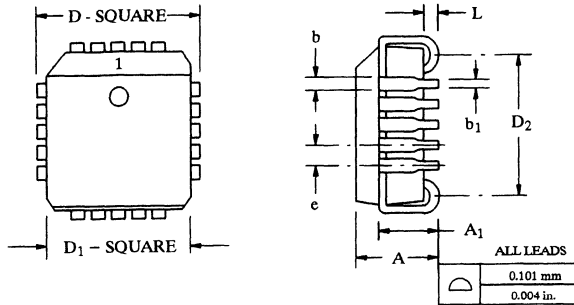
## ■ LCC, 20- to 28-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A <sub>1</sub>	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D-20	8.69	9.09	0.342	0.358
D-28	11.23	11.63	0.442	0.458
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L <sub>1</sub>	1.96	2.36	0.077	0.093

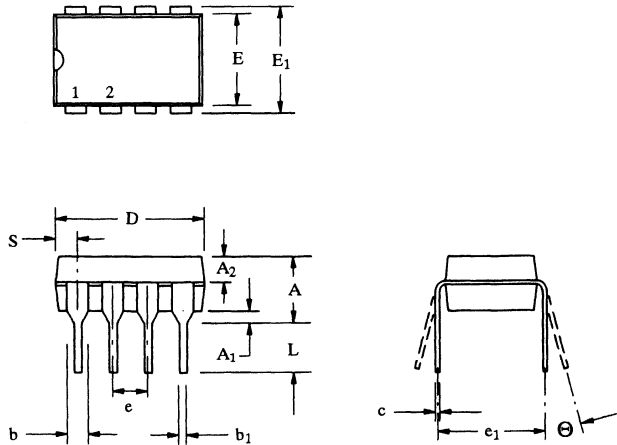
# Package Information

## ■ PLCC, 20- to 44-Pin



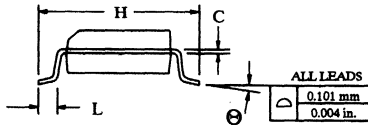
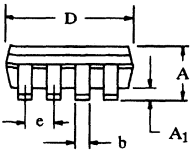
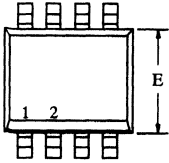
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A <sub>1</sub>	2.29	3.04	0.090	0.120
b	0.66	0.81	0.026	0.032
b <sub>1</sub>	0.33	0.55	0.013	0.021
D-20	9.78	10.03	0.385	0.395
D-28	12.32	12.57	0.485	0.495
D-44	17.40	17.65	0.685	0.695
D <sub>1</sub> -20	8.89	9.04	0.350	0.356
D <sub>1</sub> -28	11.43	11.58	0.450	0.456
D <sub>1</sub> -44	16.51	16.66	0.650	0.656
D <sub>2</sub> -20	7.37	8.38	0.290	0.330
D <sub>2</sub> -28	9.91	10.92	0.390	0.430
D <sub>2</sub> -44	14.99	16.00	0.590	0.630
e	1.27 BSC		0.050 BSC	
L	0.51	-	0.020	-

## ■ Plastic DIP, 8- to 20-Pin



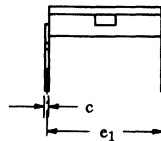
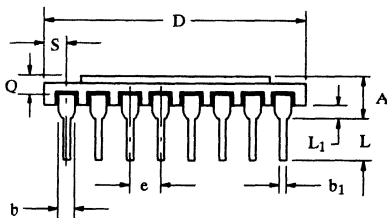
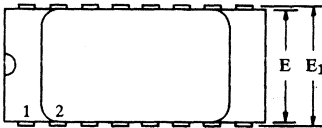
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A <sub>1</sub>	0.38	1.27	0.015	0.050
A <sub>2</sub>	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b <sub>1</sub>	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.65	11.68	0.380	0.460
D-14	17.27	19.30	0.680	0.760
D-16	18.93	21.33	0.745	0.840
D-20	24.89	26.92	0.980	1.060
E	5.59	7.11	0.220	0.280
E <sub>1</sub>	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e <sub>1</sub>	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
S-14	1.02	2.03	0.040	0.080
S-16	0.38	1.52	0.015	0.060
S-20	1.02	2.03	0.040	0.080
$\Theta$	0°	15°	0°	15°

## ■ SOIC, 8- to 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
C	0.18	0.23	0.007	0.009
D-8	4.69	5.00	0.185	0.196
D-14	8.55	8.75	0.336	0.344
D-16	9.80	10.00	0.385	0.393
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

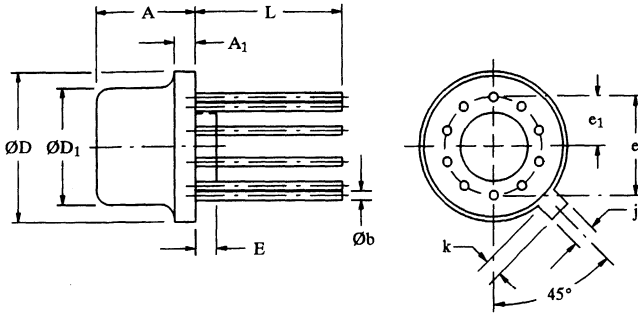
## ■ Sidebrazed Ceramic, 14- to 24-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.67	4.44	0.105	0.175
b	0.97	1.52	0.038	0.060
b <sub>1</sub>	0.38	0.53	0.015	0.021
c	0.20	0.30	0.008	0.012
D-14	17.53	19.55	0.690	0.770
D-16	19.56	21.08	0.770	0.830
D-20	24.89	26.16	0.890	1.030
D-24	29.97	31.24	1.180	1.230
E	7.12	7.87	0.280	0.310
E <sub>1</sub>	7.37	8.25	0.290	0.325
e	2.54 BSC		0.100 BSC	
e <sub>1</sub>	7.62 BSC		0.300 BSC	
L	3.18	4.44	0.125	0.175
L <sub>1</sub>	0.64	1.39	0.025	0.055
Q	0.25	-	0.010	-
S-14	0.77	2.41	0.030	0.095
S-16	0.51	1.65	0.020	0.065
S-20	0.77	1.65	0.030	0.065
S-24	0.77	2.41	0.030	0.095

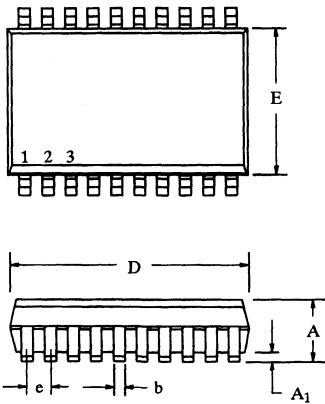
# Package Information

## ■ TO-100 Metal Can, 10-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.19	4.70	0.165	0.185
A <sub>1</sub>	-	1.02	-	0.040
Øb	0.41	0.53	0.016	0.021
ØD	8.51	9.40	0.335	0.370
ØD <sub>1</sub>	7.75	8.51	0.305	0.335
E	0.25	1.02	0.010	0.040
e	5.84 BSC		0.230 BSC	
e <sub>1</sub>	2.92 BSC		0.115 BSC	
j	0.72	0.86	0.028	0.034
k	0.74	1.14	0.029	0.045
L	12.70	-	0.500	-

## ■ Wide-Body SOIC, 16- to 28-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.15	2.90	0.085	0.114
A <sub>1</sub>	0.10	0.30	0.004	0.012
b	0.35	0.45	0.014	0.018
c	0.23	0.28	0.009	0.011
D-16	9.95	10.75	0.392	0.423
D-20	12.50	13.30	0.492	0.524
D-24	15.05	15.85	0.593	0.624
D-28	17.60	18.40	0.693	0.724
E	7.25	8.00	0.285	0.315
e	127 BSC		0.050 BSC	
H	9.80	10.60	0.386	0.417
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

## Conversion Table

	Original "DG" Part No.	JAN Part No.	Original "DG" Part No.	JAN Part No.
<b>DG180 Series to MIL-M-38510</b> This family consists of silicon, break-before-make, multi-chip analog switches with drivers.	DG181AP/883 DG181AP/883 DG181AA/883 DG181AA/883 DG181AL/883 DG182AP/883 DG182AP/883 DG182AA/883 DG182AA/883 DG182AL/883 DG184AP/883 DG184AP/883 DG184AL/883 DG185AP/883 DG185AP/883 DG185AL/883	JM38510/11101BCC JM38510/11101BCA JM38510/11101BIC JM38510/11101BIA JM38510/11101BXA JM38510/11102BCC JM38510/11102BCA JM38510/11102BIC JM38510/11102BIA JM38510/11102BXA JM38510/11103BEC JM38510/11103BEA JM38510/11103BXA JM38510/11104BEC JM38510/11104BEA JM38510/11104BXA	DG187AP/883 DG187AP/883 DG187AA/883 DG187AA/883 DG187AL/883 DG188AP/883 DG188AP/883 DG188AA/883 DG188AA/883 DG188AL/883 DG190AP/883 DG190AP/883 DG190AL/883 DG191AP/883 DG191AP/883 DG191AL/883	JM38510/11105BCC JM38510/11105BCA JM38510/11105BIC JM38510/11105BIA JM38510/11105BXA JM38510/11106BCC JM38510/11106BCA JM38510/11106BIC JM38510/11106BIA JM38510/11106BXA JM38510/11107BEC JM38510/11107BEA JM38510/11107BXA JM38510/11108BEC JM38510/11108BEA JM38510/11108BXA
<b>DG200 Series to MIL-M-38510</b> This family consists of monolithic, silicon, CMOS negative logic analog switches.	DG200AAP/883 DG200AAK/883 DG200AAA/883 DG200AAA/883 DG201AAP/883 DG201AAK/883	JM38510/12301BCC JM38510/12301BCA JM38510/12301BIC JM38510/12301BIA JM38510/1202BCC JM38510/12302BEA		
<b>DG300 Series to MIL-M-38510</b> This family consists of silicon, CMOS, monolithic, analog switches with drivers.	DG300AAP/883 DG300AAK/883 DG300AAA/883 DG301AAP/883 DG301AAK/883 DG301AAA/883 DG302AAP/883 DG302AAK/883 DG303AAP/883 DG303AAK/883	JM38510/11601BCC JM38510/11601BCA JM38510/11601BIA JM38510/11602BCC JM38510/11602BCA JM38510/11602BIA JM38510/11603BCC JM38510/11603BCA JM38510/11604BCC JM38510/11604BCA	DG304AAP/883 DG304AAK/883 DG304AAA/883 DG305AAP/883 DG305AAK/883 DG305AAA/883 DG306AAP/883 DG306AAK/883 DG307AAP/883 DG307AAK/883	JM38510/11605BCC JM38510/11605BCA JM38510/11605BIA JM38510/11606BCC JM38510/11606BCA JM38510/11606BIA JM38510/11607BCC JM38510/11607BCA JM38510/11608BCC JM38510/11608BCA
<b>DG506 Series to MIL-M-38510</b> This family consists of monolithic, silicon, CMOS/analog logic microcircuit.	DG506AAR/883 DG507AAR/883 DG508AAP/883 DG508AAP/883 DG509AAP/883 DG509AAP/883	JM38510/19001BXC JM38510/19003BXC JM38510/19007BEA JM38510/19007BEC JM38510/19008BEA JM38510/19008BEC		
	<b>Basic "DG" Part No.</b>	<b>Standard Military Drawing Part No.</b>	<b>Basic "DG" Part No.</b>	<b>Standard Military Drawing Part No.</b>
<b>Standard Military Drawings</b> The following analog switches and multiplexers consists of monolithic, silicon CMOS except for the DG180, DG189, and DG129 parts which are silicon, multichip with bipolar driver.	DG129AP DG180AL DG180AP DG180AA DG189AP DG201AAZ DG201AAK DG201AAP DG201AAL DG201AAL DG271AZ DG271AK DG401AZ DG401AK DG403AK DG405AZ DG405AK DG408AK DG408AZ	7801401CA 8767301AA 8767301CA 8767301IA 5962-9068901MEA 77053012A 7705301EA 7705301EC 7705301FA 7705301FC 5962-86716022A 5692-8976301EA 5962-90569012A 5962-9056901EA 5692-8976301EA 5962-89961012A 5962-8996101EA 5962-9204201MEA 5962-9204201M2A	DG409AK DG409AZ DG411AZ DG411AK DG412AZ DG412AK DG413AZ DG413AK DG441AK DG441AZ DG442AK DG442AZ DG508AAP DG508AAP DG508AAL DG528AK DG542AP	5962-9204202MEA 5962-9204202M2A 5962-9073101M2A 5962-9073101MEA 5962-9073102M2A 5962-9073102MEA 5962-9073103M2A 5962-9073103MEA 5962-9204101MEA 5962-9204101M2A 5962-9204102MEA 5962-9204102M2A 7705201EA 7705201EC 7705201FA 5692-8768901VA 5962-9155201MEA

## Process Option Flows

Test and Condition		U.S. Build Only if Specified <sup>a</sup>	U.S. Build or QML Offshore Build	Parts Marked /883 or SMD, as Applicable <sup>c</sup>	
Description	Method Per MIL-STD-883	Space Rated Extended Hi-Rel <sup>b</sup>	Class B S/S JAN Devices	SMD and /883 Compliant Non-JAN Method 5004/5005	Ruggedized Plastic -4 Flow
Traceability to W/L		X	X	X	N/A
SEM		X	N/A	N/A	N/A
Internal Visual	2010	Condition A	Condition B	Condition B	Condition B
Die Shear	2019	X	N/A	N/A	N/A
Bond Strength Cert/Data	2011	X	N/A	N/A	N/A
Stab Bake	1008-C	X	X	X	X
Temp Cycle	1010-C	X	X	X	X
Centrifuge	2001-E	X	X	X	N/A
PIND	2020-A	X	N/A	N/A	N/A
Fine Leak	1014-A or -B	X	X	X	N/A
Gross Leak	1014-C	X	X	X	N/A
1st Electrical	per spec	X	X	X	X
Burn-In	1015-A or -C	72 hrs -A	160 hrs per S/S	160 hrs -A or -C	160 hrs. -A or -C
Interim Electrical Post Burn-In		per spec <sup>d</sup>	Static 25°C PDA per S/S	Static 25°C PDA = 5%	Static 25°C PDA = 5%
Burn-In	1015-A or -C	240 hrs Dyn. (Min.)	per S/S	N/A	N/A
Interim Electrical Post Burn-In	Static <sup>e</sup>	Static 25°C PDA = 5%	N/A	N/A	N/A
	Functional <sup>e</sup>	Functional 25°C PDA = 3% (datalog)	per S/S	N/A	N/A
Final Electrical	Min. Temp.	X	X	X	X
	Max. Temp.	X	X	X	X
Fine Leak	1014-A or -B	X	N/A	N/A	N/A
Gross Leak	1014-C	X	N/A	N/A	N/A
X-Ray	2012	X	N/A	N/A	N/A
QCI A	5005	per spec <sup>d</sup>	X	X	-55, 25, 125°C
QCI B	5005	X	X	X	N/A
QCI C	5005	N/A	X	X	N/A
QCI D	5005	X	X	X	N/A
External Visual	2009	X	X	X	X
Deltas Option		Option	X	N/A	N/A
Solder Dip Option		Option	Option	Option	N/A

**Notes:**

- On U. S. builds, unless otherwise specified by 38510 or drawing, parts may be assembled offshore.
- Space Rated Extended Hi-Rel process option available under customer SCD only.
- Parts not qualified for /883 or SMD must not be marked as such. A special flow for non-compliant, non-JAN product can be generated as custom. Contact marketing for details.
- Per spec is a reference to customer SCD.
- PDA applies to both burn-ins.

**Process Option Flows for Chip/Wafer**

Standard Die/Chip with Element Evaluation	Standard Die/Chip	Standard Die/Wafer Form
Die ship element evaluation non-compliant/ non-JAN subgroup 1 and 3 performed in-line	Die ship No canned sample	Die Wafer form
Wafer probe Static 25°C (min) per device spec Internal visual Method 2010 cond. B	Wafer probe Static 25°C (min) per device spec Internal visual Method 2010 cond. B	Wafer probe Static 25°C (min) per device spec Internal visual Method 2010 cond. B
Canned sample:* Method 2008 MIL STD 883 Class B device Subgroup 1 (ss-10/0) Internal visual Method 2010 cond. B Subgroup 2 (ss-10/1) Final electrical Static @25°C min/max oper. temp. (per device spec) Subgroup 3 (5 Die min) (s/s = 10/0 or 20/1 wires) Non-Destructive Test Method 2023 wire bond eval. Method 2011 (cert and data)  *SEM available	Die prep process	

# Cross Reference



**Siliconix Part Number (Direct Replacement)** Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, the specifications should be carefully compared.

**Siliconix Approximate Replacement**

Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed, as these parts may have different pin configurations. Before selecting a device as a substitute, the specifications should be carefully compared. For devices not shown in this guide, or for additional information, the user should contact the nearest Siliconix sales office.

Industry Part Number	Siliconix Part Number	Approximate Replacement	Page
8100609EA		5962-9056901EA	1-127
8100610EA		5962-9056901EA	1-127
8100611EA		5962-8996101EA	1-127
8100612EA		5962-8976301EA	1-127
8100613EA		5962-8976301EA	1-127
8100614EA		5962-8976301EA	1-127
AD200DIAA	DG200AAA		1-32
AD200DIAP		DG200AAK	1-32
AD200DIBA	DG200ABA		1-32
AD200DICJ		DG200ACJ	1-32
AD200DIPB		DG200ABK	1-32
AD201DIAP		DG411AK	1-137
AD201DIBP		DG411AK	1-137
AD201DICJ		DG411DJ	1-137
AD302DIAP	DG302AAK		1-90
AD302DIBP	DG302AAK		1-90
AD302DICJ	DG302ACJ		1-90
AD303DIAP	DG303AAK		1-90
AD303DIBP	DG303AAK		1-90
AD303DICJ	DG303ACJ		1-90
AD7506DK		DG506ABK	2-52
AD7506JN	DG506ACJ		2-52
AD7506JQ	DG506ACK		2-52
AD7506KN	DG506ACJ		2-52
AD7506KQ	DG506ABK		2-52
AD7506SD		DG506AAK	2-52
AD7506SQ	DG506AAK		2-52
AD7506TE	DG506AAZ/883		2-52
AD7506TQ	DG506AAK		2-52
AD7507JN	DG507ACJ		2-52
AD7507JQ	DG507ABK		2-52
AD7507KN	DG507ACJ		2-52
AD7507KQ	DG507ABK		2-52
AD7507SQ	DG507AAK		2-52
AD7507TE	DG507AAZ/883		2-52
AD7507TQ	DG507AAK		2-52
AD7509KD		DG509ABK	2-60
AD7509KN		DG509ACJ	2-60
AD7509SD		DG509AAK	2-60
ADG200AA		DG200AAA	1-32
ADG200AA/883		DG200AAA/883	1-32
ADG200AP		DG200AAK	1-32
ADG200AP/883		DG200AAK/883	1-32
ADG200BA		DG200ABA	1-32
ADG200BP		DG200ABK	1-32
ADG200CJ		DG200ACJ	1-32
ADG201ABQ	DG441AK		1-163
	DG201ABK		1-37
ADG201AKN	DG441DJ		1-163
	DG201ACJ		1-37

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	DG201ADY		1-37
ADG201ATE	5962-9204101M2A		1-163
	DG201AAZ/883		1-37
ADG201ATE/883B	5962-9204101M2A		1-163
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ADG201ATQ	DG441AK		1-163
	DG201AAK		1-37
ADG201ATQ/883	DG441AK/883		1-163
	DG201AAK/883		1-37
ADG201CJ	DG441DJ		1-163
	DG201ACJ		1-37
ADG201HSAQ	DG201HSAK883		1-52
	DG271AK		1-85
ADG201HSBQ		DG201HSAK883	1-52
		DG271AK	1-85
ADG201HSJN	DG201HSDJ		1-52
	DG271CJ		1-85
ADG201HSKN	DG201HSDJ	DG271CJ	1-52
ADG201HSKR	DG201HSDY	DG271DY	1-52
ADG201HSSQ	DG201HSAK883		1-52
	DG271AK		1-85
ADG201HSTE	DG201HSAZ883		1-52
		DG271AZ/883	1-85
ADG201HSTE/883B	DG201HSAZ883		1-52
		DG271AZ/883	1-85
ADG201HSTQ	DG201HSAK883		1-52
		DG271AK	1-85
ADG201HSTQ/883B	DG201HSAK883		1-52
		DG271AK/883	1-85
ADG202ABQ	DG442AK		1-163
	DG202AK		1-37
ADG202AKN	DG442DJ		1-163
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ADG202AKR	DG442DY		1-163
ADG202ATQ	DG442AK		1-163
	DG202AK		1-37
ADG202ATQ/883B	DG442AK/883		1-163
	DG202AK/883		1-37
ADG211AKN	DG444DJ		1-171
	DG411DJ		1-137
	DG211CJ		1-60
ADG211AKR	DG444DY		1-171
	DG411DY		1-137
	DG211DY		1-60
ADG212AKN	DG445DJ		1-171
	DG412DJ		1-137
	DG212CJ		1-60



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ADG212AKR	DG445DY		1-171
	DG412DY		1-137
	DG212DY		1-60
ADG221BQ	DG221AK/883		1-75
ADG221KN	DG221CJ		1-75
ADG221KR	DG221DY		1-75
ADG221TQ	DG221AK/883		1-75
ADG408BN	DG408DJ		2-11
ADG408BR	DG408DY		2-11
ADG408TQ	DG408AK		2-11
ADG409BN	DG409DJ		2-11
ADG409BR	DG409DY		2-11
ADG409TQ	DG409AK		2-11
ADG411BN	DG411DJ		1-137
ADG411BR	DG411DY		1-137
ADG411TQ	DG411AK		1-137
ADG412BN	DG412DJ		1-137
ADG412BR	DG412DY		1-137
ADG412TQ	DG412AK		1-137
ADG441BN	DG441DJ		1-163
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ADG442TQ	DG442AK		1-163
ADG444BN	DG444DJ		1-171
ADG444BQ		DG441AK	1-171
ADG444BR	DG444DY		1-171
ADG444TQ		DG441AK	1-171
ADG445BN	DG445DJ		1-171
ADG445BQ		DG442AK	1-171
ADG445BR	DG445DY		1-171
ADG445TQ		DG442AK	1-171
ADG506ABQ	DG506ABK		2-52
	DG406AK/883		2-1
ADG506AKN	DG506ACJ		2-52
	DG406DJ		2-1
ADG506AKP	DG506ADN		2-52
	DG406DN		2-1
ADG506ATE	DG506AAZ/883		2-52
	DG406AZ/883		2-1
ADG506ATQ	DG506AAK		2-52
	DG406AK/883		2-1
ADG507ABQ	DG507ABK		2-52
	DG407AK/883		2-1
ADG507AKN	DG507ACJ		2-52
	DG407DJ		2-1
ADG507AKP	DG407DN		2-1
ADG507ATE	DG507AAZ/883		2-52
	DG407AZ/883		2-1
ADG507ATQ	DG507AAK		2-52
	DG407AK/883		2-1
ADG508ABQ	DG508ABK		2-60
	DG408AK		2-11
ADG508AKN	DG508ACJ		2-60
	DG408DJ		2-11

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ADG508AKR	DG508ADY		2-60
	DG408DY		2-11
ADG508ATE	DG508AAZ/883		2-60
ADG508ATQ	DG508AAK		2-60
	DG408AK		2-11
ADG509ABQ	DG509ABK		2-60
	DG409AK		2-11
ADG509AKN	DG509ACJ		2-60
	DG409DJ		2-11
ADG509AKR	DG509ADY		2-60
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ADG509ATE	DG509AAZ/883		2-60
ADG509ATQ	DG509AAK		2-60
	DG409AK		2-11
ADG528ABQ	DG528BK		2-70
	DG428AK		2-22
ADG528AKN	DG528CJ		2-70
	DG428DJ		2-22
ADG528AKP	DG528DN		2-70
	DG528AK		2-70
ADG528ATQ	DG428AK		2-22
	DG529BK		2-70
ADG529ABQ	DG429AK		2-22
	DG529CJ		2-70
ADG529AKN	DG429DJ		2-22
	DG529AK/883		2-70
ADG529ATQ	DG429AK		2-22
	DG129AP/883		1-1
AH0126D	DG129AP/883		1-1
AH0126D/883	DG129AP/883		1-1
AH0129D	DG129AP/883		1-1
AH0129D/883	DG129AP/883		1-1
AH0154/883	DG129AP/883		1-1
AH0154D	DG129AP/883		1-1
CDG201AK		DG541AP	1-179
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CDG211CJ		DG541AP	1-179
CDG306AK		DG541AP	1-179
CDG308BJ		DG541DJ	1-179
CDG308BK		DG541AP	1-179
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CLC110AJE	Si581DY		3-1
CLC114AJP	Si584DJ		3-16
CLC114AJE	Si584DY		3-16
CLC410AJP	Si582DJ		3-8
CLC410AJE	Si582DY		3-8
DG200AAP/883	DG200AAK/883		1-32
DG200ABP	DG200ABK		1-32
DG200AK	DG200AAK		1-32
DG200AP	DG200AAK		1-32
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DG200BA	DG200ABA		1-32
DG200BK	DG200ABK		1-32
DG200BP	DG200ABK		1-32
DG200CA	DG200ABA		1-32
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DG201ACJ-2	DG441DJ		1-163
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DG201ACSE	DG441DY		1-163
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DG201ACY	DG441DY		1-163
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DG201AK	DG441AK		1-163
	DG201AAK		1-37
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	DG201AAK/883		1-37
DG201BK	DG441AK		1-163
	DG201ABK		1-37
DG201CJ	DG441DJ		1-163
	DG201ACJ		1-37
DG202AK	DG442AK		1-163
	DG202AK		1-37
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DG202BSE	DG442DY		1-163
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DG202CJ-2	DG442DJ		1-163
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DG202CK	DG442AK		1-163
	DG202AK		1-37
DG202CSE	DG442DY		1-163
	DG212DY		1-60
DG202DY	DG442DY		1-163
	DG212DY		1-60
DG211CJ-2	DG444DJ		1-171
	DG411DJ		1-137
	DG211CJ		1-60
DG211CSE	DG444DY		1-171
	DG411DY		1-137
	DG211DY		1-60
DG211CY	DG444DY		1-171
	DG411DY		1-137
DG211DY	DG211DY		1-60
	DG444DY		1-171
DG212CJ	DG412DJ		1-137
	DG212CJ		1-60
	DG445DY		1-171
DG212CSE	DG412DY		1-137
	DG212DY		1-60
	DG445DY		1-171
DG212CY	DG412DY		1-137
	DG212DY		1-60
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DG212DY	DG412DY		1-137
	DG212DY		1-60
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DG221CY	DG221DY		1-75
DG271AK-2	DG271AK/883		1-85
DG271BK	DG271AK		1-85
DG271CK	DG271AK		1-85
DG281AA/883	DG181AA/883		1-4
DG281AP/883	DG181AP/883		1-4
DG284AP/883	DG184AP/883		1-11
DG287AP/883	DG187AP/883		1-18
DG290AP/883	DG190AP/883		1-25
DG300AA	DG300AAA/883		1-90
DG300AAA	DG300AAA/883		1-90
DG300AAA-2	DG300AAA/883		1-90
DG300AAA/HR	DG300AAA/883		1-90
DG300AAK-2	DG300AAK/883		1-90
DG300AAK/HR	DG300AAK/883		1-90
DG300ACA	DG300ABA		1-90
DG300ACK	DG300ABK		1-90
DG300AK	DG300AAK		1-90
DG300BA	DG300ABA		1-90
DG300BK	DG300ABK		1-90
DG300CJ	DG300ACJ		1-90
DG300CK	DG300ABK		1-90
DG301AA	DG301AAA		1-90
DG301AAA-2	DG301AAA/883		1-90
DG301AAA/HR	DG301AAA/883		1-90
DG301AAK-2	DG301AAK/883		1-90
DG301AAK/HR	DG301AAK/883		1-90
DG301ACA	DG301ABA		1-90
DG301ACK	DG301ABK		1-90
DG301AK	DG301AAK		1-90
DG301BA	DG301ABA		1-90
DG301BK	DG301ABK		1-90
DG301CJ	DG301ACJ		1-90
DG301CK	DG301ABK		1-90
DG302AAK-2	DG302AAK/883		1-90
DG302AAK/HR	DG302AAK/883		1-90
DG302ABK	DG302AAK		1-90
DG302ACK	DG302AAK		1-90
DG302AK	DG302AAK		1-90
DG302BK	DG302AAK		1-90
DG302CJ	DG302ACJ		1-90
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DG303AK	DG303AAK		1-90
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DG306BK	DG306AAK/883		1-99
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IH5143CPE	DG403DJ		1-127
IH5143MJE	DG403AK		1-127
IH5143MJE/883B	DG403AK/883		1-127
IH5144MJE		DG405AK	1-127
IH5144MJE/883B		DG405AK/883	1-127
IH5145CJE	DG405AK		1-127
IH5145CPE	DG405DJ		1-127
IH5145MJE	DG405AK		1-127
IH5145MJE/883B	DG405AK/883		1-127
IH5208CJE	DG459AK/883		2-34
IH5208CPE	DG459DJ		2-34
IH5208IJE	DG459AK/883		2-34
IH5208MJE	DG459AK/883		2-34
IH5208MJE/883B	DG459AK/883		2-34
IH6108CJE	DG408AK		2-11
	DG508ACK		2-60

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IH6108CPE	DG408DJ		2-11
	DG508ACJ		2-60
IH6108MJE	DG408AK		2-11
	DG508AAK		2-60
IH6116CJ1		DG406AK	2-1
		DG506AAK	2-52
IH6116CPI		DG406DJ	2-1
		DG506ACJ	2-52
IH6116MJ1		DG406AK	2-1
		DG506AAK	2-52
IH6116MJ1/883B		DG406AK/883	2-1
		DG506AAK/883	2-52
IH6208CJE	DG409AK		2-11
	DG509ACK		2-60
IH6208CPE	DG409DJ		2-11
	DG509ACJ		2-60
IH6208MJE	DG409AK		2-11
	DG509AAK		2-60
IH6208MJE/883B	DG409AK/883		2-11
	DG509AAK/883		2-60
IH6216CJ1		DG407AK	2-1
		DG507AAK	2-52
IH6216CPI		DG407DJ	2-1
		DG507ACJ	2-52
IH6216MJ1		DG407AK	2-1
		DG507AAK	2-52
IH6216MJ1/883B		DG407AK/883	2-1
		DG507AAK/883	2-52
JM38510/11601BCC	JM38510/11601BCA		1-90
JM38510/11602BCC	JM38510/11602BCA		1-90
JM38510/11603BCC	JM38510/11603BCA		1-90
JM38510/11604BCC	JM38510/11604BCA		1-90
JM38510/11605BCC	JM38510/11605BCA		1-99
JM38510/11606BCC	JM38510/11606BCA		1-99
JM38510/11607BCC	JM38510/11607BCA		1-99
JM38510/11608BCC	JM38510/11608BCA		1-99
JM38510/12301BCC	JM38510/12301BCA		1-32
JM38510/12302BEC	JM38510/12302BEA		1-37
LP11201AD		DG411AK	1-137
LP11201N		DG411DJ	1-137
LP11202D		DG412AK	1-137
LP12201D		DG411AK	1-137
LP12202D		DG412AK	1-137
LP12202N		DG412DJ	1-137
LP13201D		DG411AK	1-137
LP13201N		DG411DJ	1-137
LP13202D		DG412AK	1-137
LP13202N		DG412DJ	1-137
LTC1044CJ8	SI7660CJ		4-1
MAX301CPE	DG401DJ		1-127
MAX301CSE	DG401DY		1-127
MAX301EPE	DG401DJ		1-127
MAX301ESE	DG401DY		1-127
MAX301EJE	DG401AK		1-127
MAX301MLP	DG401AZ/883		1-127
MAX301MJE	DG401AK		1-127
MAX303CPE	DG403DJ		1-127
MAX303CSE	DG403DY		1-127

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MAX303EPE	DG403DJ		1-127
MAX303ESE	DG403DY		1-127
MAX303EJE	DG403AK		1-127
MAX303MLP	DG403AZ/883		1-127
MAX303MJE	DG403AK		1-127
MAX305CPE	DG405DJ		1-127
MAX305CSE	DG405DY		1-127
MAX305EPE	DG405DJ		1-127
MAX305ESE	DG405DY		1-127
MAX305EJE	DG405AK		1-127
MAX305MLP	DG405AZ/883		1-127
MAX305MJE	DG405AK		1-127
MAX306CJ	DG406DJ		2-1
MAX306DJ	DG406DJ		2-1
MAX306DN	DG406DN		2-1
MAX306DK	DG406AK		2-1
MAX306AK	DG406AK		2-1
MAX307CJ	DG407DJ		2-1
MAX307DJ	DG407DJ		2-1
MAX307DN	DG407DN		2-1
MAX307DK	DG407AK		2-1
MAX307AK	DG407AK		2-1
MAX308EPE	DG408DJ		2-11
MAX308ESE	DG408DY		2-11
MAX308EJE	DG408AK		2-11
MAX308MJE	DG408AK		2-11
MAX309EPE	DG409DJ		2-11
MAX309ESE	DG409DY		2-11
MAX309EJE	DG409AK		2-11
MAX309MJE	DG409AK		2-11
MAX317CPA	DG417DJ		1-146
MAX317CSA	DG417DY		1-146
MAX317EPA	DG417DJ		1-146
MAX317ESA	DG417DY		1-146
MAX317EJA	DG417AK		1-146
MAX317MJA	DG417AK		1-146
MAX318CPA	DG418DJ		1-146
MAX318CSA	DG418DY		1-146
MAX318EPA	DG418DJ		1-146
MAX318ESA	DG418DY		1-146
MAX318EJA	DG418AK		1-146
MAX318MJA	DG418AK		1-146
MAX319CPA	DG419DJ		1-146
MAX319CSA	DG419DY		1-146
MAX319EPA	DG419DJ		1-146
MAX319ESA	DG419DY		1-146
MAX319EJA	DG419AK		1-146
MAX319MJA	DG419AK		1-146
MAX331MJE	DG441AK		1-163
MAX332MJE	DG442AK		1-163
MAX351CPE	DG411DJ		1-137
MAX351CSE	DG411DY		1-137
MAX351EPE	DG411DJ		1-137
MAX351ESE	DG411DY		1-137
MAX351EJE	DG411AK		1-137
MAX351MJE	DG411AK		1-137
MAX352CPE	DG412DJ		1-137
MAX352CSE	DG412DY		1-137
MAX352EPE	DG412DJ		1-137
MAX352ESE	DG412DY		1-137

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MAX352EJE	DG412AK		1-137
MAX352MJE	DG412AK		1-137
MAX353CPE	DG413DJ		1-137
MAX353CSE	DG413DY		1-137
MAX353EPE	DG413DJ		1-137
MAX353ESE	DG413DY		1-137
MAX353EJE	DG413AK		1-137
MAX353MJE	DG413AK		1-137
MAX358CJE	DG458AK/883		2-34
MAX358CPE	DG458DJ		2-34
MAX358CPE-2	DG458DJ		2-34
MAX358EJE	DG458AK/883		2-34
MAX358EPE	DG458DJ		2-34
MAX358MJE	DG458AK/883		2-34
MAX358MJE/883	DG458AK/883		2-34
MAX358MJE/HR	DG458AK/883		2-34
MAX358MLP	DG458AZ/883		2-34
MAX359CJE	DG459AK/883		2-34
MAX359CPE	DG459DJ		2-34
MAX359CPE-2	DG459DJ		2-34
MAX359EJE	DG459AK/883		2-34
MAX359EPE	DG459DJ		2-34
MAX359IJE	DG459AK/883		2-34
MAX359MJE	DG459AK/883		2-34
MAX359MJE/883	DG459AK/883		2-34
MAX359MJE/HR	DG459AK/883		2-34
MAX359MLP	DG459AZ/883		2-34
MAX361CPE	DG441DJ		1-163
MAX361CSE	DG441DY		1-163
MAX361EPE	DG441DJ		1-163
MAX361ESE	DG441DY		1-163
MAX361EJE	DG441AK		1-163
MAX361MJE	DG441AK		1-163
MAX362CPE	DG442DJ		1-163
MAX362CSE	DG442DY		1-163
MAX362EPE	DG442DJ		1-163
MAX362ESE	DG442DY		1-163
MAX362EJE	DG442AK		1-163
MAX362MJE	DG442AK		1-163
MAX364CPE	DG444DJ		1-171
MAX364CSE	DG444DY		1-171
MAX364EPE	DG444DJ		1-171
MAX364ESE	DG444DY		1-171
MAX365CPE	DG445DJ		1-171
MAX365CSE	DG445DY		1-171
MAX365EPE	DG445DJ		1-171
MAX365ESE	DG445DY		1-171
MP200DIAA		DG200AAA	1-32
MP200DIAP		DG200AAK	1-32
MP200DIBA		DG200ABA	1-32
MP200DICJ		DG200ACJ	1-32
MP200DIPB		DG200ABK	1-32
MP201DIBP		DG411AK	1-137
MP201DICJ		DG411DJ	1-137
MP20ADIAP		DG411AK	1-137
MP302DIAP	DG302AAK		1-90
MP302DIBP	DG302AAK		1-90
MP302DICJ	DG302ACJ		1-90
MP303DIAP	DG303AAK		1-90

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MP303DIBP	DG303AAK		1-90
MP303DICJ	DG303ACJ		1-90
MP7506JD	DG506ACK		2-52
MP7506JN	DG506ACJ		2-52
MP7506KD	DG506ACK		2-52
MP7506KN	DG506ACJ		2-52
MP7506SD	DG506AAK		2-52
MP7506TD	DG506AAK		2-52
MP7507JD	DG507AAK		2-52
MP7507JN	DG507ACJ		2-52
MP7507KD	DG507AAK		2-52
MP7507KN	DG507ACJ		2-52
MP7507SD	DG507AAK		2-52
MP7507TD	DG507AAK		2-52
MP7508KD		DG508ABK	2-60
MP7508KN		DG508ACJ	2-60
MP7508SD		DG508AAK	2-60
MP7509KD		DG509ABK	2-60
MP7509KN		DG509ACJ	2-60
MP7509SD		DG509AAK	2-60
MUX08BQ		DG408AK	2-11
MUX08FP		DG408DJ	2-11
MUX08FQ		DG408AK	2-11
MUX16BT		DG506AAK	2-52
MUX16FT		DG506ABK	2-52
MUX24BQ		DG409AK	2-11
MUX24FP		DG409DJ	2-11
MUX24FQ		DG409AK	2-11
MUX28BT		DG507AAK	2-52
MUX28FT		DG507ABK	2-52
SI7661CA		SI7661CJ	4-7
SW01BQ		DG201AAK	1-37
SW01BQ883		DG201AAK/883	1-37
SW01FQ		DG201ABK	1-37
SW02BQ		DG202AK	1-37
SW02BQ883		DG202AK/883	1-37
SW02FQ		DG202AK	1-37
SW05BK		DG200AAA	1-32
SW05BK883		DG200AAA/883	1-32
SW05BY		DG200AAK	1-32
SW05BY883		DG200AAK/883	1-32
SW05FK		DG200ABA	1-32
SW05FY		DG200ABK	1-32
SW05GP		DG202CJ	1-37
SW201BQ		DG411AK	1-137
SW201BQ883		DG411AK/883	1-137
SW201FQ		DG411AK	1-137
SW201GP		DG411DJ	1-137
SW202BQ		DG412AK	1-137
SW202BQ883		DG412AK/883	1-137
SW202FQ		DG412AK	1-137
SW202GP		DG412DJ	1-137
TSC7660COA	SI7660DY		4-1
TSC7660CPA	SI7660CJ		4-1

This Cross Reference material is accurate to the best knowledge and belief of Siliconix. Since individual circuit design and layout can influence device performance, the purchaser must be responsible for the ultimate selection and determination of interchangeability.



<b>General Information</b>	<b>1</b>
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<b>Worldwide Sales Offices and Distributors</b>	<b>6</b>



## U.S. Sales Offices

### EASTERN

Huntsville, AL (35824)  
TEMIC  
125 Electronics Boulevard, Ste. C-1  
TEL: (205) 461-7894/7895  
FAX: (205) 461-7928

Hoffman Estates, IL (60195)  
TEMIC  
1030 W. Higgins Road, Ste. 101  
TEL: (708) 490-0374  
FAX: (708) 490-1499

Annapolis, MD (21403)  
TEMIC  
1419 Forest Drive, Ste. 103  
TEL: (410) 269-1898  
FAX: (410) 974-8170

Troy, MI (48084)  
TEMIC  
Troy Technical Center  
Continental Plaza  
2701 Troy Center Drive, Ste. 100  
TEL: (810) 244-1400  
FAX: (810) 244-0848

Nashua, NH (03062)  
TEMIC  
20 Heather Court  
TEL: (603) 886-9603  
FAX: (603) 886-9603

Annandale, NJ (08801)  
TEMIC  
1322 Route 31 North  
TEL: (908) 735-6100  
FAX: (908) 735-2258

Ossining, NY (10562)  
TEMIC  
74 Revolutionary Road  
TEL: (914) 945-0618  
FAX: (914) 945-0769

White Plains, NY (10605)  
TEMIC  
12 Roland Drive  
TEL: (914) 997-1265  
FAX: (914) 997-1277

Asheville, NC (28801)  
TEMIC  
46 Haywood Street, Ste. 337  
TEL: (704) 252-9827  
FAX: (704) 252-3083

### WESTERN

Santa Clara, CA (95056)  
TEMIC c/o Siliconix Inc.  
2201 Laurelwood Road  
P.O. Box 54951

TEL: (408) 970-5700  
FAX: (408) 970-3950

Irvine, CA (92619-1084)  
TEMIC  
P.O. Box 51084  
TEL: (714) 552-4080  
FAX: (714) 552-4181

Houston (77027)  
TEMIC  
2100 West Loop South, Ste. 800  
TEL: (713) 297-8871  
FAX: (713) 297-8872

## U.S. Sales Representatives

### ALABAMA

Huntsville (35803)  
Rep, Inc.  
11535 Gilleland Road  
TEL: (205) 881-9270  
FAX: (205) 882-6692

### ALASKA

See Washington

### ARIZONA

Tempe (85283)  
Quadrep Southern  
40 W. Baseline Road, Ste. 112  
TEL: (602) 839-2102  
FAX: (602) 839-2126

### ARKANSAS

See Texas (Arlington)

### CALIFORNIA (Southern)

San Diego (92130)  
Quadrep Southern, Inc.  
11995 El Camino Real, Ste. 305  
TEL: (619) 755-1188  
FAX: (619) 793-9269

Irvine (92718)  
Quadrep Southern, Inc.  
15215 Alton Parkway, Ste. 200  
TEL: (714) 727-4222  
FAX: (714) 727-4033

### CALIFORNIA (Northern)

San Jose (95134)  
Quadrep, Inc.  
2635 N. First Street, Ste. 116  
TEL: (408) 432-3300  
FAX: (408) 432-3428

### COLORADO

Littleton (80122)  
Quadrep, Inc.  
7891 S. Garfield Way  
TEL: (303) 771-6886  
FAX: (303) 771-6887

### CONNECTICUT

Wallingford (06492)  
Technology Sales, Inc.  
237 Hall Avenue  
TEL: (203) 269-8853  
FAX: (203) 269-2099

### DELAWARE

See New Jersey (Southern)

### DISTRICT OF COLUMBIA

See Maryland

### FLORIDA

Deerfield Beach (33441)  
MEC  
400 Fairway Drive Ste. 107  
TEL: (305) 426-8944  
FAX: (305) 570-8568

Largo (34643)  
MEC  
10637 Harborside Drive North  
TEL: (813) 393-5011  
FAX: (813) 393-5202

Winter Park (32789)  
MEC  
1305 Raintree Place  
TEL: (407) 740-0023  
FAX: (407) 740-0083

### GEORGIA

Tucker (30084)  
Rep, Inc.  
1944 Northlake Parkway  
TEL: (404) 938-4358  
FAX: (404) 938-0194

### HAWAII

See California (Northern)

### IDAHO

Boise (83702)  
Q.R. Crown  
1524 W. Hays  
TEL: (208) 344-9588  
FAX: (208) 344-9550

### ILLINOIS

Hoffman Estates (60195)  
Victory Sales  
1030 W. Higgins Road, Ste. 101  
TEL: (708) 490-0300  
FAX: (708) 490-1499

### INDIANA

Indianapolis (46250)  
Victory Sales  
8041 Knue Road  
TEL: (317) 577-4786  
FAX: (317) 577-4789

### IOWA

Cedar Rapids (52402)  
Stan Clothier Company  
1930 Street Andrews NE  
TEL: (319) 393-1576  
FAX: (319) 393-7317

### KANSAS

Lenexa (66215)  
Stan Clothier Co.  
13000 W. 87th Street Parkway, Ste. 105  
TEL: (913) 492-2124  
FAX: (913) 492-1855

### KENTUCKY

See Indiana

### LOUISIANA

See Arlington, Texas

### MAINE

See Massachusetts

### MARYLAND

Towson (21204)  
Arbotek Associates, Inc.  
102 W. Joppa Road  
TEL: (410) 825-0775  
FAX: (410) 337-2781

### MASSACHUSETTS

Waltham (02154)  
Technology Sales, Inc.  
332 Second Avenue  
TEL: (617) 890-5700  
FAX: (617) 890-3913

### MICHIGAN

See TEMIC Sales Offices, Troy, MI

### MINNESOTA

Eden Prairie (55344)  
Stan Clothier  
9600 W. 76th Street, Ste. A  
TEL: (612) 944-3456  
FAX: (612) 944-6904

### MISSISSIPPI

See Alabama

### MISSOURI

Saint Charles (63303)  
Stan Clothier Company  
3910 Old Highway 94, South, Ste. 116  
TEL: (314) 928-8078  
FAX: (314) 447-5214

### MONTANA

See Washington

### NEBRASKA

See Missouri

### NEVADA (Except Clark County)

See California (Northern)

### NEVADA (Clark County)

See Arizona

### NEW HAMPSHIRE

See Massachusetts

### NEW JERSEY

See New York (Metro/L.I.)

### NEW MEXICO

See Arizona

## U.S. Sales Representatives (Cont'd)

### NEW YORK (Upstate)

Fairport (14450)  
Technology Sales, Inc.  
920 Perinton Hills Office Park  
TEL: (716) 223-7500  
FAX: (716) 223-5526

### NEW YORK (Metro/L.I.)

Babylon (11702)  
Astrorep Incorporated  
103 Cooper Street  
TEL: (516) 422-2500  
FAX: (516) 422-2504

### NORTH CAROLINA

Morrisville (27560)  
Rep. Inc.  
2500 Gateway Centre Blvd., Ste. 400  
TEL: (919) 469-9997  
FAX: (919) 481-3879

### NORTH DAKOTA

See Minnesota

### OHIO

See Indiana

### OKLAHOMA

See Texas (Arlington)

### OREGON

Portland (97224)  
Q.R. Crown, Inc.  
17020 SW Upper Boones Ferry Road,  
Ste. 202  
TEL: (503) 620-8320  
FAX: (503) 639-4023

### PENNSYLVANIA (Western)

See Indiana

### PENNSYLVANIA (Eastern)

See New York (Metro/L.I.)

### PUERTO RICO

San German (00683-0121)  
Technology Sales, Inc.  
PO Box 122, Edificio Rali, Ste. 216  
TEL: (809) 892-4745  
FAX: (809) 892-1128

### RHODE ISLAND

See Massachusetts

### SOUTH CAROLINA

See Tennessee

### SOUTH DAKOTA

See Minnesota

### TENNESSEE

Jefferson City (37760)  
Rep. Inc.  
P. O. Box 490  
1908 Branner Avenue  
TEL: (615) 475-9012/9013  
FAX: (615) 475-6340

### TEXAS

Arlington (76006)  
Ion Associates, Inc.  
2221 E. Lamar, Ste. 250  
TEL: (817) 695-8000  
FAX: (817) 695-8010

Austin (78759)  
Ion Associates, Inc.  
4412 Spicewood Springs Road, Ste. 202  
TEL: (512) 794-9006  
FAX: (512) 794-9008

Houston (77014)  
Ion Associates, Inc.  
14347-A Turrey Chase Blvd.  
TEL: (713) 537-7717  
FAX: (713) 537-5612

### UTAH

See Colorado

### VERMONT

See Massachusetts

### VIRGINIA

See Maryland

### WASHINGTON

Bellevue (98005)  
Q.R. Crown, Inc.  
375 118th Ave., S.E., Ste. 110  
TEL: (206) 453-5100  
FAX: (206) 646-8775

### WEST VIRGINIA

See Maryland

### WISCONSIN

Brookfield (53005)  
Victory Sales  
405 N. Calhoun Road, Ste. 208  
TEL: (414) 789-5770  
FAX: (414) 789-5760

### WYOMING

See Colorado

## Canadian Sales Representatives

Brampton, Ontario (L6T 1K2)  
Electronics Sales Professionals (ESP) Inc.  
27 Anne Court  
TEL: (416) 458-1103  
FAX: (416) 458-4469  
British Columbia  
See Washington

Montreal, Quebec (H2B 1Z2)  
Electronics Sales Professionals (ESP) Inc.  
2102 Place Etienne-Brule  
TEL: (514) 388-6596  
FAX: (514) 388-8402

North Gower, Ontario (K0A 2T0)  
Electronics Sales Professionals (ESP) Inc.  
5936 Third Line Road North RR #3  
TEL: (613) 489-3379  
FAX: (613) 489-2778

Scarborough, Ontario (M1V 3P6)  
Electronics Sales Professionals (ESP) Inc.  
60 Wilderness Drive  
TEL: (416) 321-9693  
FAX: (416) 321-9794

## Chip Distributor

### FLORIDA

Orlando (32810)  
Chip Supply, Inc.  
7725 N. Orange Blossom Trail  
TEL: (407) 298-7100  
TWX: (810) 850-0103  
FAX: (407) 290-0164

## U. S. Distributors

### ALABAMA

Huntsville (35816)  
Future Electronics Corp.  
4825 University Square, Ste. 12  
TEL: (205) 830-2322  
FAX: (205) 830-6664

Huntsville (35801)  
Marshall Industries  
3313 Memorial Parkway South, Ste. 150  
TEL: (205) 881-9235  
FAX: (205) 881-1490

Huntsville (35816)  
Pioneer Tech.  
4835 University Square, Ste. 5  
TEL: (205) 837-9300  
FAX: (205) 837-9358

### ARIZONA

Phoenix (85034)  
Future Electronics Corp.  
4636 E. University Drive, Ste. 245  
TEL: (602) 968-7140  
FAX: (602) 968-0334

Phoenix (85044)  
Marshall Industries  
9830 S. 51st Street, Ste. B121  
TEL: (602) 496-0290  
FAX: (602) 893-9029

Phoenix (85040)  
Wyle Laboratories-EMG  
4141 E. Raymond Street, Ste. 1  
TEL: (602) 437-2088  
FAX: (602) 437-2124

Tempe (85281)  
Bell Industries  
140 S. Lindon Lane #102  
TEL: (602) 966-3600  
(800) 525-6666  
FAX: (602) 967-6584

Tempe (85281)  
Hamilton/Hallmark  
1626 S. Edward Drive  
(800) 332-8638  
FAX: (800) 257-0568

### CALIFORNIA

Agoura Hills (91301)  
Bell Industries  
30101 Agoura Court, Ste. 118  
TEL: (818) 865-7900  
(800) 525-6666  
FAX: (818) 991-7695

Agoura Hills (91301)  
Pioneer Std.  
5126 Claret Drive, Ste. 160  
TEL: (818) 865-5800  
FAX: (818) 865-5814

Calabasas (91302-1959)  
Marshall Industries  
26637 Agoura Road  
TEL: (818) 878-7000  
FAX: (818) 880-6846

Calabasas (91302)  
Wyle Laboratories  
26010 Mureau Road, Ste. 150  
TEL: (818) 880-9000  
FAX: (818) 880-5510

Chatsworth (91311)  
Future Electronics Corp.  
9301 Oakdale Ave., Ste. 210  
TEL: (818) 772-6240  
FAX: (818) 772-6247

Costa Mesa (92626)  
Hamilton/Hallmark - #29  
3170 Palmans Street  
TEL: (714) 641-4100  
FAX: (714) 641-4122

Culver City (90230)  
Hamilton Corporate  
10950 W. Washington Blvd.  
TEL: (310) 558-2000  
FAX: (310) 558-2076

El Monte (91731)  
Marshall Corporate  
9320 Elstar Avenue  
TEL: (818) 307-6000  
FAX: (818) 307-6297

Irvine (92718)  
Bell Industries  
220 Technology Drive, Ste. 100  
TEL: (714) 727-4500  
(800) 525-6666  
FAX: (714) 453-4610

Irvine (92714)  
Future Electronics Corp.  
1692 Browning Ave.  
TEL: (714) 250-4141  
FAX: (714) 250-4185

Irvine (92718)  
Marshall Industries  
1 Morgan  
TEL: (714) 859-5050  
FAX: (714) 581-5255

Irvine (92718)  
Pioneer Std.  
217 Technology Drive, Ste. 110  
TEL: (714) 753-5090  
FAX: (714) 753-5074

Irvine (92714)  
Wyle Laboratories-EMG  
17872 Cowan Avenue  
TEL: (714) 863-9953  
TWX: (910) 595-1572  
FAX: (714) 863-0473

Los Angeles (90049)  
Bell Industries  
11812 San Vicente Blvd., Ste. 300  
TEL: (310) 826-2355  
(800) 525-6666  
FAX: (310) 826-1534

Milpitas (95035)  
Marshall Industries  
336 Los Coches Street  
TEL: (408) 942-4600  
FAX: (408) 262-1224

Rancho Cordova (95670)  
Marshall Industries  
3039 Kilgore Ave. Ste. 140  
TEL: (916) 635-9700  
FAX: (916) 635-6044

Rancho Cordova (95742)  
Wyle Distribution Group  
Sacramento Division  
2951 Sunrise Blvd., Ste. 175  
TEL: (916) 638-5282  
FAX: (916) 638-1491

Reseda (91335)  
JAN Devices  
6925 Canby, Bldg. 109  
TEL: (818) 708-1100  
FAX: (818) 708-7436

Rocklin (95677)  
Bell Industries  
4311 Anthony Ct, Ste. 100  
TEL: (916) 652-0418  
(800) 525-6666  
FAX: (916) 652-0403

Rocklin (95765)  
Hamilton/Hallmark - #35  
580 Menlo Drive, Ste. 2  
TEL: (916) 624-9781  
FAX: (916) 961-0922

San Diego (92123)  
Bell Industries  
5520 Ruffin Road, Ste. 209  
TEL: (619) 576-3924  
(800) 525-6666  
FAX: (619) 492-9826

San Diego (92122)  
Future Electronics Corp.  
5151 Shoreham Place, Ste. 220  
TEL: (619) 625-2800  
FAX: (619) 625-2810

San Diego (92123)  
Hamilton/Hallmark - #02  
4545 Viewridge Avenue  
TEL: (619) 571-7540  
FAX: (619) 277-6136

San Diego (92123)  
Marshall Industries  
5961 Kearny Villa Road  
TEL: (619) 627-4140  
FAX: (619) 627-4163

San Diego (92123)  
Wyle Laboratories-EMG  
9525 Chesapeake Drive  
TEL: (619) 565-9171  
FAX: (619) 565-6512

San Jose (95131)  
Hamilton/Hallmark - #03  
2105 Lundy Avenue  
TEL: (408) 435-3500  
FAX: (408) 435-3720

San Jose (95131-1326)  
Future Electronics Corp.  
2220 O'Toole Avenue  
TEL: (408) 434-1122  
FAX: (408) 433-0822

San Jose (95134)  
Pioneer Tech.  
134 Rio Robles  
TEL: (408) 954-9100  
FAX: (408) 954-9113

San Jose (95119)  
Zeus Electronics  
6276 San Ignacio Ave., Ste. E  
TEL: (408) 629-4789  
FAX: (408) 629-4792

Santa Clara (95052)  
Wyle Distribution Group  
3000 Bowers Avenue  
TEL: (408) 727-2500  
TWX: (910) 379-6480  
FAX: (408) 727-5896

Sunnyvale (94089)  
Bell Industries  
1161 No. Fairroads Avenue  
TEL: (408) 734-8370  
(800) 525-6666  
FAX: (408) 734-8875

Woodland Hills (91367)  
Hamilton/Avnet - #46  
21150 Califa Street  
TEL: (818) 594-0404  
FAX: (818) 594-8234

Yorba Linda (92686)  
Zeus Electronics  
22700 Savi Ranch Pkwy.  
TEL: (714) 921-9000  
FAX: (714) 921-2715

### COLORADO

Lakewood (80215)  
Future Electronics Corp.  
12600 W. Colfax Avenue, Ste. B110  
TEL: (303) 232-2008  
(800) 950-3532  
FAX: (303) 232-2009

Denver (80222)  
Bell Industries  
1873 S. Bellaire Street, Ste. 100  
TEL: (303) 691-9270  
(800) 525-6666  
FAX: (303) 691-9036

Englewood (80111)  
Hamilton/Hallmark - #06  
12503 E. Euclid Drive, Ste. 20  
TEL: (303) 799-7800  
FAX: (303) 790-4991

Thornton (80241)  
Marshall Industries  
12351 N. Grant Street, Ste A  
TEL: (303) 451-8444  
FAX: (303) 457-2899

Thornton (80241)  
Wyle Distribution Group  
451 E. 124th Avenue  
TEL: (303) 457-9953  
FAX: (303) 457-4831

### CONNECTICUT

Cheshire (06410)  
Future Electronics Corp.  
Westgate Office Center  
700 West Johnson Ave.  
TEL: (203) 250-0083  
FAX: (203) 250-0081

Cheshire (06410)  
Hamilton/Hallmark - #21  
125 Commerce Court, Unit 6  
TEL: (203) 797-2800  
FAX: (203) 272-1704

Shelton (06484)  
Pioneer Std.  
2 Trap Falls Road  
TEL: (203) 929-5600  
FAX: (203) 929-9791

Meriden (06413)  
Bell Industries  
1064 E. Main Street  
TEL: (203) 639-6000  
(800) 525-6666  
FAX: (203) 639-6005

Wallingford (06492)  
Marshall Industries  
20 Sterling Drive  
Barnes Industrial Park  
TEL: (203) 265-3822  
FAX: (203) 284-9285

### FLORIDA

Altamonte Springs (32701)  
Bell Industries  
650 S. North Lake Blvd., Ste. 400  
TEL: (407) 339-0078  
(800) 525-6666  
FAX: (407) 339-0139

Altamonte Springs (32701)  
Future Electronics Corp.  
650 S. Northlake Blvd.  
TEL: (407) 767-8414  
FAX: (407) 834-9318

Altamonte Springs (32701)  
Marshall Industries  
380 S. Northlake Blvd., Ste. 1024  
TEL: (407) 767-8585  
FAX: (407) 767-8676

Altamonte Springs (32701)  
Pioneer Tech.  
337 South Northlake Blvd. #1000  
TEL: (407) 834-9090  
FAX: (407) 834-0865

Deerfield Beach (33442)  
Pioneer Tech.  
674 S. Military Trail  
TEL: (305) 428-8877  
FAX: (305) 481-2950

Fort Lauderdale (33309)  
Hamilton/Hallmark - #17  
3350 N.W. 53rd Street, Ste. 105  
TEL: (305) 484-5016  
FAX: (305) 484-4740

Fort Lauderdale (33309)  
Marshall Industries  
2700 W. Cypress Creek Road, Ste. D114  
TEL: (305) 977-4880  
FAX: (305) 977-4887

Lake Mary (32746)  
Zeus Electronics  
37 Skyline Drive, Bldg. D, Ste. 3101  
TEL: (407) 333-3055  
FAX: (407) 333-9681

Largo (34641)  
Future Electronics  
2200 Tall Pines Drive, Ste. 108  
TEL: (813) 330-1222  
FAX: (813) 338-9598

## U. S. Distributors (Cont'd)

### GEORGIA

Duluth (30136)  
Hamilton/Hallmark - #15  
3425 Corporate Way  
TEL: (404) 447-7500  
FAX: (404) 625-5490

Duluth (30136)  
Pioneer Tech.  
4250C Rivergreen Parkway  
TEL: (404) 623-1003  
FAX: (404) 623-0665

Norcross (30071)  
Bell Industries  
3000 Business Park Drive #D  
TEL: (404) 446-7167  
(800) 525-6666  
FAX: (404) 446-7264

Norcross (30071)  
Future Electronics Corp.  
4960 Peachtree Ind., Bldg., Ste. 230  
TEL: (404) 441-7676  
FAX: (404) 441-7580

Norcross (30093)  
Marshall Industries  
5300 Oakbrook Pkwy., Ste. 140  
TEL: (404) 923-5750  
FAX: (404) 923-2743

### ILLINOIS

Addison (60101)  
Pioneer Std.  
2171 Executive Drive, Ste. 200  
TEL: (708) 495-9680  
FAX: (708) 495-9831

Bensenville (60106)  
Hamilton/Hallmark - #10  
1130 Thorndale Avenue  
TEL: (708) 860-7780  
FAX: (708) 773-7969

Elk Grove Village (60007)  
Bell Industries  
870 Cambridge Drive  
TEL: (708) 640-1910  
(800) 525-6666  
FAX: (708) 640-1928

Hoffman Estates (60195)  
Future Electronics Corp.  
3150 W. Higgins Road, Ste. 160  
TEL: (708) 882-1255  
WATS: (800) 933-9841  
FAX: (708) 490-9290

Schaumburg (60173)  
Marshall Industries  
50 E. Commerce Drive, Unit I  
TEL: (708) 490-0755  
FAX: (708) 490-0569

### INDIANA

Fort Wayne (46803)  
Bell Industries  
3433 E. Washington Blvd.  
TEL: (219) 422-4300  
(800) 525-6666  
FAX: (219) 423-3420

Indianapolis (46268)  
Bell Industries  
P.O. Box 6885  
5230 W. 79th Street  
TEL: (317) 875-8200  
(800) 525-6666  
FAX: (317) 875-8219

Indianapolis (46268)  
Hamilton/Hallmark - #28  
4275 W. 96th Street  
TEL: (317) 872-8875  
FAX: (317) 876-7165

Indianapolis (46240)  
Pioneer Std.  
9350 N. Priority Way West Drive  
TEL: (317) 573-0880  
WATS: (800) 332-5503 (IN)  
WATS: (800) 428-9128 (IL, KY)  
FAX: (317) 573-0979

### IOWA

Cedar Rapids (52402)  
Hamilton/Hallmark - #44  
2335-A Blairsferry N.E.  
TEL: (319) 393-0033  
WATS: (800) 332-4757  
FAX: (319) 393-7050

### KANSAS

Lenexa (66219)  
Hamilton/Hallmark - #58  
15313 W. 95th  
TEL: (913) 888-1055  
FAX: (913) 541-7951

Lenexa (66214)  
Marshall Industries  
10413 W. 84th Terrace  
TEL: (913) 492-3121  
FAX: (913) 492-6205

Overland Park (66212)  
Future Electronics Corp.  
8826 Santa Fe Drive, Ste. 150  
TEL: (913) 649-1531  
FAX: (913) 649-1786

### KENTUCKY

Lexington (40511-1001)  
Hamilton/Hallmark  
1847 Mercer Road, Ste. G  
TEL: (606) 259-1475  
FAX: (606) 288-4936

### MARYLAND

Columbia (21046)  
Bell Industries  
8945 Guilford Road, Ste. 130  
TEL: (410) 290-5100  
(800) 525-6666  
FAX: (410) 290-8006

Columbia (21046)  
Future Electronics Corp.  
6716 Alexander Bell Drive, Ste. 101  
TEL: (410) 290-0600  
FAX: (410) 290-0328

Columbia (21046-2101)  
Hamilton/Hallmark - #12  
10240 Old Columbia Road  
TEL: (410) 988-9800  
FAX: (410) 381-2036

Gaithersburg (20877)  
Pioneer Tech.  
9100 Gaither Road  
TEL: (301) 921-0660  
FAX: (301) 921-4255

Silver Springs (20904)  
Marshall Industries  
2221 Broad Birch Drive, Ste. G  
TEL: (301) 622-1118  
FAX: (301) 622-0451

### MASSACHUSETTS

Andover (01810)  
Bell Industries  
100 Burr Road, Suite 106  
TEL: (508) 474-8880  
(800) 525-6666  
FAX: (508) 474-8902

Bolton (01740)  
Future Electronics Corp.  
41 Main Street  
TEL: (508) 779-3000  
FAX: (508) 779-5143

Burlington (01803)  
Wyle  
15 Third Ave.  
TEL: (617) 272-7300  
FAX: (617) 272-6809

Lexington (02173)  
Pioneer Std.  
44 Hartwell Ave.  
TEL: (617) 861-9200  
FAX: (617) 863-1547

Peabody (01960)  
Hamilton/Hallmark - #18  
10 M Centennial Drive  
TEL: (508) 532-3701  
FAX: (508) 532-9802

Wilmington (01877)  
Zeus Electronics  
25 Upton Drive  
TEL: (508) 658-4776  
FAX: (508) 694-2199

Wilmington (01887)  
Marshall Industries  
33 Upton Drive  
TEL: (508) 658-0810  
FAX: (508) 657-5931

### MICHIGAN

Grand Rapids (49512)  
Future Electronics Corp.  
4505 Broadmoor SE  
TEL: (616) 698-6800  
WATS: (800) 334-6808  
FAX: (616) 698-6821

Grand Rapids (49512)  
Pioneer Std.  
4394 Broadmoor Ave. SE, Ste. 235  
TEL: (616) 698-1801  
FAX: (616) 698-1831

Livonia (48150)  
Future Electronics Corp.  
35200 Schoolcraft Road, Ste. 106  
TEL: (313) 261-5270  
FAX: (313) 261-8175

Livonia (48150)  
Marshall Industries  
31067 Schoolcraft Road  
TEL: (313) 525-5850  
FAX: (313) 525-5855

Plymouth (48270)  
Pioneer Std.  
44190 Plymouth Oaks Drive  
TEL: (313) 416-2157  
FAX: (313) 416-2415

Novi (40375)  
Hamilton/Hallmark - #66  
41650 Gardenbrook, Ste. 100  
TEL: (313) 347-4271  
FAX: (313) 347-4021

### MINNESOTA

Bloomington (55341)  
Hamilton/Hallmark - #63  
9401 James Avenue South, Ste. 140  
TEL: (612) 881-2600  
FAX: (612) 881-9461

Eden Prairie (55344)  
Future Electronics Corp.  
10025 Valley View Road, Ste. 196  
TEL: (612) 944-2200  
FAX: (612) 944-2520

Eden Prairie (55344)  
Pioneer Std.  
7625 Golden Triangle Drive  
TEL: (612) 944-3355  
FAX: (612) 944-3794

Plymouth (55447)  
Marshall Industries  
3955 Annapolis Lane  
TEL: (612) 559-2211  
FAX: (612) 559-8321

### MISSOURI

Earth City (63045)  
Hamilton/Hallmark - #05  
3783 Rider Trail South  
TEL: (314) 291-5350  
FAX: (314) 291-0362

Saint Louis (63141)  
Future Electronics Corp.  
12125 Woodcrest Executive Drive,  
Ste. 220  
TEL: (314) 469-6805  
WATS: (800) 727-6805  
FAX: (314) 469-7226

### NEW HAMPSHIRE

See Massachusetts

### NEW JERSEY

Fairfield (07004)  
Bell Industries  
271 Route 46 West, Ste. F202-203  
TEL: (201) 227-6060  
(800) 525-6666  
FAX: (201) 227-2626

Fairfield (07006)  
Marshall Industries  
101 Fairfield Road  
TEL: (201) 882-0320  
FAX: (201) 882-0095

Fairfield (07006)  
Pioneer Std.  
14 "A" Madison Road  
TEL: (201) 575-3510  
FAX: (201) 575-3454

Marlton (08053)  
Future Electronics Corp.  
12 E. Stow Road, Ste. 200, Bldg. 12  
TEL: (609) 596-4080  
FAX: (609) 596-4266

Mt. Laurel (08054)  
Marshall Industries  
158 Gaither Drive, Unit 100  
TEL: (609) 234-9100 (NJ)  
TEL: (215) 627-1920 (PA)  
FAX: (609) 778-1819

### NEW MEXICO

Albuquerque (87123)  
Bell Industries  
11728 Linn N.E.  
TEL: (505) 292-2700  
(800) 525-6666  
FAX: (505) 275-2819

Albuquerque (87109-3147)  
Hamilton/Hallmark - #22  
7801 Academy Road NE-Bldg. 2, Ste. 102  
TEL: (505) 345-0001  
TWX: (910) 989-0614  
FAX: (505) 828-0360

### NEW YORK

Binghamton (13905)  
Pioneer Std.  
1249 Front Street, #201  
TEL: (607) 722-9300  
FAX: (607) 722-9562

Endicott (13760)  
Marshall Industries  
100 Marshall Drive  
TEL: (607) 798-1611  
FAX: (607) 797-7031

Fairport (14450)  
Pioneer Std.  
840 Fairport Park  
TEL: (716) 381-7070  
FAX: (716) 381-5955

Hauppauge (11788)  
Future Electronics Corp.  
801 Motor Parkway  
TEL: (516) 234-4000  
FAX: (516) 234-6183

Hauppauge (11788)  
Hamilton/Hallmark - #20  
933 Motor Parkway  
TEL: (516) 434-7470  
FAX: (516) 434-7491

Port Chester (10573)  
Zeus Electronics  
100 Midland Avenue  
TEL: (914) 937-7400  
FAX: (914) 937-2553

Rochester (14623)  
Future Electronics Corp.  
333 Metro Park  
TEL: (716) 272-1120  
FAX: (716) 272-7182

Rochester (14623)  
Hamilton/Hallmark - #61  
1057 E. Henrietta Road  
TEL: (716) 475-9130  
FAX: (716) 475-9119

## U. S. Distributors (Cont'd)

### NEW YORK (Cont'd)

Rochester (14624)  
Marshall Industries  
1250 Scottville Road  
TEL: (716) 235-7620  
TWX: (510) 253-5526  
FAX: (716) 235-0052

Syracuse (13212-4513)  
Future Electronics Corp.  
200 Salina Meadows Pkwy., Ste. 130  
TEL: (315) 451-2371  
FAX: (315) 451-7258

Woodbury (11797)  
Pioneer Std.  
60 Crossways Park W.  
TEL: (516) 921-8700  
FAX: (516) 921-2143

### NORTH CAROLINA

Concord (28026)  
Future Electronics  
Charlotte Motor Speedway, Ste. 314  
P.O. Box 600  
TEL: (704) 455-9030  
FAX: (704) 455-9173

Morrisville (27560)  
Pioneer Tech.  
2200 Gateway Center Blvd., Ste. 215  
TEL: (919) 460-1530  
FAX: (919) 460-1540

Raleigh (27604)  
Future Electronics Corp.  
5225 Capitol  
1 North Commerce Center  
TEL: (919) 790-7111  
FAX: (919) 790-9022

Raleigh (27604)  
Hamilton/Hallmark - #24  
3510 Spring Forrest Road  
TEL: (919) 878-0819, X210  
FAX: (919) 954-0940

Raleigh (27604)  
Marshall Industries  
5224 Greens Dairy Road  
TEL: (919) 878-9882  
FAX: (919) 872-2431

### OHIO

Cleveland (44105)  
Pioneer Std.  
4800 E. 131st Street  
TEL: (216) 587-3600  
FAX: (216) 587-3906

Dayton (45459)  
Bell Industries  
446 Windsor Park Drive  
TEL: (513) 434-8231  
(800) 525-6666  
FAX: (513) 434-8103

Dayton (45459)  
Hamilton/Hallmark - #64  
7760 Washington Village Drive  
TEL: (513) 439-6721  
FAX: (513) 439-6705

Dayton (45414)  
Marshall Industries  
3520 Park Center Drive  
TEL: (513) 898-4480  
FAX: (513) 898-9835

Dayton (45424)  
Pioneer Std.  
4433 Interpoint Blvd.  
TEL: (513) 236-9900  
FAX: (513) 236-8133

Mayfield Heights (44124)  
Future Electronics Corp.  
6009 E Lander Haven Drive  
TEL: (216) 449-6996  
FAX: (216) 449-8987

Solon (44139)  
Marshall Industries  
30700 Bainbridge Road Unit A  
TEL: (216) 248-1788  
FAX: (216) 248-2312

Worthington (43085)  
Hamilton/Hallmark - #79  
777 Dearborn Lane, Ste. L  
TEL: (614) 888-3313  
WATS: (800) 767-0392  
FAX: (614) 888-0767

### OKLAHOMA

Tulsa (74146)  
Hamilton/Hallmark - #46  
5411 S. 125th East Avenue, Ste. 305  
TEL: (918) 252-7297  
FAX: (918) 254-6207

Tulsa (74146)  
Pioneer  
9717 E. 42nd Street, Ste. 105  
TEL: (918) 665-7840  
FAX: (918) 665-1891

### OREGON

Beaverton (97005)  
Bell Industries  
9275 S.W. Nimbus  
TEL: (503) 644-3444  
(800) 525-6666  
FAX: (503) 520-1948

Beaverton (97006)  
Future Electronics Corp.  
Cornell Oaks Corp. Center  
15236 N.W. Greenbrier  
TEL: (503) 645-9454  
FAX: (503) 645-1559

Beaverton (97005)  
Hamilton/Hallmark - #27  
9750 SW Nimbus Ave.  
TEL: (503) 526-6200  
WATS: (800) 962-8648  
FAX: (503) 641-5939

Beaverton (97005)  
Marshall Industries  
9705 S.W. Gemini  
TEL: (503) 644-5050  
FAX: (503) 646-8256

Beaverton (97005)  
Wyle Laboratories-EMG  
9640 Sunshine Ct.  
Bldg. G-200  
TEL: (503) 643-7900  
FAX: (503) 646-5466

### PENNSYLVANIA

Horsham (19044)  
Pioneer Tech.  
500 Enterprise Road  
Keith Valley Business Center  
TEL: (215) 674-4000  
TWX: (510) 665-6778  
FAX: (215) 674-3107

Pittsburgh (15205)  
Marshall Electronics  
401 Parkwayview Drive  
TEL: (412) 788-0441  
FAX: (412) 788-0447

Pittsburgh (15238)  
Pioneer Std.  
259 Kappa Drive  
TEL: (412) 782-2300  
FAX: (412) 963-8255

Traverse (19053)  
Bell Industries  
2556 Metropolitan Drive  
TEL: (215) 953-2800  
(800) 525-6666  
FAX: (215) 364-4927

### TEXAS

Austin (78759)  
Future Electronics  
9020 II Capital of Texas Hwy. N.  
TEL: (512) 502-0991  
(800) 678-0991  
FAX: (512) 502-0740

Austin (78727)  
Hamilton/Hallmark - #26  
12211 Technology Blvd.  
TEL: (512) 258-8848  
FAX: (512) 258-3777

Austin (78758)  
Pioneer Std.  
1826 D Kramer Lane  
TEL: (512) 835-4000  
FAX: (512) 835-9829

Austin (78759)  
Wyle Distribution  
4030 W. Braker Lane, Ste. 420  
TEL: (512) 345-8853  
FAX: (512) 345-9330

Dallas (75244)  
Pioneer Std.  
13765 Beta Road  
TEL: (214) 386-7300  
FAX: (214) 490-6419

Houston (77082)  
Future Electronics Corp.  
11271 Richmond Ave., Ste. 106  
TEL: (713) 556-8696  
FAX: (713) 589-7069

Houston (77063)  
Hamilton/Hallmark - #11  
8000 West Glen  
TEL: (713) 781-6100  
FAX: (713) 953-8420

Houston (77040)  
Marshall Industries  
10681 Haddington  
TEL: (713) 467-1666  
FAX: (713) 467-9805

Houston (77099)  
Pioneer Std.  
10530 Rockley Road, Ste. 100  
TEL: (713) 495-4700  
FAX: (713) 495-5642

Houston (77099)  
Wyle Distribution  
11001 S. Willcrest, #100  
TEL: (713) 879-9953  
FAX: (713) 879-6540

Richardson (75081)  
Bell Industries  
1701 Greenville Avenue, Ste. 306  
TEL: (214) 690-0486  
(800) 525-6666  
FAX: (214) 690-0467

Richardson (75081)  
Future Electronics Corp.  
1850 N. Greenville Avenue, Ste. 146  
TEL: (214) 437-2437  
FAX: (214) 669-2347

Richardson (75081)  
Marshall Industries  
1551 N. Glenville Drive  
TEL: (214) 705-0604  
FAX: (214) 705-0675

Richardson (75081)  
Wyle Distribution  
1810 N. Greenville Avenue  
TEL: (214) 235-9953  
FAX: (214) 644-5064

Carrollton (75006)  
Zeus Electronics  
3220 Commander Drive  
TEL: (214) 380-4330  
FAX: (214) 447-2222

### UTAH

Midvale (84047)  
Bell Industries  
6912 South 185 West, Ste. B  
TEL: (801) 561-9691  
(800) 525-6666  
FAX: (801) 255-2477

Orem (84058)  
Wyle Laboratories-EMG  
973 S. 700 E.  
TEL: (800) 414-4144  
FAX: (801) 226-0210

Salt Lake City (84106)  
Future Electronics Corp.  
3450 South Highland Drive, Ste. 301  
TEL: (801) 467-4448  
FAX: (801) 467-3604

Salt Lake City (84121)  
Hamilton/Hallmark - #09  
1100 E. 6600 S., Ste. 120  
TEL: (801) 266-2022  
FAX: (801) 263-0104

Salt Lake City (84119-1552)  
Marshall Industries  
2355 S. 1070 W #1D  
TEL: (801) 485-1551  
FAX: (801) 487-0936

West Valley City (84119)  
Wyle Laboratories-EMG  
1325 W. 2200 S., Ste. E  
TEL: (801) 974-9953  
FAX: (801) 972-2524

### WASHINGTON

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1715 114th Ave., S.E., Ste. 208  
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(800) 525-6666  
FAX: (206) 646-8559

Bellevue (98007)  
Pioneer Tech.  
2800 156th Avenue, S.E.  
TEL: (206) 644-7500  
FAX: (206) 644-7300

Bothell (98011)  
Future Electronics Corp.  
19102 N. Creek Pkwy., Ste. 118  
TEL: (206) 489-3400  
FAX: (206) 489-3411

Bothell (98011)  
Marshall Industries  
11715 N. Creek Pkwy, South, Ste. 112  
TEL: (206) 486-5747  
FAX: (206) 486-6964

Redmond (98052)  
Hamilton/Hallmark - #07  
8630 154th Avenue, N.E.  
TEL: (206) 881-6697  
FAX: (206) 867-0159

Redmond (98052)  
Wyle Distribution Group  
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FAX: (206) 881-1567

### WISCONSIN

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120 Bishops Way, Ste. 163  
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FAX: (414) 784-8207

Milwaukee (53214)  
Marsh Electronics, Inc.  
1563 South 101st Street  
TEL: (414) 475-6000  
FAX: (414) 771-2847

New Berlin (53146)  
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2440 S. 179th Street  
TEL: (414) 780-7200  
FAX: (414) 780-7201

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(800) 525-6666  
FAX: (414) 547-6547

Waukesha (53186)  
Future Electronics Corp.  
20875 Crossroads Cir., Ste. 200  
TEL: (414) 786-1884  
FAX: (414) 786-0744

Waukesha (53186)  
Marshall Industries  
20900 Swenson Drive  
TEL: (414) 797-8400  
FAX: (414) 797-8270

## Canadian Distributors

### ALBERTA

Calgary (T1Y 6B5)  
Future Electronics Corp.  
3833-29th Street N.E.  
TEL: (403) 250-5550  
FAX: (403) 291-7054

Edmonton (T6E 5N9)  
Future Electronics Corp.  
4606 97th Street  
TEL: (403) 438-2858  
FAX: (403) 434-0812

### BRITISH COLUMBIA

Burnaby (V5A 4N6)  
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FAX: (604) 294-1206

Vancouver (V5K 4X7)  
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1695 Boundary Road  
TEL: (604) 294-1166  
FAX: (604) 294-1206

### MANITOBA

Winnipeg (R3H 0N8)  
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106 King Edward Court  
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FAX: (204) 783-8133

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Brampton (L6O 5G3)  
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FAX: (416) 458-1613

Mississauga (L4V 1W5)  
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5935 Airport Road, Ste.200  
TEL: (416) 612-9200  
FAX: (416) 612-9185

Mississauga (L5T 2L1)  
Hamilton/Hallmark - #59  
151 Superior Blvd.  
TEL: (416) 564-6060  
FAX: (416) 564-6033

Ottawa (K2C 3P2)  
Future Electronics  
Baxter Centre  
1050 Baxter Road  
TEL: (613) 820-8313  
FAX: (613) 820-3271

### QUEBEC

Pointe Claire (H9R 5C7)  
Future Electronics  
237 Hymus Boulevard  
TEL: (514) 694-7710  
TLX: 05-823599  
FAX: (514) 695-3707

Pointe Claire (H9R 5P7)  
Marshall Industries  
148 Brunswick Blvd.  
TEL: (514) 694-8142  
FAX: (514) 694-6989

Quebec (G2E 5G5)  
Future Electronics Corp.  
1000 Avenue Street Jean-Baptiste, Ste. 100  
TEL: (418) 877-6666  
FAX: (418) 877-6671

Saint Laurent (H4S 1P8)  
Hamilton/Hallmark - #65  
2795 Rue Halpern  
TEL: (514) 335-1000  
TLX: (610) 421-3731  
FAX: (514) 335-2381

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Bacher Electronics GmbH  
Eitnergasse 6  
1223 Wien  
TEL: (43) 0222 81602215  
TLX: 131532  
FAX: (43) 0222 863211201

EBV Elektronik  
Diefenbachgasse 35/6  
1150 Wien  
TEL: (43) 0222 8941774  
FAX: (43) 0222 8941775

### BELGIUM

Diode  
Keibergh II  
Minervastraat, 14/B2  
1930 Zaventem  
TEL: (32) 2 7254660  
FAX: (32) 2 7254511

EBV Elektronik  
Eexelsiorlaan 35  
1930 Zaventem  
TEL: (32) 02 7209936  
FAX: (32) 02 7208152

Sonetech CY  
Limburg Styrum, 243  
B-1810 Wemmel  
TEL: (32) 2 4600707  
FAX: (32) 2 4601200

### DENMARK

TEMIC  
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FAX: (45) 42 648949

### FINLAND

Galedius Tehnik OK  
P.O. Box 125  
Magistratsporten 4A  
SF-00241 Helsinki  
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FAX: (358) 014 82 189  
ITT Components Group  
Distribution GmbH & Co  
P.O. Box 25 (Tyopajaku 5)  
PL 34  
00581 Helsinki  
TEL: (358) 0-739100  
FAX: (358) 0-712414

### FRANCE

Almex  
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B.P. 102  
92164 ANTONY CEDEX  
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FAX: (33) 1 46-66-60-28

Arrow Electronique  
73-79 Rue des Solets  
Silic 585  
94663 Rungis  
TEL: (33) 1 49-78-49-78  
FAX: (33) 1 49-78-05-96

EBV Elektronik  
16, rue de Gaillie  
77436 CHAMPS SUR MARNE  
TEL: (33) 1 64-68-86-00  
FAX: (33) 1 64-68-27-67

I.T.T. Multicomposants  
16 Avenue des Andes  
Za de Courtaubeuf  
BP 16  
91941 Les Ulis Cedex A  
TEL: (33) 1 64-46-02-00  
TLX: 603351  
FAX: (33) 1 64-46-95-95

SCAIB  
80 Rue d'Arcueil  
94523 Rungis Cedex  
TEL: (33) 1 46-87-23-13  
TLX: 20467F  
FAX: (33) 1 45-60-55-49

TEMIC  
3, Avenue du Centre  
B.P. 309  
78054 Saint-Quentin-en-Yvelines  
TEL: (33) 1 30-60-70-00  
FAX: (33) 1 30-64-06-93

### GERMANY

Alfred Neye Enatechnik GmbH  
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Postfach 1246 - 25443 Quickborn  
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FAX: (49) 4106 61223

Alfred Neye Enatechnik GmbH  
Hildesheimer Strasse 31 - 30169 Hannover  
TEL: (49) 511 816038  
FAX: (49) 511 816048

Alfred Neye Enatechnik GmbH  
Ahnenweg 2 - 40219 Dusseldorf  
TEL: (49) 211 303010  
FAX: (49) 211 3030130

Alfred Neye Enatechnik GmbH  
Rheinstrasse 24 - 64283 Darmstadt  
TEL: (49) 6151 26446  
FAX: (49) 6151 294171

Alfred Neye Enatechnik GmbH  
Breitwiesenstrasse 25 - 70565 Stuttgart  
Postfach - 70507 Stuttgart  
TEL: (49) 711 7889770  
FAX: (49) 711 7889744

Alfred Neye Enatechnik  
Bucherstrasse 100 - 90408 Nürnberg  
TEL: (49) 911 34750  
FAX: (49) 911 347530

Alfred Neye Enatechnik GmbH  
Henschelring 5 - 85551 Kirchheim/München  
TEL: (49) 89 9099990  
FAX: (49) 89 9099940

Alfred Neye Enatechnik GmbH  
Max-Stromeier Strasse 3 - 78467 Konstanz  
TEL: (49) 7531 67181  
FAX: (49) 7531 67260

Alfred Neye Enatechnik GmbH  
Leningrader Strasse 15 - 01069 Dresden  
TEL: (49) 375 4873341  
FAX: (49) 375 4872588

CED Ditrone GmbH  
Julius-Hölder-Strasse 42 - 70597 Stuttgart  
Postfach 700159 - 70571 Stuttgart  
TEL: (49) 0711 7200110  
FAX: (49) 0711 7200132

CED Ditrone GmbH  
Bernbacherstrasse 9  
90768 Fürth  
TEL: (49) 911 752216  
FAX: (49) 911 7520064

CED Ditrone GmbH  
Ebertshelmer Strasse 12 - 67280 Quirheim  
TEL: (49) 6359 83201  
FAX: (49) 6359 83201

Ditron  
Behemstrasse 3 - 10585 Berlin  
Postfach 100208 - 10562 Berlin  
TEL: (49) 030 3421041/44  
FAX: (49) 030 3419003

EBV Elektronik GmbH  
Böblinger Strasse 13 - 71229 Leonberg  
TEL: (49) 7152 300090  
FAX: (49) 7152 759558

EBV Elektronik GmbH  
Hans Finsel Str. 4 - 88540 Haar  
Postfach 1109 - 85529 Haar  
D-8013 Haar  
TEL: (49) 089 460960  
FAX: (49) 089 464488

EBV Elektronik GmbH  
Weimarstr 48  
7000 Stuttgart 1  
TEL: (49) 0711 619100  
TLX: 722271  
FAX: (49) 07512 75958

EBV Elektronik GmbH  
Versener Strasse 24 - 41462 Neuss  
TEL: (49) 2132 530072  
FAX: (49) 2131 59300087

EBV Elektronik GmbH  
In der Meineworth 21 - 30938 Burgwedel  
Postfach 1355 - 30929 Burgwedel  
TEL: (49) 5139 808070  
FAX: (49) 5139 5199

EBV Elektronik GmbH  
Schenckstrasse 99 - 60489 Frankfurt 99  
TEL: (49) 069 785037  
FAX: (49) 069 7894458

Elkose GmbH Elektronik Vertrieb  
ITT Multikomponent GmbH  
Elektronik Vertrieb  
Bahnhofstrasse 44 - 71696 Möglingen  
Postfach 1246 - 71693 Möglingen  
TEL: (49) 07141 4870  
FAX: (49) 07141 487210

Ing. Büro Rainer König  
Königsberger Strasse 16A - 12207 Berlin  
Postfach 420 - 12174 Berlin  
TEL: (49) 30 7689090  
FAX: (49) 30 7738363

Spoerle Electronic  
Kackerstrasse 10 - 52072 Aachen  
TEL: (49) 241 899690  
FAX: (49) 241 81162

Spoerle Electronic  
Rudower Strasse 27-29 - 12351 Berlin  
Postfach 47645 - 12315 Berlin  
TEL: (49) 30 606011  
TLX: 186029  
FAX: (49) 30 6014057

Spoerle Electronic  
Hildebrandstrasse 11 - 44319 Dortmund  
Postfach 130362 - 44313 Dortmund  
TEL: (49) 231 218010  
TLX: 822555  
FAX: (49) 231 2180167



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Spoerle Electronic  
Im Gefährth 11a - 63303 Dreieich  
Postfach 102140 - 63267 Dreieich  
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TLX: 417983  
FAX: (49) 6103 304201

Spoerle Electronic  
Hans-Bunte-Strasse 2 - 79108 Freiburg  
Postfach 5607 - 79023 Freiburg  
TEL: (49) 761 510450  
TLX: 7721994  
FAX: (49) 761 502233

Spoerle Electronic  
Rodeweg 18 - 37081 Göttingen  
Postfach 3352 - 37023 Göttingen  
TEL: (49) 551 9040  
TLX: 96733  
FAX: (49) 551 90446/48

Spoerle Electronic  
Winsbergweg 42 - 22525 Hamburg  
Postfach 540824 - 22508 Hamburg  
TEL: (40) 40 8531340  
TLX: 2164536  
FAX: (49) 40 85313491

Spoerle Electronic  
Roscherstrasse 31 - 04105 Leipzig  
TEL: (49) 341 5647201  
FAX: (49) 341 5852087

Spoerle Electronic  
Föhrlinger Allee 17 - 85774 Unterföhring  
Postfach 1155 - 85765 Unterföhring  
TEL: (49) 89 959990  
FAX: (49) 89 9509999/97

Spoerle Electronic Rathsbergstrasse 17 -  
90411 Nürnberg  
TEL: (49) 911 521560  
FAX: (40) 911 5215635

Spoerle Electronic  
Höpfelheimer Strasse 5 - 74321  
Biengheim-Bissingen  
Postfach 1727 - 74307 Bietigheim-Bissingen  
TEL: (49) 7142 70030  
FAX: (40) 7142 700360

TEMIC TELEFUNKEN microelectronic  
Theresienstrasse 2  
D-74072 Heilbronn  
Postfach 35 35  
D-74025 Heilbronn  
TEL: (49) 07131 67-0  
FAX: (49) 07131 67-2100

### ITALY

Canel Electronica Srl  
Viale Degli Artigianelli 6  
I-20159 Milan  
TEL: (39) 2 668 02 788  
FAX: (39) 2 668 02 919

Dott Ing. Giuseppe De Mico  
S.P.A.  
Via Vittorio Veneto 8  
20060 Cassina de Pecchi  
Milano  
TEL: (39) 02 95343600  
TLX: 330869  
FAX: (39) 02 9522227

EBV Elektronik  
Via C. Prova 34  
20092 Cinisello Balsamo, Milan  
TEL: (39) 2 66017111  
FAX: (39) 2 66017020

ESCO Italiana Spa  
V. Le Casiraghi 355  
20099 Sesto S. Giovanni, Milan  
TEL: (39) 224 09 241  
FAX: (39) 224 09 255

Intesi  
Deutsche ITT Industries  
Viale Milanofiori, E/5  
I-20094 Assago, Milan  
TEL: (39) 282 47 01  
FAX: (39) 282 42 631

TEMIC  
Via Stephenson 94  
20157 Milano  
TEL: (39) 2 33 21 211  
FAX: (39) 2 33 21 201

### NETHERLANDS

EBV  
Planetenbaan 2  
3606 AK Maarssenbroek  
TEL: (31) 03465-62353  
FAX: (31) 03465-64277

DIODE COMPONENTS BV  
Postbus 7139  
5605 JC Eindhoven  
De Run 1120  
5503 LA Veldhoven  
TEL: (31) 40-545430  
FAX: (31) 40-535540

DIODE COMPOSANTS BV  
Coltbaan 17  
3439 NG Nieuwege  
TEL: (31) 3402-91234  
FAX: (31) 3402-46764/35924

### NORWAY

Tähoen A/S  
P.O. Box 140 - Kalbakken  
Kakkolovnskroen 1  
N-0902 Oslo 9  
TEL: (47) 22 16 16 10  
FAX: (47) 22 25 73 17

### PORTUGAL

Redis Logar  
Rua Bernardo Lima  
Nr. 27-1e Izda  
1200 Lisbon  
TEL: (351) 11-520101  
FAX: (351) 11-520004

### SPAIN

ADM Electronica S.A.  
Menorca No. 3  
28009 Madrid  
TEL: (34) 1 409 47 25  
FAX: (34) 1 409 69 03

EBV Elektronik Vertriebs GmbH  
Sucursal Espana  
Calle Maria Tubau, 6  
28049 Madrid  
TEL: (34) 91 358 8608  
FAX: (34) 91 358 9430

TEMIC  
Principe de Vergara, 112  
Apartado 235  
28002 Madrid  
TEL: (34) 1 562 76 00  
FAX: (34) 1 562 75 14

### SWEDEN

ITT Muphkomponent AB  
Anklammagatan 32  
S-171 26 Solna  
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FAX: (46) 08 271 303

TEMIC Nordic A/S  
Kavallerivägen 24, Risne  
P.O. Box 2042  
17202 Sundbyberg, Sweden  
TEL: (46) 8 733-0090  
FAX: (46) 8 733-0558

TH's Elektronik AB  
Arrendevägen 36  
P.O. Box 3027  
16303 Spanga  
TEL: (46) 8 36 2970  
FAX: (46) 8 761 3065

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Ableco A.G.  
Grabenstrasse 9  
8952 Schlieren  
TEL: 1-730-0455  
FAX: 1-730-9801

EBV Elektronik  
Vorstadstr. 37  
8953 Dietikon  
TEL: 1-7401090  
FAX: 1-7415110

FABRIMEX  
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SPOERLE ELECTRONIC  
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8032 Zürich  
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FAX: (41) 1-3832379

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1400 Yverdon-les-Bains  
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FAX: (41) 24-218141

### TURKEY

ERDA Elektronik A.S.  
San Ve Tic A.S.  
Kestkin Kalem Sokak 15  
80300 Esentepe  
Istanbul  
TEL: (90) 1 144-21-68  
FAX: (90) 127 50540

### UNITED KINGDOM

Abacus Electronics Ltd.  
Abacus House  
Bone Lane  
Newbury, Berks RG14 5SP  
TEL: (44) 0 635-36 222  
TLX: 847589  
FAX: (44) 0 635-38670

Abercorn Electronics Ltd.  
Pardovan  
Philip, Lindlithgow EH49 6QZ  
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TLX: 77994  
FAX: (44) 506 834 554

BCD Microelectronics Ltd  
3 Station Road  
Swaffham Bulbeck,  
Cambridge CB8 0NB  
TEL: (44) 0223 812598  
FAX: (44) 0223 812686

Future Electronics  
Poyle Road - Colnbrook  
Berkshire SL3 0E2  
TEL: (44) 0753 687 000  
FAX: (44) 0753 689 100

HB Electronics Ltd.  
Lever Street - Bolton  
Lancs BL3 6BJ  
TEL: (44) 0204 255 44  
TLX: 63478  
FAX: (44) 0204 384911

Macro-Marketing Ltd.  
Burnham Lane  
Slough, Berkshire SL1 6LN  
TEL: (44) 0628 604422  
TLX: 847945  
FAX: (44) 0628 666873

MEMEC Ireland Ltd.  
Block H - Lock Quay  
Clare Street - Limerick  
Rep of Ireland  
TEL: (10) 353 61 411 842  
FAX: (10) 353 61 411 888

Micromark  
159 Boy'n Valley Road  
Maldenhead  
Berkshire SL6 4DT  
TEL: (44) 0628 76176  
FAX: (44) 0628 783799

ROMARTEC Ltd.  
Riversdale  
Honeysuckle Lane  
Headley Lane  
Grays Holt Hant - GU 35 8JA  
TEL: (44) 831 5065 57  
FAX: (44) 428 7219 43

TEMIC UK Ltd.  
Easthampstead Road  
Bracknell  
Berkshire RG12 1LX  
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FAX: (44) 344 427371

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1077 Buenos Aires  
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(54) 1 45-7163  
FAX: (54) 1 440-1533, (54) 1 45-2551

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Lidcombe 2141  
NSW Australia  
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FAX: (61) 2-6471545 (no charge)

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Mt. View, CA 94043  
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TLX: 345545  
FAX: (415) 967-8836

UNIÃO Digital  
Rua Texas, 622  
Brooklin Novo - 04557  
S. Paulo - SP  
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TEL: (55) 11 241-8032  
FAX: (55) 11 533-6780

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TEMIC Hong Kong Limited  
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South Tower, Harbour City  
19 Canton Road, Tsimshatsui  
Kowloon  
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FAX: (852) 3755 733

Willas - Array (Holdings) Ltd.  
Unit 1, 24/F  
Wylar Center Phase 2  
200 Tai Lin Pai Road  
Kwai Chung N.T.  
Kowloon  
TEL: (852) 4183700  
FAX: (852) 4816992

### INDIA

Amaspec (S) Pte Ltd  
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#01-07 Henderson Industrial Park  
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FAX: (65) 2714112

Spectra Innovations Inc.  
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2-Chome Chiyoda-Ku  
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FAX: (81) 3 3506-3499

TOMEN Electronics Corp.  
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Chiyoda-Ku, Tokyo 100  
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FAX: (82) 2-7853643

### MALAYSIA

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Arlington (76006)  
Ion Associates Inc.  
2221 E. Lamar, Ste. 250  
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Ion Associates Inc.  
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Scan Technology (S) Pte Ltd  
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